ILC FEC v2.1

Current and proposed changes on modified front-end card

ILC FEC v2.1 design summary

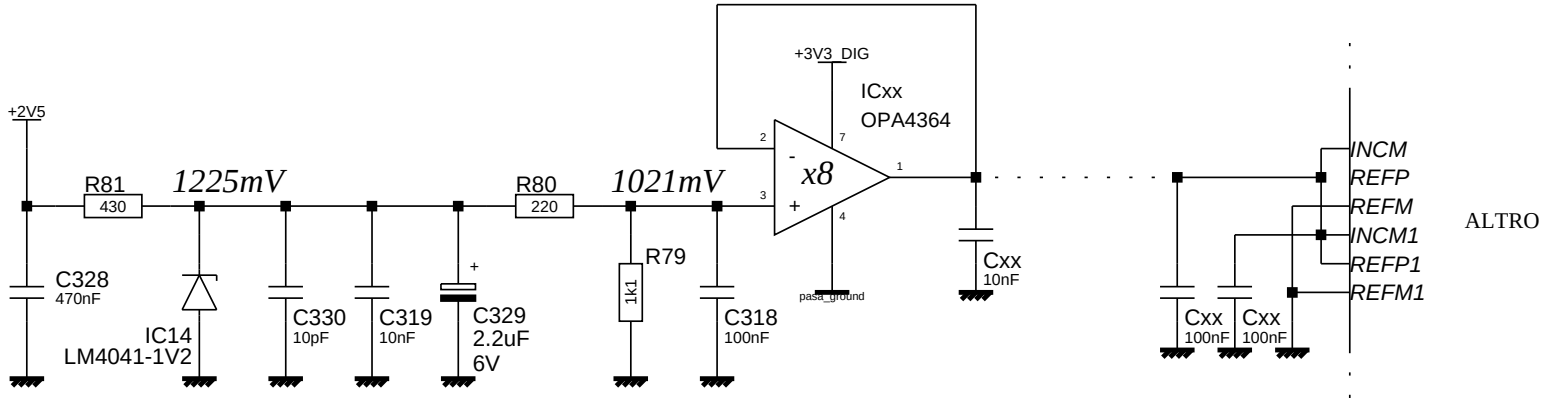
Main differences on version v2.1 prototype vs. v2.0

- ALTRO voltage references not interconnected at ALTRO, routed individually to buffer and connected there
- Additional input voltage for PCA16 regulator in order to reduce dissipation (~2.5V unreg in)
- Kapton-cable input connectors has individual ground reference-plane. Connected to analog ground-plane through several removable jumpers
- All different grounds connected at input through removable jumpers
- Digital and Analog grounds connected with removable jumpers at each ALTRO corner
- Lots of small bugfixes
- v2.1 worked immediately after mounting!

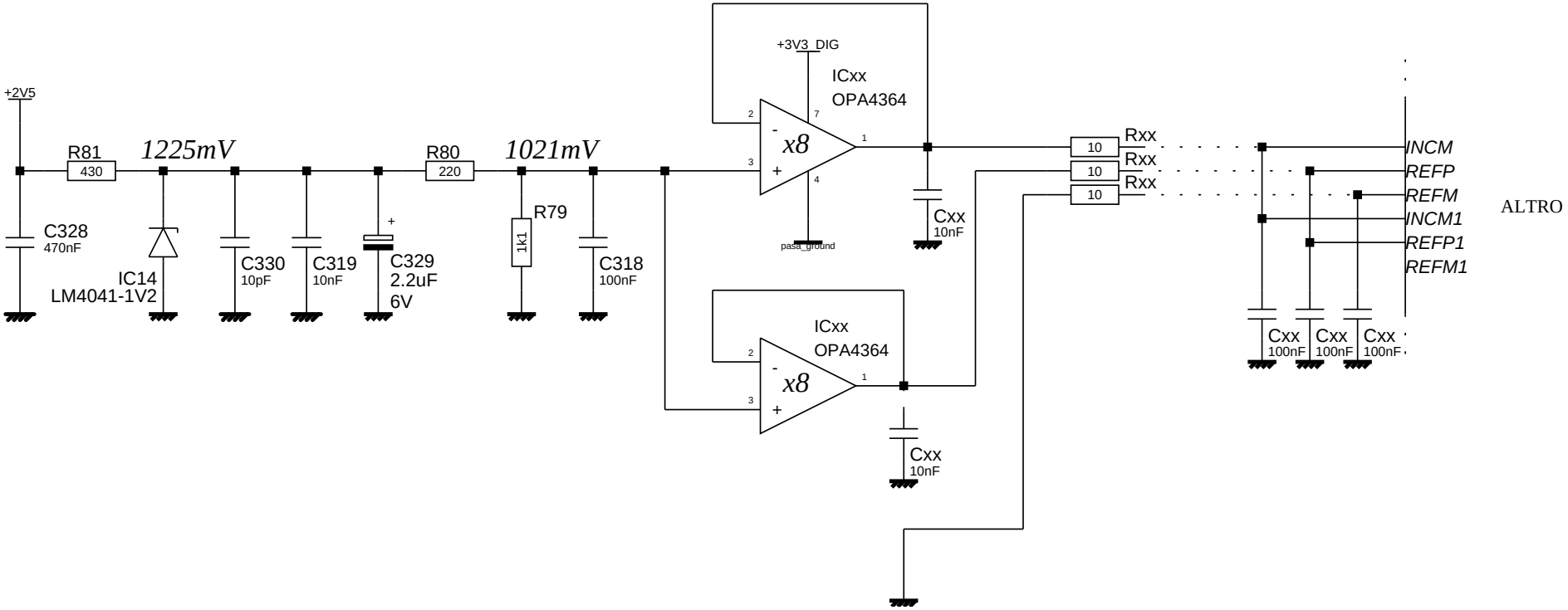
ILC FEC v2.0 reference voltage

- ALTRO voltage reference design duplicated from ALICE FEC i.e. negative reference grounded and positive+common mode references connected to reference generator through buffer
- Fixed voltage, variable by changing resistors in voltage divider
- All ALTRO references common : change one = change all, negative reference fixed at ground.
- Chipcount: 2 Quad buffers (=2 IC)

original ALICE FEC and ILC FEC2



ILC FEC 2.1



ILC FEC v2.1 vref

- One common reference voltage, variable by voltage divider
- All references on ALTRO separate, routed separately to buffers
  Connected to reference voltage through 0 Ohm jumpers
- Can be fed individually by desoldering jumper and connecting to external source – only intended for tests (not production!)
- Chipcount: 4 Quad buffers (=4 IC)

ILC FEC v2.2 vref (proposal 1)

- Keep all ALTRO references separate at ALTRO as in v2.1
- Feed buffers with reference source fed through 12-bit DAC,
  one DAC per ALTRO reference pin= 3 in total
- Control DAC from Altera FPGA -
  space for control logic exists
- Chipcount: 1 Quad DAC, 6 Quad buffers = 7 IC

ILC FEC 2.2 - alternative 1