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JRA3 Electromagnetic Calorimeter Technical Design Report

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Abstract

This note describes the design of the prototype for an Silicon Tungsten electromagnetic calorimeter with unprecedented high granularity to be operated in a detector at the International Linear Collider (ILC). The R&D for the prototype is co-funded by the European Union in the FP6 framework within the so called EUDET project in the years 2006-2010. The dimensions of the prototype are similar to those envisaged for the final detector.

Already at this stage the prototype features a highly compact design. The active and passive parts as well as the readout electronics are fully integrated within 2000 μm.

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1 INTRODUCTION

The next major worldwide project in high energy particle physics will be a linear electron positron collider at the TEV scale. This machine will complement and extend the scientific results of the LHC currently operated at CERN. The most advanced proposal for the LC is the International Linear Collider (ILC). Here, electron and positrons will be collided at centre-of-mass energies between 0.2 and 1 TeV. The detectors which will be installed around the interaction point are required to achieve a jet energy resolution of $30\%/\sqrt{E}$, thus a factor two better than the energy resolution achieved at LEP, the predecessor which has been operated at CERN between the years 1988 and 2000. The reconstruction of the final state of the e^+e^- will be based on so-called particle flow algorithms (PFA). The goal is to reconstruct every single particle of the final state which in turn demands a perfect association of the signals in the tracking systems with those in the calorimeters. As a consequence this requires a perfect tracking of the particle trajectories even in the calorimeters. For an optimal Particle Flow the calorimeters will have to be placed inside the magnetic coil of the detector which puts tight constraints on the space available for the installation of the detectors.
To meet these requirements the detectors have to cover the whole solid angle and have to feature an unprecedented high granularity. The design of the sub components of the detectors and in particular of the calorimeters have thus to follow two main guidelines:

- The number of readout channels has to be driven to an unprecedented amount ;
- The calorimeters have to be extremely compact. This concerns both the choice of the absorber material and the integration of infrastructural components such as cooling, power supply, readout lines and front end electronics.

For the electromagnetic calorimeter which surrounds the tracking system the two guidelines above lead to the choice of Tungsten with a radiation length X_0=3.5 mm, Moliere radius R_M =9 mm and Interaction length λ_I=96mm as absorber material and Silicon as the active material. The CALICE collaboration is performing a large R&D program for the development of highly granular calorimeters. A physics prototype with a pixel size of $1cm^2$ dedicated mainly to demonstrate the physics potential of a calorimeter fulfilling the requirements above but also to validate the main mechanical concepts has been constructed and is currently examined in test beam measurements at DESY, CERN and FNAL [1].
The design of the (next) prototype for a Silicon Tungsten (SiW) electromagnetic calorimeter as described in this note, called EUDET Module hereafter, takes the two guidelines into account with the emphasize on the understanding and overcoming of the engineering challenges imposed by the requirements of the overall design of the ILC detector as described in [2]. The main parameters of this module are:

- A pixel size of 5.5x5.5 mm^2 ;
- A total depth of 24 X_0 ;
- The thickness of an individual layer of 3.4 mm and 5.4 mm.

The construction of the final Module will be preceded by the construction of a so-called demonstrator with slightly different dimensions and simplified electronics. The demonstrator will allow for the study of all mechanical aspects of the final module and constitutes therefore an important step towards the EUDET Module.
The EUDET Module will be exposed to test beams starting in 2010. Here, for the first time prototypes with a layout realistic for an ILC detector will be qualified. The results will compare to those obtained with a so called physics prototype. At the same time the test beam

results will allow for a realistic estimation of the precision, which can be expected from an electromagnetic calorimeter at the ILC as well as insight into the operability of such a device during the experimentation at the ILC.

2 OVERALL DESIGN

This technological prototype should be the most representative of the final detector module too. The schematic 3D view of the prototype, in Figure 2.1, shows the current design of the alveolar structure, with 3 columns of alveoli to have representative cells in the middle of the structure. This prototype should have identical global dimensions (1.5m long) and shape (trapezoidal) and include the fastening system with the HCAL (included in the design of composite structure). It has the following sampling: at normal incidence, 22.8 X_0 are filled with 20 layers of 0.6X_0 (2.1mm) thick tungsten absorber plates, followed by 9 layers of 1.2 X_0 (4.2mm) thick plates, with an overall thickness of 198.5 mm. Each detector layer has an active area of 18 × 18 cm^2, segmented into readout cells of 5.5 × 5.5 mm^2. The active zone is hence made by 30 layers of 2 × 2 matrices, each consisting of 16 × 16 pixels, giving in total around 38000 channels.

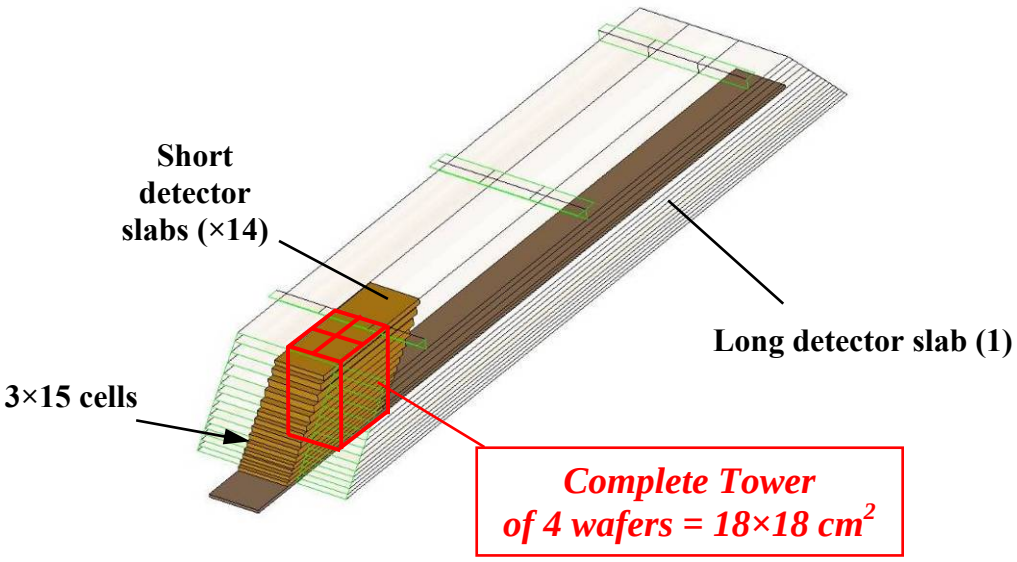


Figure 2.1 – schematic 3D view of the prototype

The design and construction of the prototype presents a number of engineering challenges. A particular innovative effort is proposed to reduce the dead area whereby half of the tungsten is incorporated into alveolar composite structures (see Figure 2.2). This technology solution has of course an important impact, not only on the reduction of passive materials and dead zones, but also on the compactness of this instrument. The alveolar structure fabricated by moulding of preimpregnated carbon fibre and epoxy ("prepreg") onto tungsten sheets, leaving free spaces between two layers to insert 1 long and 14 short detection units, called detector slabs. One detector slab consists of two active readout layers put on each side of an H-shaped supporting structure (including tungsten absorbers too), and shielded on both sides by an aluminium or copper foil 0.1mm thick, to protect from electromagnetic noise and provide the wafer substrate ground.

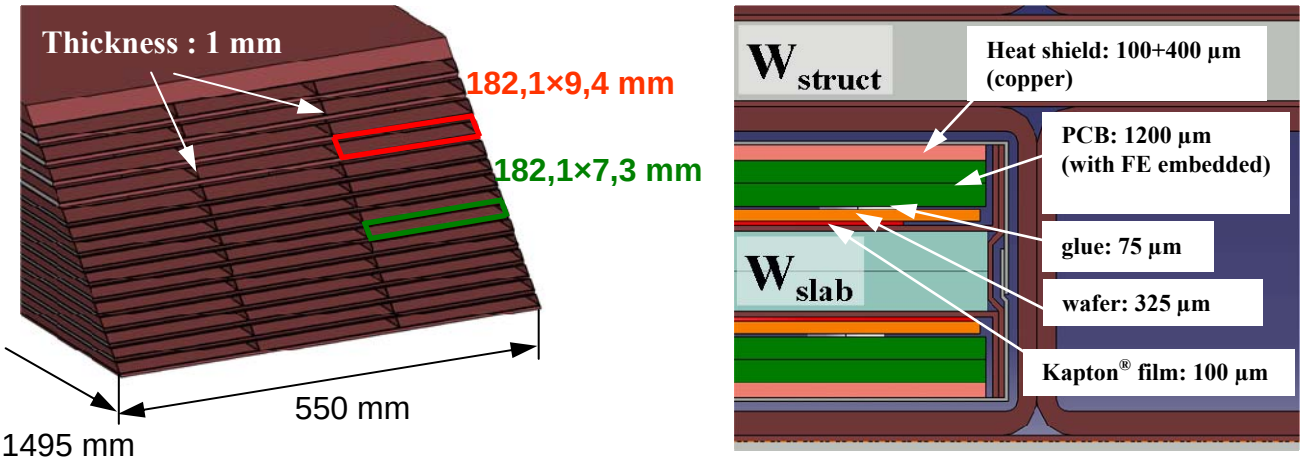


Figure 2.2 – Main dimensions of alveolar structure and slab

3 STRUCTURES AND MOULDS

All the composite parts, i.e. alveolar structure, long and short H-shaped have been made using the same carbon fibre and epoxy prepreg, TEXIPREGR CC120 ET443 [3], with an average thickness of 0.15mm. The first option to mould the alveolar structure was to obtain the final object with just one curing step. This "one bloc" process allows having a better mechanical ability of the structure but the design and the development of the global mould was more complex and expensive: this solution imposed to have the same number of cores and cells (45 cores), and finally the weigh of this metal mould imposed important curing problems due to thermal inertia and there were also important risks to fail one structure. A method of an "assembled structure" has been preferred: each alveolar layer (3 horizontal cells) are done independently, cut to the right length (with 45°) and assembled alternately with tungsten layers in a second curing step. This solution allows doing an individual inspection and choice of each layer before the final assembly, and also limiting risks to lose tungsten plates. This principle reduces also the cost of the industrial process: simpler moulds (one "alveolar layer" mould + one "assembly" mould) and the final piece is obtained in 2 simple polymerization process, limiting curing problems, weight of metal mould. Concerning, the H structure mould, we kept the same concept used for the physics prototype and it will be described next.

3.1 THE "ALVEOLAR LAYER" MOULD

This mould (Figure 3.1) is used to build the "alveolar layers" parts. It consists of 3 metal cores (steel), and some pieces machined in HEXTOOL [4] material. This proposal for composite moulds is an alternative to conventional composite tools and metal moulds, especially INVAR moulds. The main advantages of this new material are:

- The ability to make large tools with complex and tight tolerances ;
- A lighter weight compared to similar metal tooling, for easier handling and minimizing infrastructure investment ;
- A faster heat up and cool down than metal moulds ;
- Some machinable surfaces without distortions and an easily repairable ;
- A coefficient of thermal expansion to match carbon epoxy parts.

Since the thermal expansion coefficient of carbon fibres is very close to the hextool mould, distortions during the curing are small.

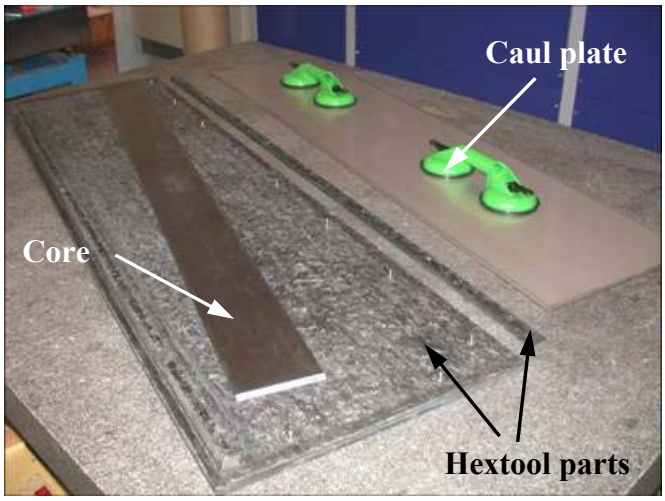


Figure 3.1 – "alveolar layer" mould (demonstrator)

Each metal core forms each alveoli. They are wrapped with 4 layers of composite. We use the differential expansion between steel and Hextool to compact all plies of reinforcement in transverse direction. A stainless steel caul plate is used in contact with the top composite surface to transmit normal pressure and temperature during cure. After curing, the cores are taken out, leaving empty spaces for the detector slabs. The thin composite sheets located between two cells consist of 8 composite plies, and are 1mm thick. Dimension and geometry tolerances of the structure are directly dependent on the machining of the mould: all cores were ground with a resulting flatness of ±0.05mm to be able to extract them correctly.
The first alveolar layer structure has been produced (Figure 3.2) with success where the main issue was solve correctly (long and thin structure). By this sample, this first "alveolar layer" mould is validated and we will focus on the design of the assembly mould now.

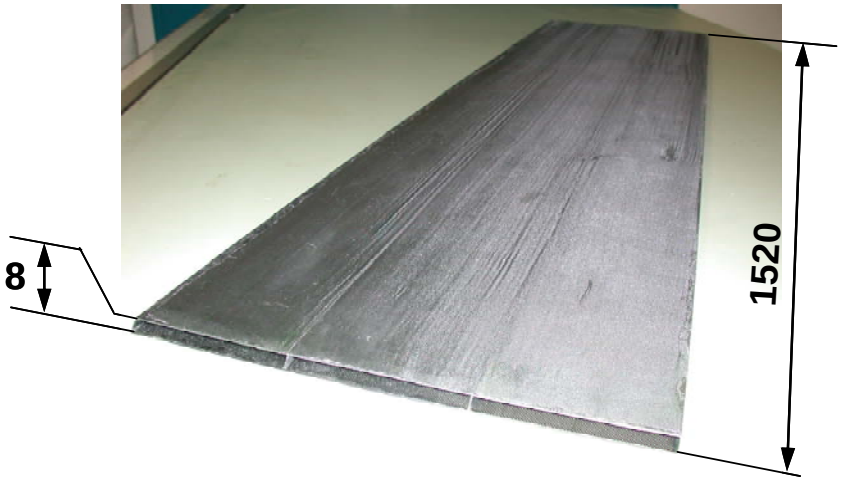


Figure 3.2 – First "alveolar layer" structure

3.2 THE ASSEMBLY MOULD

The design of this second mould has started. We choose to use a structural bonding technique. However several issues have still to be studied and solutions will depend on the mechanical characterisation of the thin inter alveolar sheets. We plan to bond alternatively all tungsten, alveolar and composite layers by using structural adhesive film. In this principle, we need to define one compacting pressure, generated by the autoclave, according

to the compressive behaviour of the thin composite sheet [7]. The gluing has to be done without damaging of these important parts, which will carry the main fraction of the mechanical load.

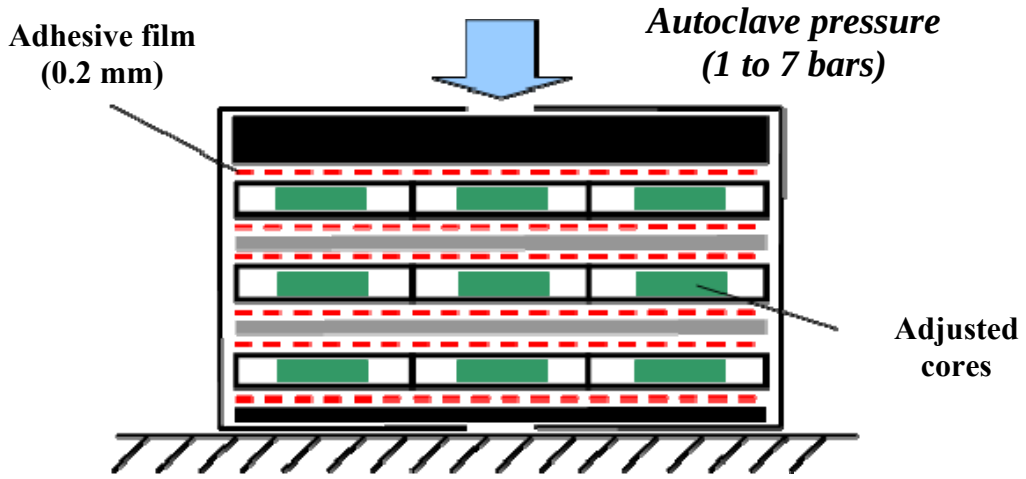


Figure 3.3 – Principle of assembly mould

During the assembly a good mechanical contact between the thin alveolar walls and the tungsten plates has to be ensured. Several solutions are under study as for example applying pressure onto each cell by employing hermetic pressurised bags or by inserting small adjusted aluminium pieces into each cell as depicted in Figure 3.3 (green parts).

Cutting tests:

Before assembling the final structure, we need to cut at 45° each alveolar layer structure in order to have the trapezoidal shape. The length of each structure is different and depends on its localisation in the final structure. Several cutting options will be tested. The first one is machining the extremity of each layer with a tool adapted for composite. The Figure 3.4 shows a conclusive test.

Figure 3.4 – First cutting test

3.3 THE H STRUCTURE MOULD

The H-shaped structure consists of several tungsten plates core wrapped with a “H” structure made from Carbon fibres. The silicon layers are attached on each side of the "H", one on the top, one on the bottom. This H structure is also the only mechanical support of the slab.
The design of its mould is done. We plan to use the same and unique mould to produce all long and short structures (180mm wide). We kept the same principle than the mould used for building the physic prototype. We just adapted it to an autoclave application. This mould would serve to obtain H structure of the demonstrator (124mm wide) too with the intention of validate the fabrication process.

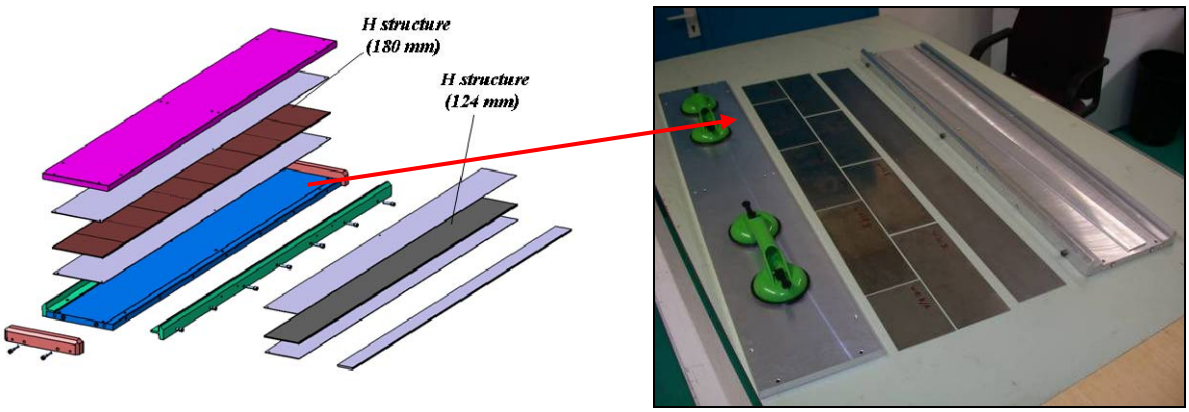


Figure 3.5 – Exploded view of the H structure mould

Figure 3.5 shows the exploded view of this mould with all components and all W plates that we need for the first test. We decided to obtain the long absorber by gluing 2 layers of shorter W plates compared to one long and unique solution (difficulty to provide long W plates with good flatness and thickness tolerances).
The first H structure has been produced (Figure 3.6) with success too. This concept of the long H structure is validated.

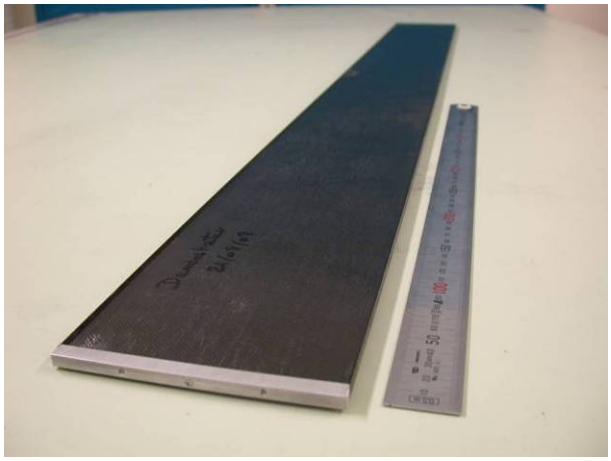


Figure 3.6 – First long H-shaped structure

4 SILICON WAFERS

4.1 DESCRIPTION

Silicon sensors were chosen as the best compromise, despite their potentially high cost, between granularity and integration capability. A particular attention has been taken to the overall cost of the sensors with a large impact on the design requiring the study of new structures of the sensors. Extrapolating to the future evolution of the detector to be a candidate for the ILC, the cost has to be scaled to a production of approximately 3000m^2 of silicon sensors. The manufacturing costs can be controlled minimizing the number of production steps to typically 4 or 5. This constraint prevents most of the commonly used techniques to provide a secured design of the structures against current leakage. Nevertheless an R&D effort was made to overcome this particular aspect and to develop efficient sensors.

The detection process is based on electrons-holes pairs generation in high resistivity silicon (5 kΩ.cm) from the successive products of the electromagnetic shower. A matrix of PIN diodes is burned onto raw silicon wafers using standard manufacturing processes from the industry of microelectronics like acceptor/donator ions implantation, oxide growth or metal deposit. The size of one square PIN diode can be at the order of a few millimetres as required by the simulation of the physics performance of the detector. Nevertheless the integration of the electronic read-out was regarded to be seen as critical according to the requirements of the detector mechanics. It limits the actual granularity to diodes of about 5mm large. The sensor thickness is constrained by the availability of commercial raw wafers and the signal dynamics: about 300 µm complies with the read-out electronics.

The diodes matrix is surrounded by a so called “guard ring” structure which is made thanks to the same processing steps. Other well known techniques like etching, MOS effect or polarization of the guard-rings require additional steps and would have increased the overall cost. Consequently the guard rings are left floating and are therefore not connected to any mechanical or electronic component. This is a novelty and the reference design is not yet finalized.

The silicon wafer can be simply glued to printed circuit boards. From the point of view of the sensors, no other particular technique is needed for their integration which then uses widely available commercial products.

4.2 CURRENT STATUS

4.2.1 Manufacturing and process

The test beam data taking at CERN, DESY and FNAL with the physics prototype helped to gain experience in operating silicon wafers for calorimetric purposes and to study details of the performance of the wafers. These wafers have 6 cm^2 in their lateral dimension with a pixel size of 1cm^2 and an overall thickness of 500 µm. A complete description and a report on the work done on these sensors can be found in [1].

When exposed to high energetic particle beams a crosstalk between the floating guard-ring and the bordering pixels became apparent. It is mandatory to suppress this effect or to reduce it by at least two orders of magnitude to fully achieve the expected behaviour. This observation has motivated mainly two investigations:

- Simulation and study of the effect to propose an alternate and new design of the guard-ring structure (see section above) ;

- Ordering of sensors from Hamamatsu supposed not to exhibit the crosstalk coupling. The Hamamatsu sensors (Figure 4.1) have new dimensions fitting the EUDET requirements: 330 µm thick and 0.25 cm^2 diodes on a 90×90 mm^2 surface.

The whole design has been scaled to this new size (mechanical support, number of read-out channels) and a batch of prototype was received on April 2008 from Hamamatsu.

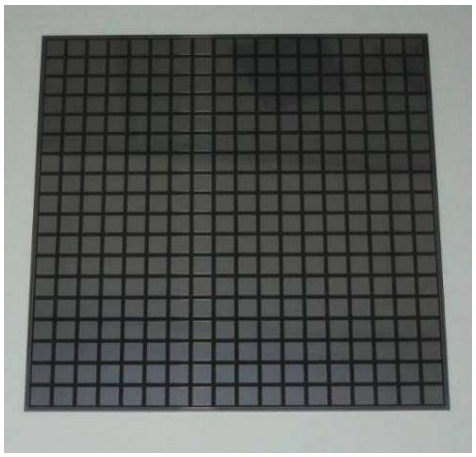


Figure 4.1- Picture of the Hamamatsu prototype

4.2.2 Reception tests of Hamamatsu sensors

Straight upon reception the sensors have been subject to a validation process:

- The overall current with respect to the bias voltage gives the breakdown voltage and the quality of the protection structures against leakages. The breakdown voltage has been found to be above 500V to be compared to the operation voltage of 500V ;
- The capacitance as a function of the bias voltage shows the doping profile and the quality of the depletion (minor variation according to the bias voltage). The sensors are used polarized above the full depletion voltage. A special care concerning the variations of the capacitance according to the bias voltage which may be responsible for electronics noise has been taken.

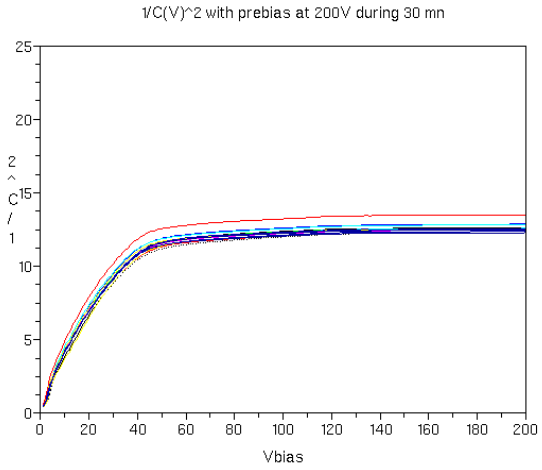


Fig 4.2 - Example of $C(V)^{-2}$ characteristic

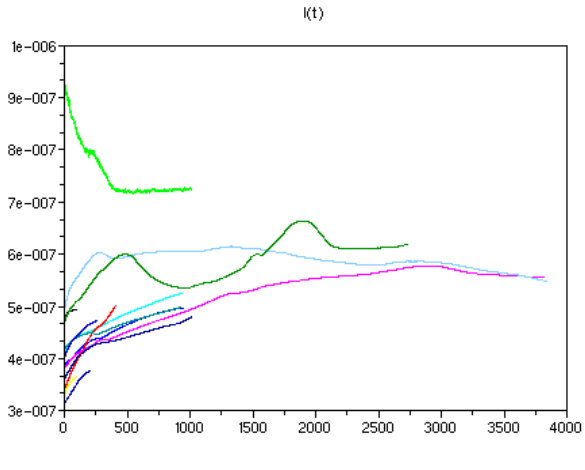


Figure 4.3 - Example of I(t) measurement for several sensors.

During regular beam operation the wafers will be fully depleted i.e. operated in the flat part of Figure 4.2. The depletion curve of an individual wafer seems to evolve with the time while the bias voltage is applied. This effect can be reproduced with simulations and understood as follows:

- The current as a function of the time allows checking the proper behaviour of the sensor particularly when glued (Figure 4.3) ;
- An attenuated crosstalk effect has been observed on the Hamamatsu sensors despite the expectation. A factor 10 of additional attenuation would be required. The corresponding studies are limited by industrial property rights owned by Hamamatsu.

Effects of temperature and humidity are also checked but no clear impact was found.
An interaction between the glue and sensors has been discovered for the physics prototype for sensors produced by one of the two manufacturers. Therefore long term tests are being performed with the sample purchased from Hamamatsu. Once glued, the current leakage is increased by a factor 10 but start to decrease after being biased for a few hours. The criticality of the current leakage with respect to the electronics has to be checked.

4.2.3 Integration

From the point of view of the sensors, the integration of the detector requires the following studies:

- Gluing technique and its automation to deposit up to 256 glue dots minimizing the glue thickness ;
- Tolerance of temperature elevation during the assembly of a detection module (SLAB) ;
- Bias voltage distribution allowing the replacement of failing detector units.

These points are discussed in details in Chapter 8.

4.2.4 Simulations

Measurement results (Figure 4.4) have been compared with simulations (Figure 4.5) at silicon level (finite elements method) in order to better understand the behaviour of the wafer.

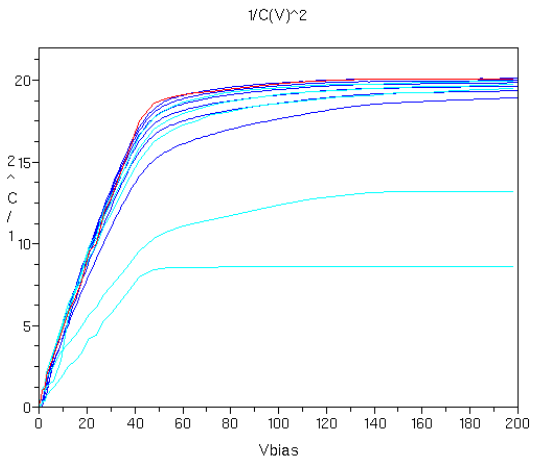


Figure 4.4 - Measurement (dark blue) and simulation (light blue) comparison according to trapped charges at the sensor surface. A simulation model (red) is obtained from the mix of two components of the $C(V)^{-2}$ response.

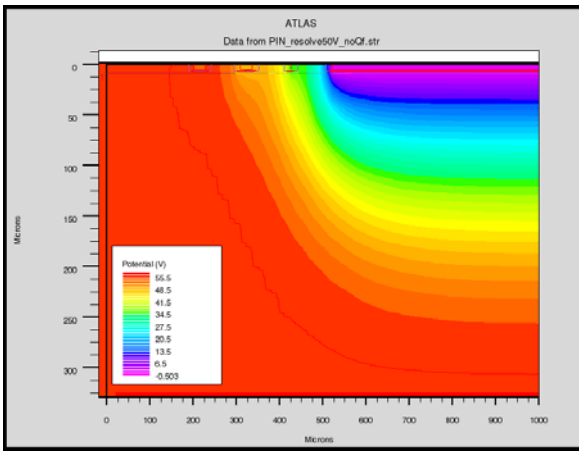


Figure 4.5 - Simulation of the electrical potential, helping to evaluate the components of capacitive couplings of the sensor. One pixel a 3 guard rings are shown.

According to the simulations, the time dependency of the bias voltage curve can be explained by trapped charges at the surface. Discussions with Hamamatsu are ongoing in order to find a remedy.

4.2.5 Conclusions about design

The very first tests of 30 Hamamatsu sensors are encouraging. Static tests validate the design: the breakdown voltage is far away from the bias point and C(V) characteristics are as expected and well understood by simulation. Nevertheless these sensors seem to need to be biased about 1 hour prior usage since their characteristics are evolving in a time dependent but converging way.
On previous versions of the sensors from other manufacturers, the constraints on the overall cost impose a manufacturing process which leads to implement floating guard-rings. It leaves crosstalk couplings to appear within the wafer and evidence of crosstalk has been found during the tests. Specific studies of this phenomenon are ongoing (see next paragraph) in order to avoid the dependency only one manufacturer (Hamamatsu).
Recent prototypes of sensors from Hamamatsu validate the principle of the new size with 330 µm thick silicon. The yield of accepted wafers after static test reaches 100% allowing the cost of this technology to be close to the other manufacturers.
Studies are ongoing to solve the crosstalk effect, check every integration constraints and to find out a final candidate for the EUDET detector.

4.3 ON GOING STUDIES ON INTERNAL CROSSTALK

On previous prototypes, data from particle beam clearly show some square patterns in a small fraction of measured events when the incoming particle hit the guard-ring.

4.3.1 Modeling

Several kinds of modelling or simulations were investigated to understand the crosstalk effect:

- Numerical simulations at silicon level used to fit the parameters of the other simulations or models ;
- Simulation at an electrical level to evaluate the crosstalk levels ;
- Hardware models made from small printed circuit boards and a measurement bench to test new guard-ring layout ;
- An analytic model of the measurement bench.

Simulations and models show that the crosstalk can come from an unexpected signal to be propagated all along the guard-rings generating a non zero response in the nearest detection cells thus creating the square shape.

4.3.2 New innovative design

The idea to literally cut the guard-ring into small segments was proposed to avoid the propagation along the guard-ring. Simulation, models and measurements on printed circuit hardware models have shown the segmented guard-rings could avoid the crosstalk. The use of segmented guard-rings (Figure 4.6) is a challenge as the risk of current leakage could dramatically increase preventing the use of the sensors due to unprotected paths for the

current. This innovative layout of the guard-ring has the advantage to require no additional manufacturing steps. Thus it does not increase the cost.

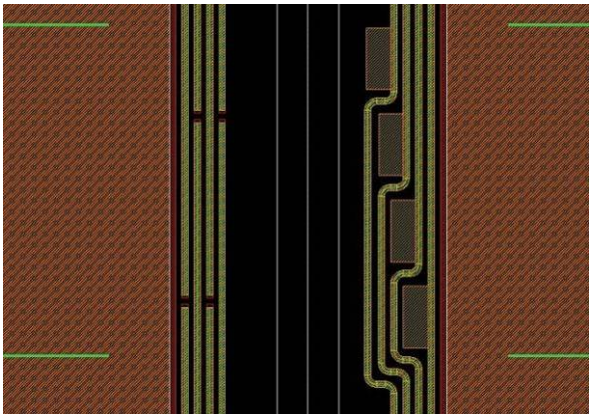


Figure 4.6 - Layout (CAD view) of segmented guard ring and pads for testing

4.3.3 Test bench

A measurement bench (Figure 4.7 and 4.8) allows to inject a stimulus and to measure the crosstalk signal thanks to micropositionners and tungsten needles (probe heads).

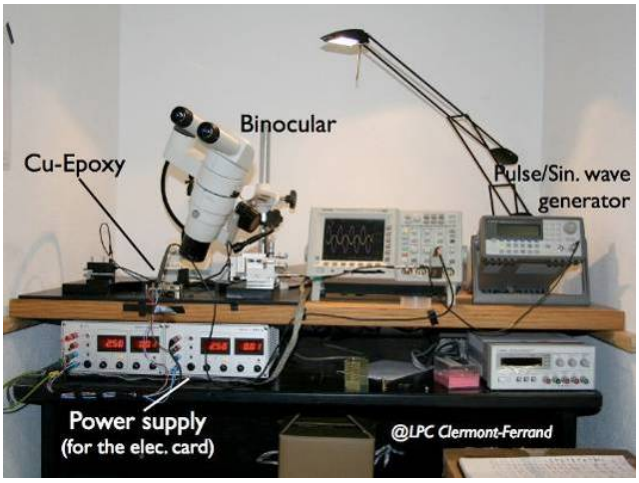


Figure 4.7 - Overall view of the testbench.

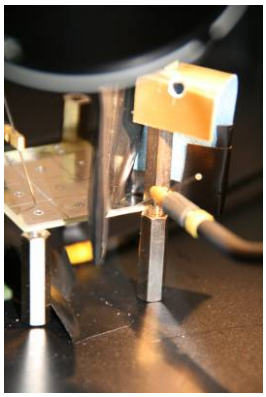


Figure 4.8 - Zoom on the test area equipped with probes mounted on precision 3D positionners.

First measurements have been performed on fake sensors made of small printed circuit boards with several guard ring patterns [6]. The principle of segmented guard rings prior has been validated to measure real sensors.

4.4 FUTURE ACTIONS AND PROSPECTS

At a short term, two paths are explored:

- The manufacturing of real sensors with segmented guard-rings. The sensors are layout and should come back from OnSemi (Czech) and BARC (India). These sensors will be tested using the test facilities shown above (developed at LPC, IN2P3, Clermont-Ferrand, FRANCE) ;

- The final investigations on Hamamatsu sensors, in particular about the tolerance of the glue and the crosstalk effect using a laser or a particle beam.

At mid term, other layout techniques and the possibility to bind the guard-rings to a reference voltage will be checked. In the meantime the Hamamatsu sensors can be used to demonstrate the feasibility of the EUDET prototype as soon as their tolerance to the glue is checked. Solving the crosstalk effect is required both for physics performance and to avoid the dependency in a single manufacturer. For this last point, a simple layout and a well known manufacturing process should be used. This justifies the studies described above.

5 SKIROC CHIP

5.1 SKIROC DESCRIPTION

SKIROC is the name of the front-end ASIC designed to read out the Si-W technological prototype. It is the acronym for "Silicon Kalorimeter Integrated Read Out Chip".
The final front end chip designed for the EUDET Module is to embed 64 channels of front end electronics. Four chips will be necessary to read out each 256-channel silicon wafer. The design of this chip takes the time structure of the tentative ILC beam into account. Hence, in order to reduce the power consumption by two orders of magnitude, the front-end chip has to be switched off during the 199ms between two bunch trains of 1ms each. The starting up of the chip is a crucial point because it is necessary to reach a 15 bit resolution and stability within a very short settling time in order to not to compromise the calorimetric measurement.

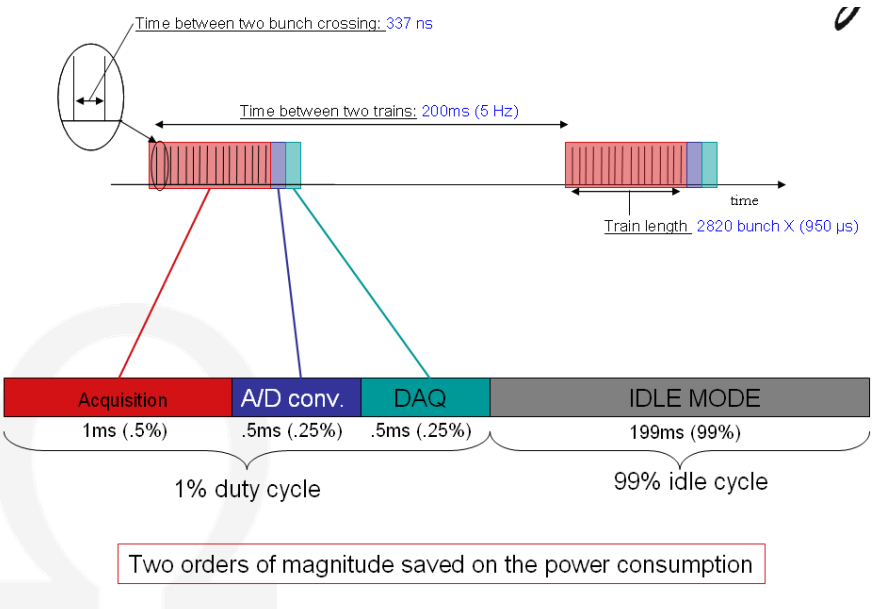


Figure 5.1 - ASIC behaviour versus Beam structure

The requirements on the electronics to meet the EUDET Module specifications are the following:

- Designed for 5.5×5.5 mm² pads ;
- 64 channels ;
- Detector DC coupled ;
- Auto-trigger ;
    - MIP/noise ratio on trigger channel : 16

- 2 gains / 12 bit ADC → 2000 MIP ;
  - MIP/noise ratio on charge measurement : 11
- Power pulsing ;
  - Programmable stage by stage for technological study
  - Fast start up (<50µs) with 15 bit resolution
- Calibration injection capacitance to perform electrical calibration ;
- Embedded band gap for references stable with temperature and supply voltage ;
- Embedded decoupling capacitance and bias devices ;
- Embedded DAC for trig threshold ;
- Compatible with the DAQ of the physics prototype for cross checks ;
  - Serial analogue output
  - External "force trigger"
- Probe bus for debug ;
- 24 bits Bunch Crossing ID ;
- SRAM with data formatting ;
- Output & control with daisy-chain compatible with other EUDET demonstrator detectors.

All these features render SKIROC to be a complex device which will be able to operate autonomously in the three main modes required by the beam structure: Acquisition, A/D conversion, DAQ read-out. A complex digital machine drives the different functionality of SKIROC.

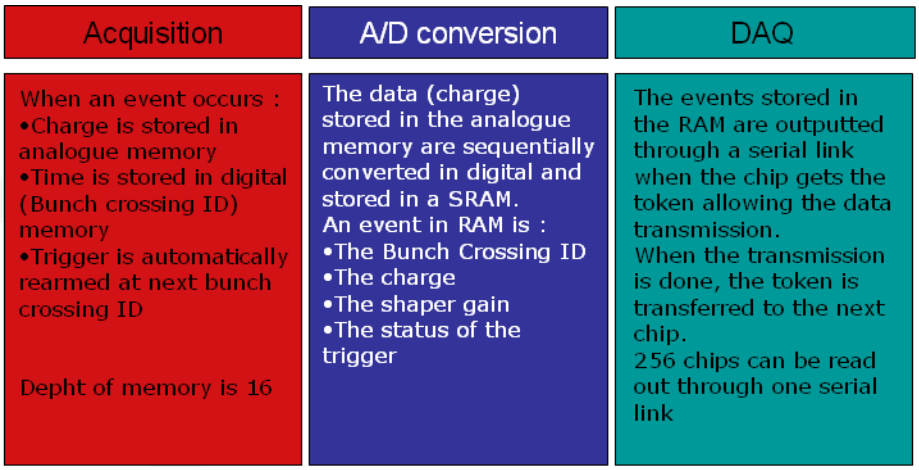


Figure 5.2 - SKIROC mode description

The digital part drives the whole system on chip. Several modes (see Figure 5.2) are available to ensure sequencing in the chip. During the acquisition mode, the digital starts the analogue core and drive the analogue memories and the trigger to memorize the data when signal occurs at the inputs of the chip. During the conversion mode, the values stored in the analogue memory are digitized using the multi-channel ADC. The data are stored in an internal RAM.
The DAQ mode allows the DAQ to output the data. A daisy chain allows a serial read out of 256 ASICs. The data transferred to the DAQ are composed as follow: Chip ID, Time measurement (Bunch crossing ID), charge measurement.
The ASIC is embedding an analogue core including a multi gain charge preamp followed by a dual gain shaper and an analogue memory. The chip is self triggered to achieve an efficient

and embedded zero suppression. Each channel includes a fast shaper followed by an adjustable-threshold discriminator. The chip trigger is fired when one or more channel fire during a bunch crossing.

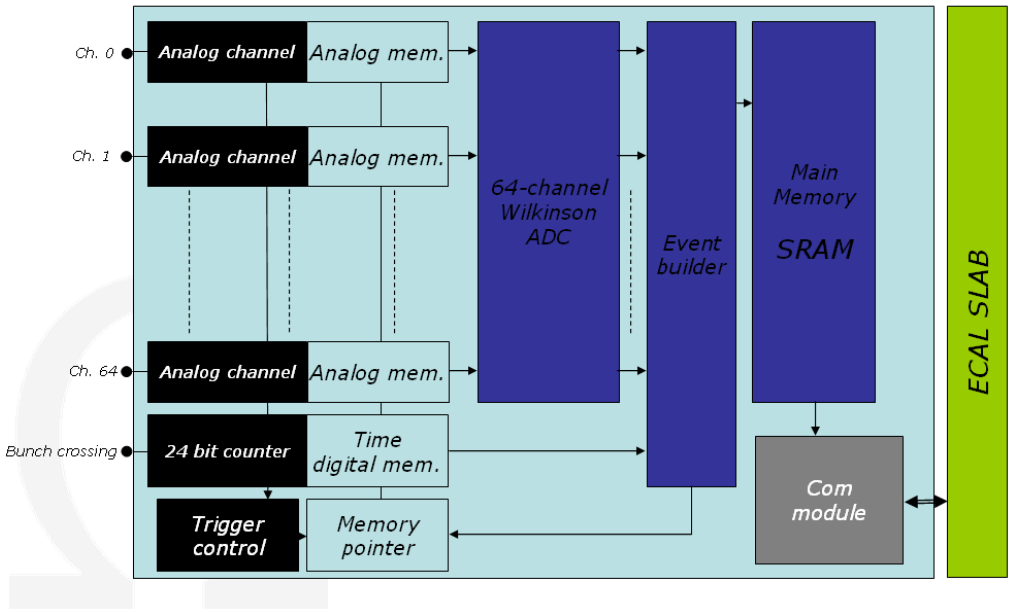


Figure 5.3 - Block scheme of SKIROC

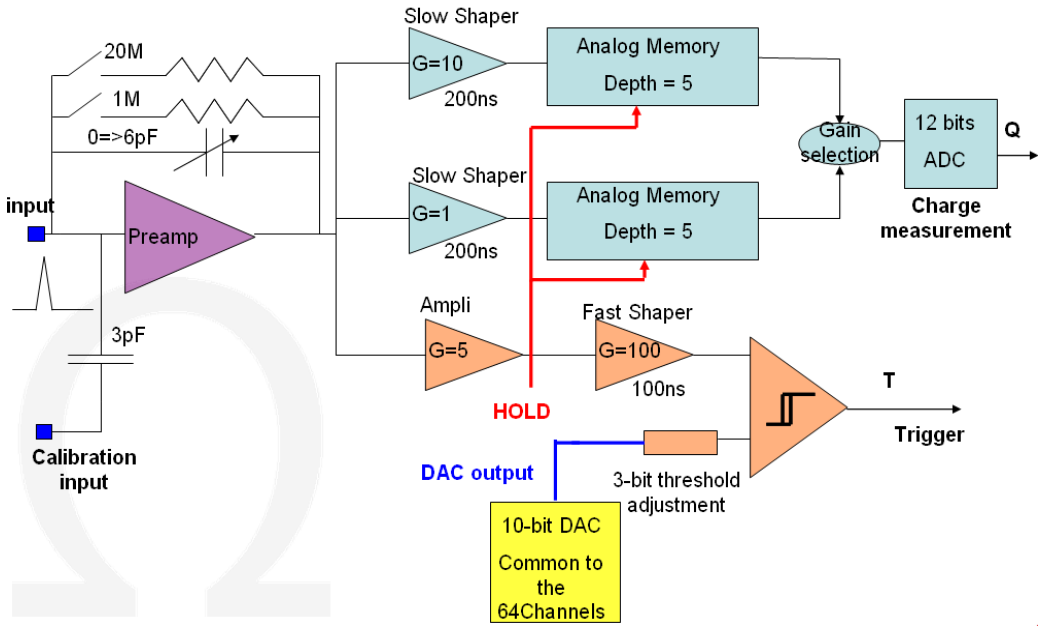


Figure 5.4 - One channel block scheme of Skiroc

5.2 SKIROC1 MEASUREMENT

Extensive measurement has been performed on SKIROC1, the first iteration of the SKIROC ASIC embedding only 36 channel for cost eduction. Results are presented in this section. A bug has been identified and will be corrected in next iteration foreseen for the end of 2008.

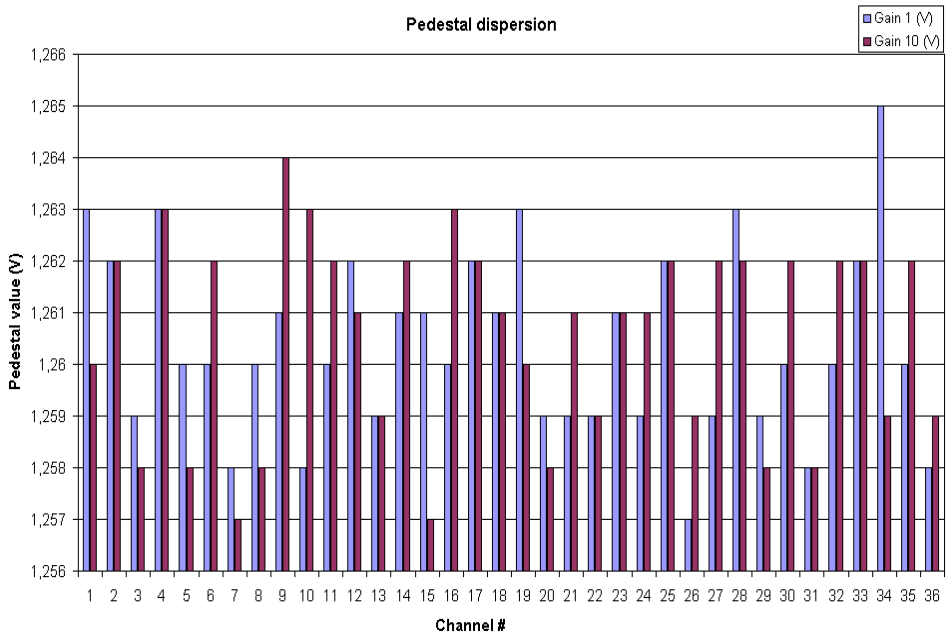


Figure 5.5 - Pedestal measurement on Gain 1 and Gain 10

Pedestal measurements do agree nicely with simulated results. Variations visible in Figure 5.5 are due to statistical dispersion in the transistor offset. The value of 1.8mV RMS is within specifications.

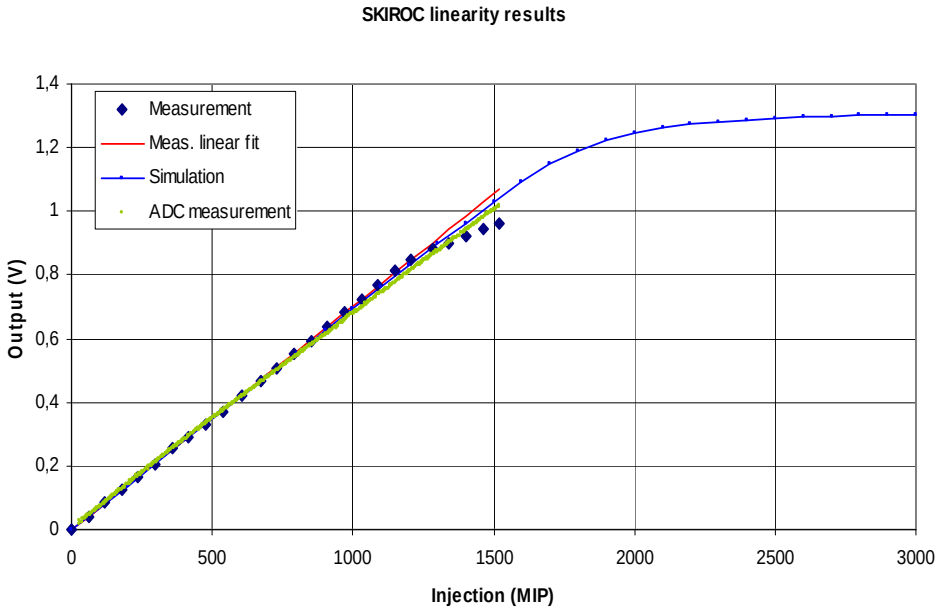


Figure 5.6 - Linearity measurement (analog and digital)

A minor bug in the ADC reduces the dynamic range by 25% and prevented the linearity characterisation over the whole expected dynamic range (Figure 5.6). Nevertheless, results on 75% of dynamic range are found to be within requirements.

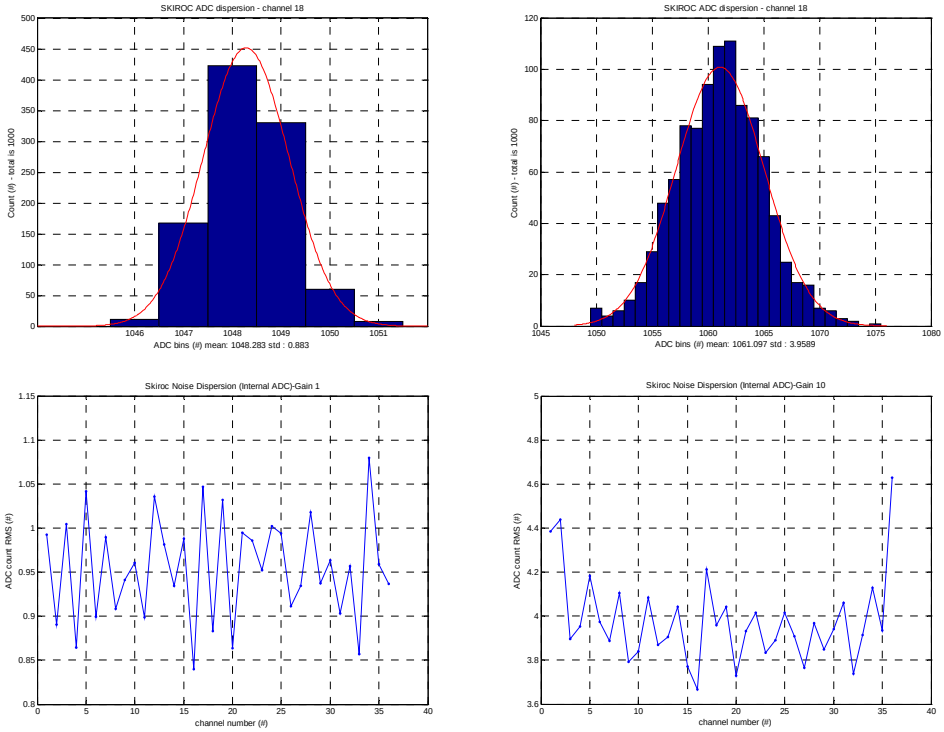


Figure 5.7 - Performance of a whole read out chain (preamp to ADC)

The noise and dispersion performances of the whole ASIC are as expected by the simulation. The 12 bit Wilkinson ADC does not add noise compared to the standard analogue read out.

5.3 SCHEDULE AND FURTHER PLAN

The production of SKIROC2 is planned by the end of 2008 to match the general EUDET schedule. The year 2009 will be dedicated to probe tests of SKIROC2 and its assembly on the front-end PCB described in the next chapter.

6 ACTIVE SENSORS UNIT (ASU)

6.1 PCB DESCRIPTION

The front-end PCB is the interface between the front-end electronics on one side and the detector on the other side. Each of these front-end PCB will carry 4 Wafers and 16 read-out chip. A first iteration to demonstrate the feasibility has been designed in 2008 and has underlined the challenge of building such a complex PCB for industry.
The first prototype carries only 8 ASICs thus a half of the detector channels (see Figure 6.1). It is a 8 layers PCB with NiAU surface treatment. The thickness of that PCB is 1.2mm envisaging 1mm as an ultimate goal

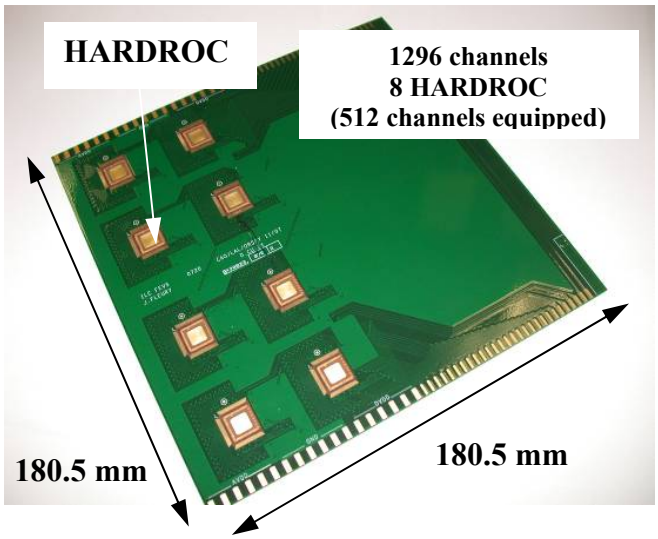


Figure 6.1 - FEV5 first prototype artist view

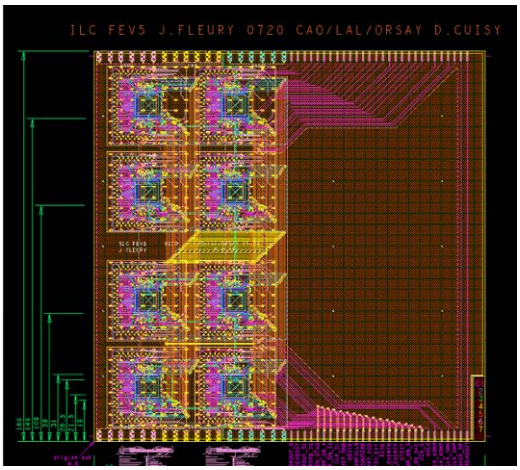


Figure 6.2 - Layout of the 8 layer PCB

To reduce the thickness of the readout electronics, the front-end ASIC is directly bonded in a groove foreseen in the PCB. A sketch showing all PCB layers is given in Figure 6.3.

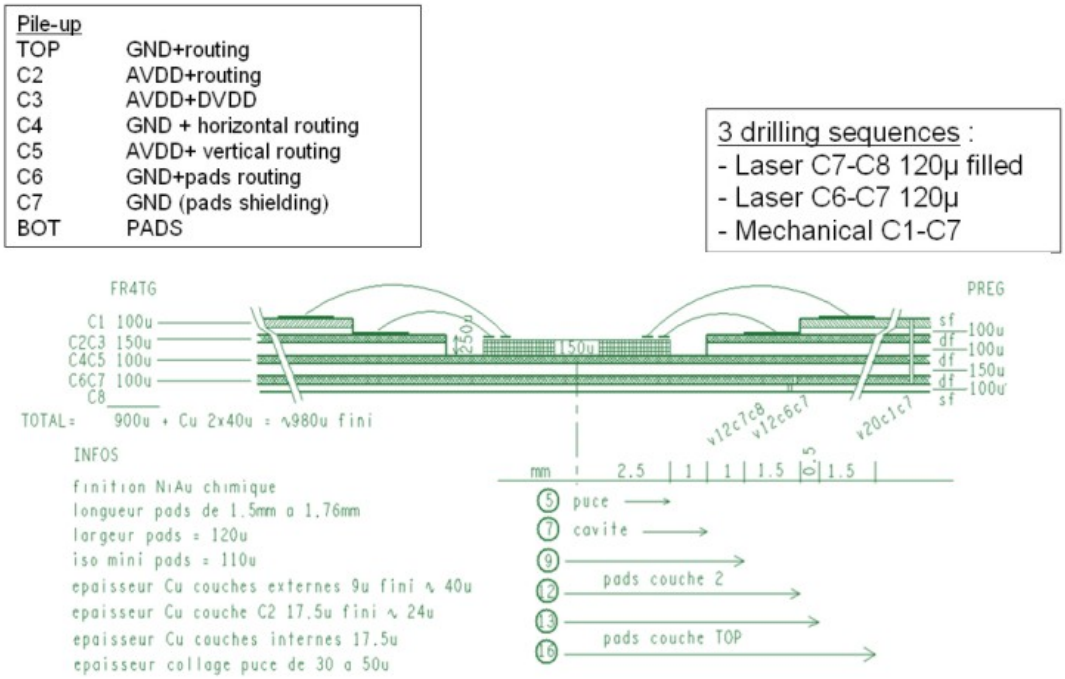


Figure 6.3 - PCB FEV5 pile up

The fabrication of these PCB in an industrial way is not yet proven and demands more investigation. The current prototypes are unfortunately not bondable due to the lack of copper and gold on Layer 2.
A task force is currently seeking to solve this crucial problem in order to be able to produce the PCB in 2009.

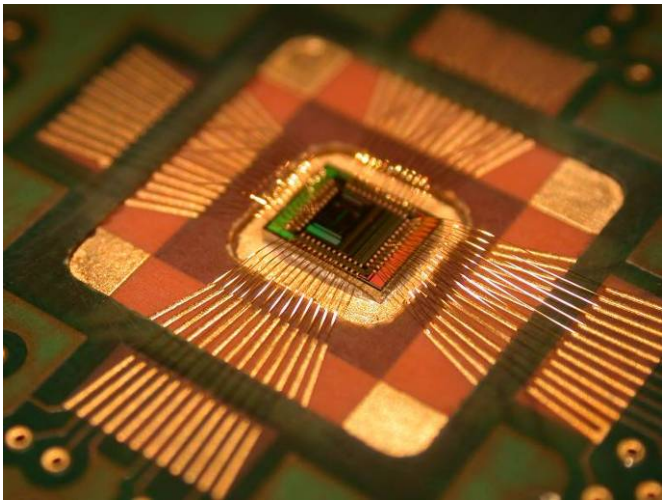


Figure 6.4 - Example of seccussful bonding in a test PCB

6.2 INTERCONNECTION

6.2.1 Outline Scheme

The primary function of the inter-ASU connections is to realise the electrical paths along the length of the slab:

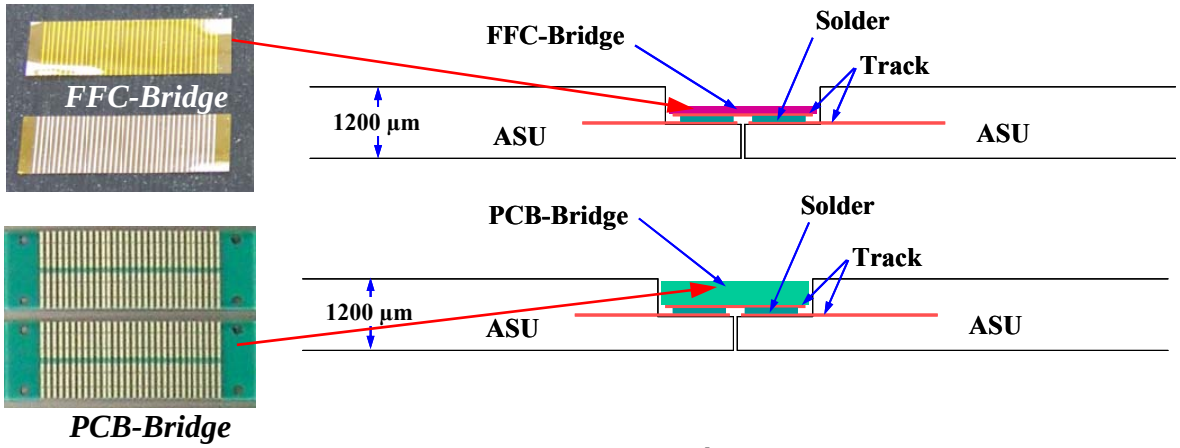
- Low voltage power ;
- Clocks and other fast control signals ;
- Slow controls via a serial path ;
- Data readout paths ;
- Various monitoring signals, notably temperature.
-

The interconnection must not jeopardise the quality of critical signals, especially the clocks. Redundancy options multiply the number of paths required. Also, given the longitudinal arrangement of the VFEs in 4 rows, it is attractive to provide a separate set of these signals for each row (this 4-lane solution greatly simplifies routing, reduces trace length and the number of vias, and avoids lengthy stubs on fast traces).
So a system that provides an adequate number of connections is needed. A strong mechanical connection is not a primary function: indeed the mechanical design might be considered over constrained if the connection were too rigid. It might usefully contribute to the thermal path along the slab. It should be capable of rework: removal of a faulty ASU, insertion of a new ASU, and its connection to its neighbours. This operation must be do-able without damaging the detector wafer or its conductive glue connections. And all this must be achieved within the ASU height restriction; this rules out the use of connectors.

6.2.2 Bridge scheme of interconnection

- The abutting edges of the ASUs are stepped to give vertical space for the connections
- Modularise into 4 groups of connections: this fits with the 4 sets of traces model ;
- Each group comprises a footprint of 30 pads on a 1mm pitch on the stepped edge ;
- A bridge piece with corresponding pads is soldered across the gap between the ASUs

- Two designs (see Figure 6.5) of bridge have been investigated: the rigid PCB-Bridge and the flexible FFC-Bridge ("FFC" stands for "Flat, Flexible Cable"). They have the same footprint: they are about 33mm long by 7mm wide ;
- The PCB-Bridge is 400µm thick, and is made of FR4 laminate ;
- The FFC-Bridge is only about 40µm thick, and comprises tin-plated copper conductors bonded to polyimide film.



igure 6.5 – Interconnection design

6.2.2.1 IR soldering procedure and investigations

This reflow task must give a quality joint without damaging the detector or the connections to its pads, which are currently implemented using conductive adhesive. It must fit into the slab assembly process as described in Chapter 10. It must also be shown to be capable of being scaled to the production of the final ECAL.
An infra red heater was designed and manufactured using a 500W linear quartz-halogen lamp in a housing with an elliptical reflector and boro-silicate glass window. The lamp is about 118mm long, and also emits a lot of visible light.
The ASUs (or, in our investigations, two custom designed test-ASUs) are aligned, and the footprints solder pasted using a stencil.
The interconnect bridge is carefully placed over the joint (see Figure 6.6).

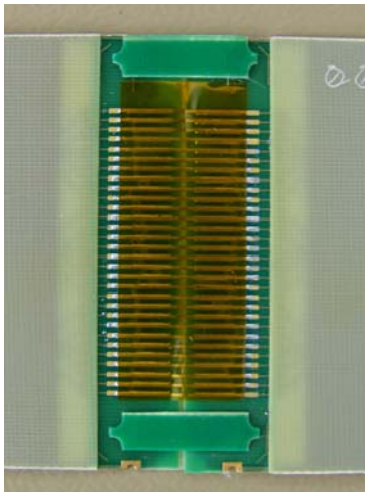


Figure 6.6 – View of FFC-Bridge joint

Usually some small pressure has to be applied to hold the bridge flat: typically this is done using a narrow glass plate.
The lamp is placed over the joint: its height is such as to give a somewhat de-focused image of the lamp that is broad enough to heat the full width of the bridge.
The lamp is turned on for long enough to get good reflow of the joint.
To date we have only used lead-free solder paste ($\theta_L \sim 220°C$), and this takes around 90s for a good bond. After initial profiling, joints have been consistently good for both types of bridge:

- Peel strength is excellent: the traces separate from the PCB or polyimide backing rather than breaking the solder joint ;
- No shorts ;
- Connection resistance less than 10mΩ.

6.2.2.2 Glue-Test investigations

We could now make a preliminary statement indicating that the glue joints survive the soldering process. But the conductive path needs "re-forming". Clearly we must convince ourselves that glue joints are going to work whatever interconnect method we use. We are also investigating the effect on the conductive glue joints: we have a Glue test PCB that has been attached to an aluminised 300μm glass plate (to mimic the detector) with an array of dots of the conductive glue. These were applied by the Manchester Group using the same adhesive and technique as proposed for detector assembly. The arrangement allows the resistance of the glue dots to be measured: the measurements will be repeated after the soldering operation. We will then try Tin-Lead ($\theta_L \sim 183°C$), and Tin-Bismuth ($\theta_L \sim 150°C$) solders to see any changes of the effect on the glue joints.

6.2.2.3 Laser soldering

We are grateful to the Soldat Group at the University of Hull for advice and trials on test pieces [7]. The advantage of laser soldering is the delivery of controlled heating exactly where it's needed – minimising the heating of neighbouring parts. Ad hoc tests at Hull have demonstrated the soldering of a few FFC pads to a test board using a semiconductor diode laser at 810nm delivering about 15W for around a second. More tests are planned to optimise the process, and to establish whether it could be used for the PCB-Bridges.
We also need to verify this doesn't damage the detector wafers or its bonds, and need to establish viable re-work procedures.
We are currently looking at OEM laser modules that cost around €3000 with a view to setting up a system at Cambridge.
It seems reasonable to assume we would need no more than 90s per bridge, so the technique should be practical for the construction of the EUDET Module which has some 176 bridges.
The process should scale for full detector production by duplicating the laser sources and simultaneously bonding 4 bridges across the slab and/or several ASU-ASU interconnections along the slab.

6.2.3 Signal Integrity studies

Two lines of investigation have been studied: one to look at data readout and clock distribution along a 1.68m emulated slab populated with a row of FPGAs. The other is a test of fast LVDS signals along differential traces using the bridge interconnection scheme.

6.2.3.1 Readout test

This uses 8-layer PCBs (ASU-Test0) of 240mm length (as originally planned for the ASUs) with a variety of traces. Interconnection uses a row of pads on opposite edges on a 2mm pitch bridged with individual fine wires soldered by hand. The FPGAs were programmed to produce pseudo random data that was readout using a token passing scheme combined with a readout clock. A common readout line was used with a supplementary line to indicate valid data: in fact the logic was copied from the HARDROC HCAL readout chip [8]. The slab was extended to 7 ASU-Test0 boards. The tests showed that such a single readout path could support data rates of up to around 2 or 3 Mb/s with very low bit error rate, but looked problematical much above those speeds.

6.2.3.2 Fast clock and control test

This uses 4-layer PCBs (ASU_Test2) of 170mm length. The boards are 400µm thick, but are packed out to 800µm over most of their length to give the step at the edges planned for the real ASUs. There are bridge footprints on the top of these exposed steps, and differential pairs of traces between ground planes (striplines) connect corresponding pairs of pins on the footprints at opposite edges. The inter-pair spacing is varied between different groups of these traces, allowing cross-coupling to be explored. Slabs made of 4 such boards interconnected with PCB- and FFC-Bridges have been well tested (see Figure 6.7). One of these slabs has now been extended to 10 such boards: a total length of 1.7m, and will be tested soon.

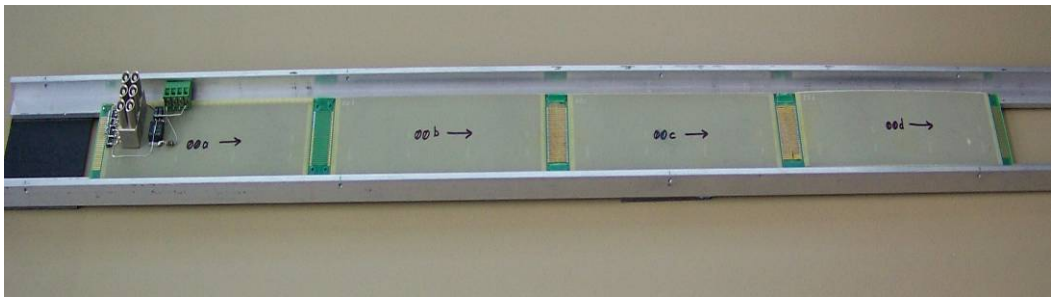


Figure 6.7 - Section Test Slab

A BusLVDS clock signal was used to drive the centre pair of a group of 5: this is the aggressor trace, and the neighbours are near- and far-victims. The driver is close to the board edge. All pairs (including the aggressor) are parallel terminated at the near end with 100Ω. The far ends of the tracks have 82Ω differential terminations. Fast differential scope probes were used to examine the signals at various points along the slab.
Work with the 4-section assembly has shown that:

- At 40 MHz clock can be sent along the board very cleanly ;
- Amplitude at far end is 77% of near-end value;
- Overshoot and ripple very small ;
- Minimal cross-talk if pair-pair spacing twice track plus gap distance ;
- Adding 10pF capacitors to pairs at ASU edges introduces noticeable degradation, but indicates that multi-drop loading will probably be all right.

Figure 6.8 - 40MHz clock at points along the slab

6.3 HV DISTRIBUTION FILM

The sensors are biased to a relatively high voltage comprised between 100 and 300 V. The reserved room for the bias voltage distribution is 100 µm thick only. A flexible PCB based on a polyimide substrate or similar could be a good candidate. It features conductive and insulator layers within the allowed thickness. Several designs are investigated with variations on the shape, the number of conductive layers and the gluing technique. A design with two conductive layers is preferred: it would provide build-in decoupling capacitance of the HV. In addition, the film and the way to glue it onto the ASUs should not prevent the disassembly of the SLAB.
Two major options are looked at:

- A single film covering the whole surface of the SLAB. In this case the gluing could be avoided but the quality of the contact relies on the pressure and the surface state of the conductive layer ;
- Individual film for each ASU designed in a "flag" shape (see Figure 6.9). A large square shaped end could be glued onto the ASU. It is prolonged with a ribbon up to a common HV connexion outside the SLAB.

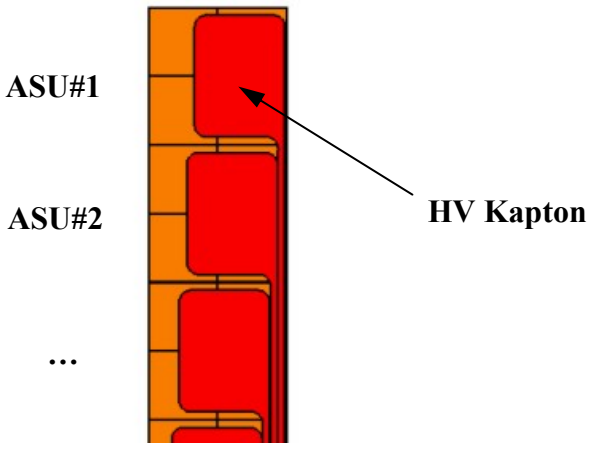


Figure 6.9 – HV kapton with "flag" shape

In both cases, the total length of the film is slightly higher than the SLAB length: 150 cm. Indeed, the connexion to the HV power supply is made at the DIF side of the SLAB.
The length is critical: it is largely beyond current industrial standards. A manufacturing process using raw materials in rolls have to be found and tested. Preliminary contacts have been initiated with some companies and prototypes are expected by the end of this year.

7 DIF CARD

7.1 INTRODUCTION

The DIF acronym (Detector InterFace) refers to the electronics located at the end of a detector slab. The DIF interfaces the Very Front End (VFE) chips embedded in the ASUs of a detector slab with the controls and readout systems, and services. Its main tasks are to:

- provide power to the ASUs, accommodating the fluctuations in the power requirements resulting from the sequential operation of the VFE chips ;
- provide clock and control signals to the VFE chips, and receive and buffer the event data ;
- provide an interface between the VFE chips and the data-acquisition (DAQ) system, for transporting data off detector, and receive and issue configuration data towards the VFE chips ;
- provide the interface of detector control systems (DCS) for monitoring purposes.

To isolate the requirements regarding the power provision from those regarding the DAQ interface, it was decided to introduce an Intermediate Board (IB) between the actual DIF and the end of the slab. The IB is supposed to connect directly to the slab and accommodate the power supply electronics and sensors associated with the DCS. The DIF connects to the IB by means of a high-density connector which is standardized across the Calorimeter sub-detectors.

7.2 DIF AND INTERMEDIATE BOARD FORM FACTOR AND LAYOUT

The DIF and IB are located at the end of the slab, where they have to fit in the tight space available for the detector services. Figure 7.1 depicts the available space for the DIF and IB in the plane of the slab. As the current prototype was designed for development of the DIF functionality, it slightly exceeds the allocated space. With a minor optimisation effort, a production DIF could be made to fit the designated space.

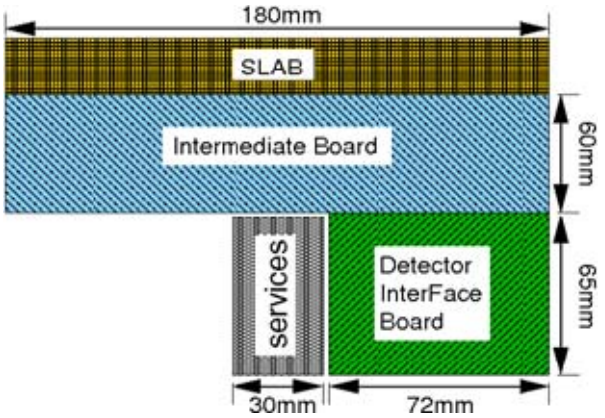


Figure 7.1 - Space allocations for the DIF and IB (top view)

The DIF is designed to cover less than half the width of the slab, to allow for an interleaved stacking of DIFs compatible with the slab pitch, as displayed in Figure 7.2. As the IB connects directly to the slab, it covers the full slab width. The IB PCB is assumed to have a thickness of 1.2mm, identical to that of the ASUs. Considering the modest functional requirements, the IB PCB and its components are assumed to fit within the allowed height budget.

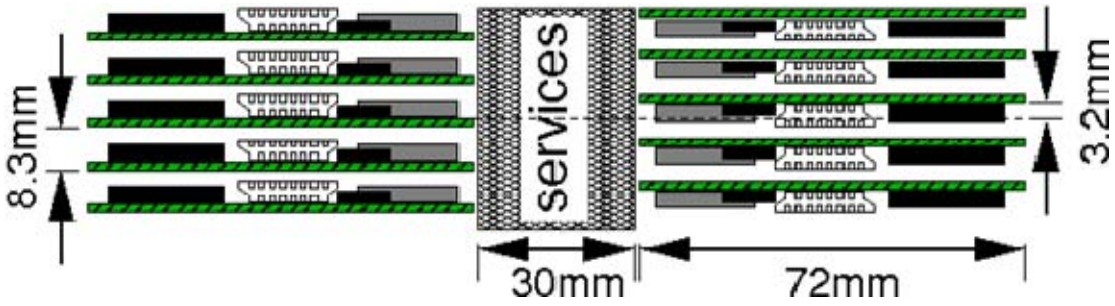
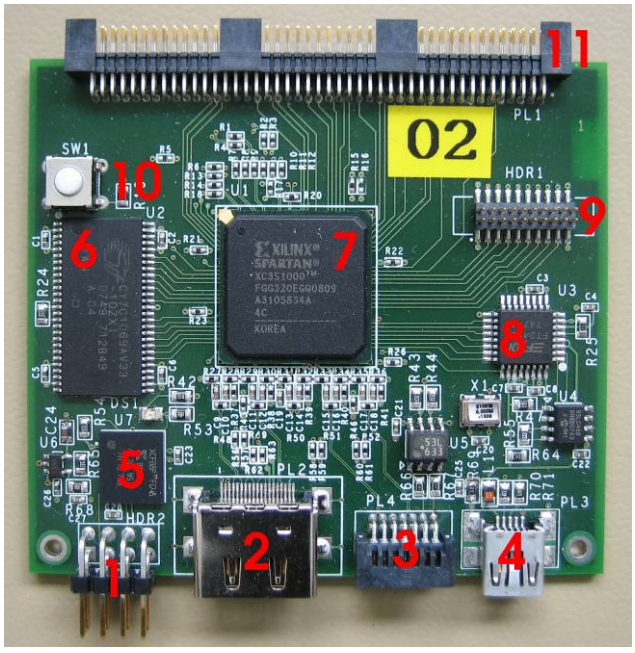


Figure 7.2 - Perpendicular view of DIFs arranged at the end of the slabs

Figure 7.3 contains a photograph of the DIF prototype with identification of the main components. As this prototype was designed for functional versatility instead of minimal dimensions, a smaller form factor can easily be achieved by optimising the number of electronic components w.r.t. the required functionality. Board space could be saved by removing the USB hardware and user connector and (by re-evaluating the FPGA) possibly the RAM chip.



The numbers on the photograph refer to the following components:

1. Programming connector ;
2. HDMI connector for DAQ link ;
3. DIF-DIF redundancy link connector ;
4. Mini-USB connector for tests ;
5. Non-volatile programming ROM ;
6. 2MB SDRAM memory chip ;
7. FPGA Xilinx Spartan3-1000 ;
8. USB interface chip ;
9. User connector for debugging ;
10. FPGA reset pushbutton ;
11. DIF-Intermediate board connector.

Figure 7.3 - Photograph of the DIF, with its main components identified

7.3 DIF AND IB POWER CONSUMPTION

From measurements as well as simulations using the Xilinx Power Estimator software, it appears that FPGA power consumption is dominated by the number and switching speed of allocated I/O ports. Therefore it is assumed that the power consumption of the DIF can be estimated by installing firmware which resembles the DIF with respect to the number, type and clock speed of the I/O ports, but lacking the complex logic providing the functionality of the true DIF.

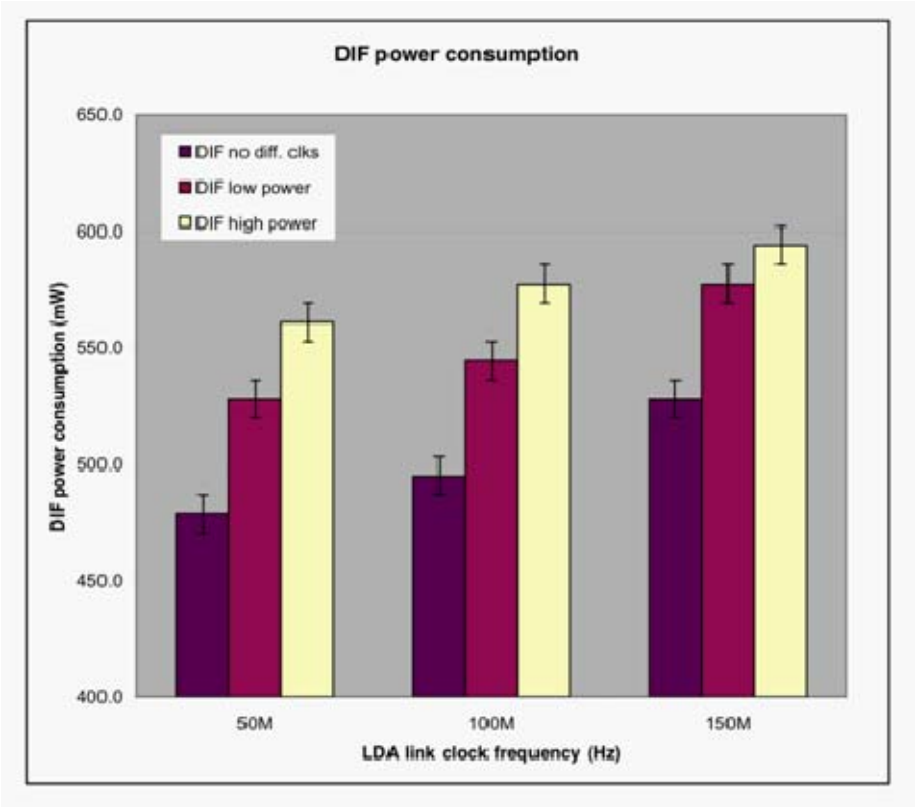


Figure 7.4 - Power consumption figures for a simplified DIF and no IB -see text

Figure 7.4 contains a plot of the DIF power consumption for three different speeds of the incoming LDA master clock, as well as high and low drives current (power) settings for the outgoing differential clock and data links. The plot suggests that the DIF power consumption is well within 1W, but it should be kept in mind that the tested object lacks the complexity of a final DIF, and does not include the IB power requirements. As the IB allocates power regulation hardware, its power dissipation probably adds significantly to the total power envelope. To be safe, it is recommended to estimate the DIF and IB power consumption at 1.5W nominal, and 2W for the worst-case scenario.

8 CONDUCTING GLUE DOTS

Electrical connection of the individual pixels of the silicon to the ASU PCB pads is achieved by dots of conducting silver loaded glue (Epotek E-4110). The basic concept has previously been demonstrated with the several thousand channels of the physics prototype using 60mm square wafers with 10mm square pixels.

The move to 90 mm wafers/ 5mm pixels places tighter constraints on the gluing process.

8.1 THICKNESS TOLERANCES /DOT SIZE

The calorimeter design requires glue thickness of ~100 microns. For 5 mm square pixels we require glue dots in the 3.5 to 2.5 mm diameter range to avoid overlap. Tests with glass dummies show this corresponds to a 50 micron thickness variation i.e. the overall spacing has to be controlled to at least this accuracy.

8.2 ELECTRICAL PROPERTIES

Detailed studies have been performed on glue properties.
Figure 8.1 shows a typical glue test board. Two such boards are glued together and individual dot 4-terminal resistances measured. A typical 3mm diameter, 66 micron thick dot between gold PCBs shows R< 0.005 Ω.

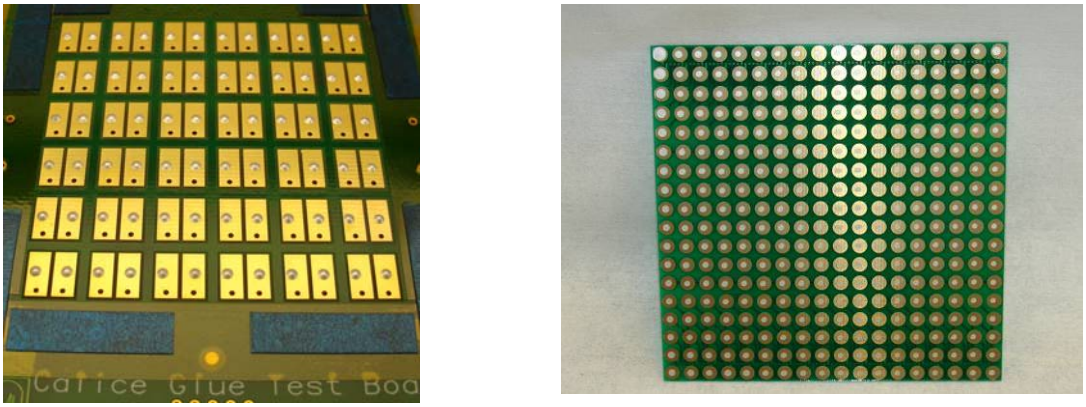


Figure 8.1- Glue test boards

Several studies have reported confusing high resistance effects, probably associated with thin oxide formation at the glue/ Aluminium contact to the wafer.
By detailed low voltage I-v measurements of virgin untested glue dots we have shown that initial high resistance behaviour reverts back to a low resistance after one off application of biases of the order of two volts. This is interpreted as punch though off the oxide layer.
Long term aging tests have been carried out by monitoring the overall resistance of arrays of dots connected serially ("snake" tests) whilst undergoing thermal cycling in an environmental chamber no significant effects were seen after 500 hrs.

8.3 PRODUCTION GLUING OF THE ASUS

The basic processes required are:

- Controlled glue dot deposition on to the PCB ;
- The 4 silicon wafers are picked up, aligned and placed on the PCB ;
- Accurate thickness and planarity control via vacuum jigs ;
- The assembled ASU is allowed to cure.

The various stages of the production chain concepts have been individually prototyped and will be trialled in the assembly of the demonstrator module with a view to eventual integration in a single automated sequence.

8.4 GLUE DEPOSITION

Glue dots are automatically deposited on the ASU PCB using a volumetric dispenser mounted on a Sony Cast Pro robot. This provides programmable 3d positioning to 20 microns together with dwell time control.
Direct volumetric control provides a fixed glue dot volume relatively independent of viscosity variations. The extrusion pressure profile is tailored to avoid glue tailing.

Dot size and position have been shown to be highly reproducible. It is possible to generate the 1536 dots required for 4 wafers at a rate of about 0.4 Hz, well within the glue workability time.

8.5 WAFER PLACEMENT

Four wafers have to sequentially be picked up, aligned and placed on the glue dots on the PCB with a positional accuracy of 100 microns. This is achievable with minor modifications to standard commercially available electronics industry pick – and place technology. In assembling the demonstrator, we will show the concepts using a modified manual BGA workstation.
The wafer is picked up and aligned with the PCB pixels via split field optics.
Such a procedure is readily automatable. We have previously built such a system using pattern recognition software to align wafers for the Atlas experiment.

8.6 THICKNESS/PLANARITY CONTROL

As described in above, the design requires tight tolerances on the planarity and thickness of the assembled ASU, which feeds though to the glue thickness. This is achieved by holding both the PCB and aligned wafers on vacuum jigs, while the glue cures. A portable trolley with vacuum reservoir and controls allows jigs to be moved between build stations (glue robot, pick and place, cure oven) under vacuum.
For the future we are investigating whether a second fast curing glue could be used to tack the wafer in position at the correct spacing on the placement workstation, markedly simplifying the automation process.

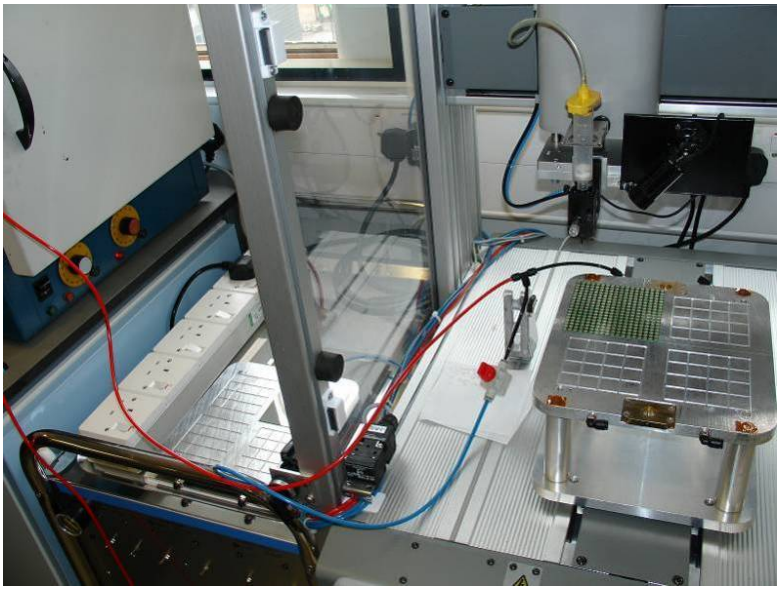


Figure 8.2- Showing a test board mounted on the vacuum jig under the dispenser head of the robot. Vacuum trolly and controls are also visible. The curing oven is to the left of the picture

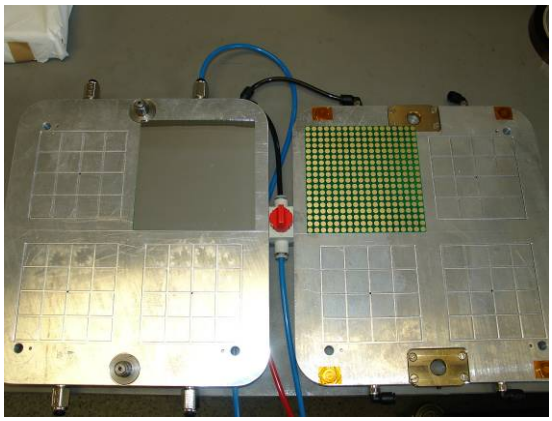


Figure 8.3- Jig, test board and wafer

Figure 8.4- BGA Workstation

9 HEAT DISSIPATION

The cooling system for EUDET module is foreseen to be most representative for the final heat dissipation management for the whole detector. The schematic 3D view of the prototype, in Figure 9.1, shows the current design of the general cooling system, including terminations going to each slab. The prototype has been dimensioned to fit EUDET module dimensions, with its specific shape (trapezoidal), and will be tested like a standard element of the whole cooling system for the barrel.

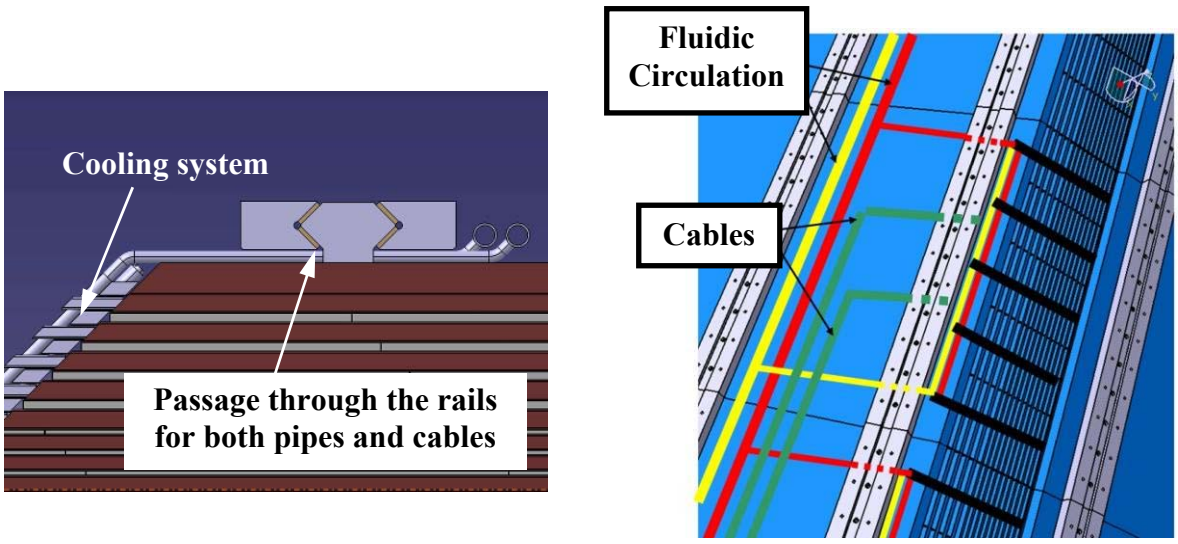


Figure 9.1 – Schematic 3D view of the cooling system

9.1 CONSTRAINTS FOR SLAB COOLING

Several constraints exist, leading to an important impact, not only on size and geometry, but also on the technology to adopt.

The constraints:

- Mechanical constraints due to electronic design (geometry of DIF card which is part

of last ASU of the SLAB) ;

- Space available: heat sources situation ;
- Service space between cooling and HCAL >1cm for cabling : DAQ + HV + GND ;
- Fastening system for cooling allowing fast connection/disconnection ;
- Heat power to dissipate, including (chips + DIF FPGA + interface components).

9.2 FLUID CIRCULATION /MOUNTING

The cooling technology is active, using fluid circulation. This solution allows fulfilling heat dissipation and mechanical requirements. The cooling system developed for tests on demonstrator is showed in Figure 9.2. This solution allows fluid circulation by the way of a network of contact areas / connector fixed on each 2 layers of copper of one slab. Free space has been found under the fastening system of the module to let a passage for pipes and cables under rails, toward exterior of detector. For the connection of pipes to each slab, it is done by the way of cold copper blocs, brazed on pipes, inserted between the 2 copper sheets of the slab, in the free space let between the 2 DIF cards.

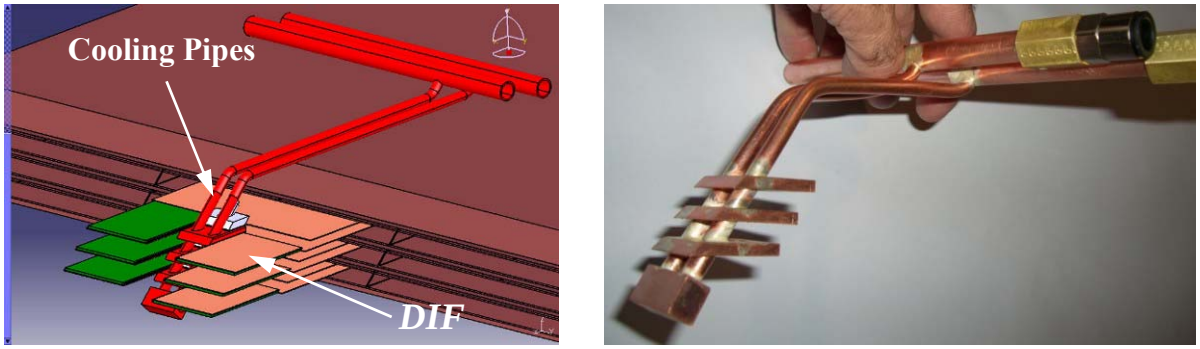


Figure 9.2 – Demonstrator: cooling and copper drain extremities

9.2.1 External cooling design

Each cooling system ❶ is inserted (Figure 9.3) and screwed to each column of slab with a thread rod and spacers ❷ and connected to the cooling network in a second step ❸.

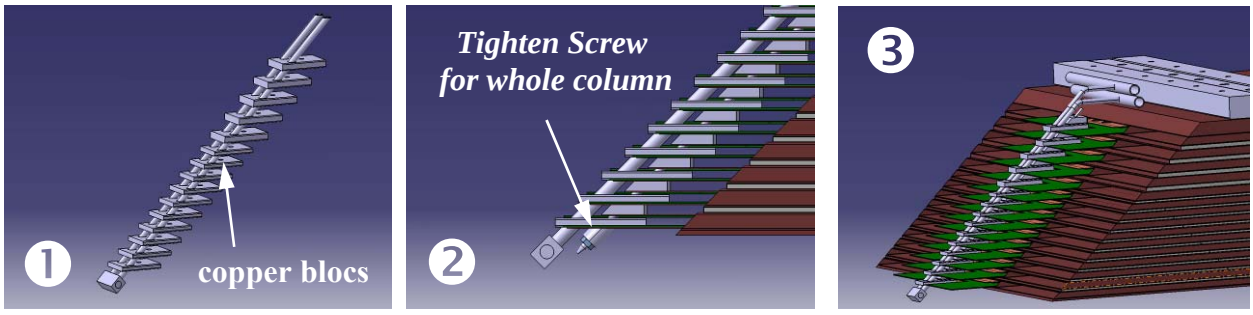


Figure 9.3 – A column (25 mm wide minimum) to ensure quick thermal system's connection

For now, the global design of the cooling setup is done, the Cooling system ❶ will be delivered end of September, 2008 for Chiller, sensors and acquisition also.

9.3 THERMAL ANALYSIS OF SLAB

The thermal analysis of heat conduction of one complete slab is performed. The model uses just the heat copper shield conductivity which is embedded in the slab and it takes into account the influence of the FPGA dissipation (DIF) on current design of cooling system. Various simulations also have been done with a FPGA power growing from 300mW to 2 W in order to provide advantageous proposals for the cooling system, especially for contact areas. The main advantages of these numerical simulations are to demonstrate the ability to make such a light, fast connected and performing system, even in worse conditions of conductivity.

Boundary conditions:

- **Load case**:

Total wafer power = 0.205 W
FPGA power = 2W (on DIF surface)
Main plate : 300 µm thick;
Upper plate : 100 µm;
Slab length : 1,55 m;

- **Limit Conditions :**

Temperature = 20°C,
Copper : λ = 400 W/m/K

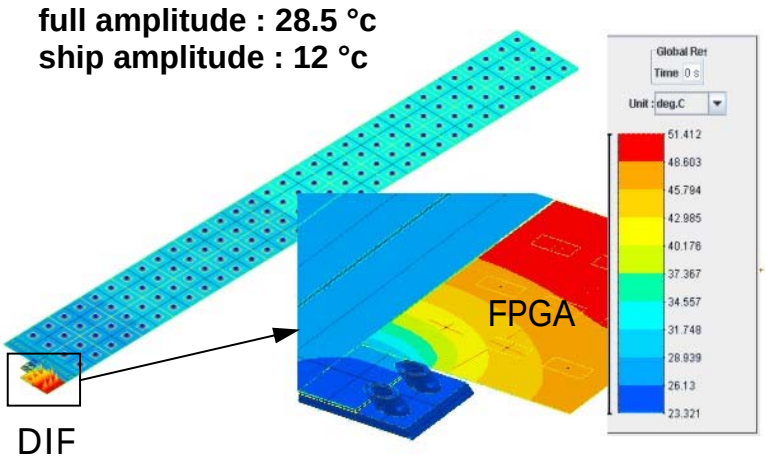


Figure 9.4 – Example of numerical simulation of heat dissipation in one layer

Thermal grease will be deposited on chips, under the copper foil (1.8×1.8 cm^2 chips, 300 µm thick + Cu 100µm). The copper drain is adapted to DIF card to be in contact with FPGA on DIF (« hot » Kapton for demonstrator). A thermal foam is inserted between the copper drain and the cold bloc in order to allow a heat dissipation as high as possible.

10 INTEGRATION OF PROTOTYPE

After production of single electronic components, mechanical structures, cooling and cabling services, they are assembled all together to achieve detector slabs and EUDET module integration. One of the major challenges appeared at preliminary studies is the non destructive disassembly of electronic sensitive components. This constraint is applied to the interconnection of ASU, to silicon wafers contact with High Voltage kapton feeding (see Chapter 6) and to thermal link between wire bonded chips with copper shielding and thermal drain foil (see chapter 10.3 below).
The integration procedure should also consider the total detector slab thickness including mechanical tolerances with respect to alveolar structure dimensions & their highly compact design. The thermal management of terminal boards (DIF card) is developed through this section.

10.1 INTEGRATION PROCEDURE

In order to achieve detector slab assembly including its insertion into alveolar structure with optimal number of handling operations, one unique integration cradle is under design. This cradle is ~1.6 meter long, U shaped in aluminium rectangular bar to safely clamp the H structure with full access to one of the slab two layers. Alignment and sliding edges are directly bolted to the cradle borders. They are guiding ASU positioning in the H structure before interconnection as well as the insertion & clamping of copper shielding and thermal drain foil. Table 10.1 is summarizing main integration steps of one detector slab and its insertion into alveolar structure.

Step	*Designation/operation*	*Comments*
1	**Insertion of H structure into integration cradle with alignment & lateral fastening.**	**Design of integration cradle in progress.**
2	**Sliding of HV kapton into H structure, positioning & gluing to H with few removable glue dots. Putting up HV contact agent.**	**HV removable contacts are under investigation.**
3	**ASU-1 placing, alignment & gluing to H structure with few removable glue dots. {Electronic chips + Si wafers are already integrated to ASU and quality controlled}.**	**ASU handling with vacuum pads + safe clamping.**
4	**ASU-2 placing, alignment & gluing to H structure with few removable dots. Interconnection bridge putting up & soldering.**	**Soldering device is aligned to ASU ends.**
5	**ASU-3-4… placing, alignment & gluing to H structure with few removable dots. Interconnection bridge putting up & soldering.**	**All ASU integration steps to slab detector are identical.**
6	**Electrical continuity tests of HV contacts & ASU interconnection bridges. Electronic control of full slab sensors.**	
7	**Insertion of Copper shielding & thermal drain with few glue dots to H structure + thermo-conductive agent onto electronic chips.**	**Study of Thermo-conductive agent is in progress.**
8	**Up side down tilt of detector slab by using second integration cradle similar to the first one.**	**Two end bearings are used to carry the tilt operation.**
9	**Integration of the second slab layer following steps 2 to 7**	
10	**Connection of integration cradle to alveolar structure, sliding of slab detector inside the alveoli after accurate dimensions control.**	**Interface frame ring is used to mechanical connection.**

Table 10.1 Integration steps of one detector slab & its insertion into alveolar structure

Most of these integration tasks are subject of dedicated technical specifications in order to describe input/output data, additional tooling and setups (detailed drawings + operating schemes).

10.2 CU SHIELDING & THERMAL DRAIN

As described in Chapter 9, the power dissipation is distributed along detector slab located on the electronic wire bonded chips. The goal is to transfer the heat as uniformly as possible

from the seven ASU (~1.5 meter length, 180mm wide) up to cold bloc located at one slab end. The challenge is the thermal drain thickness which should be close to the thickness obtained by simulations (400µm). The second aspect is to optimise the thermal contact between the copper and each ASIC, even if the chip and its bonded wires are protected inside the PCB by an isolate resin. One proposed solution is to use a thermal conductive agent.
Several thermal conductive agents are under investigation with specialized firms. Here are some of the most appropriate solutions with their technical data:

- Conductive grease; from 0.4 to 2.4W/m.K, electrical insulator or semi-insulator, adaptive to various thickness, stress on bonded wires to be evaluated ;
- Conductive gels; from 0.8 to 3.0W/m.K, electrical insulator or semi-insulator, adaptive to various thickness, contact with on bonded wires to be evaluated ;
- Conductive Foams; from 3.0 6.0W/m.K, electrical conductor, adaptive to various thickness, no contact with bonded wires, accurate alignment with electronic chips to be evaluated.

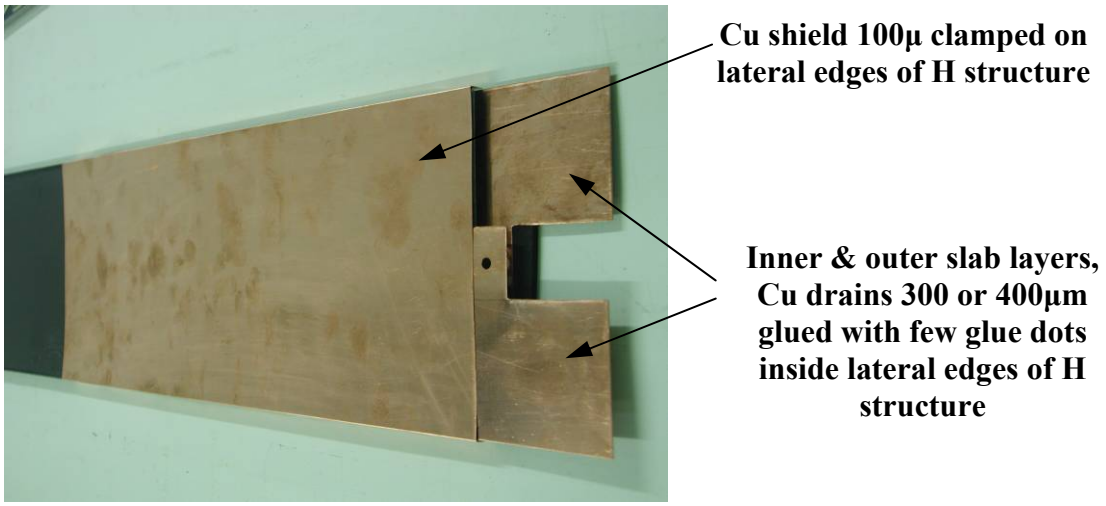


Figure 10.2 - Location of DIF board and cooling bloc at one end of the detector slab

10.3 FUTURE ITEMS & PROSPECT

To improve heat transfer along the Copper drain, in particular the local contact between electronic ships and Cu shield, the prospect is to link by brazing technique the two Cu foils. In addition, this solid link is increasing the mechanical stiffness of the foils assembly which will reduce handling difficulties with vacuum pads tooling. In the same way, the gluing to H structure can be reduced to external glue dots only along the Cu shield edges.
Considering the power dissipation of the DIF board, a fastening assembly to Cu drain is under investigation. Thermal agent (most probably thin conductive foam) will be added to improve thermal transfer by limiting pressure contact to acceptable values.

10.4 QUALITY CONTROL ISSUES:

As described through this TDR, the EUDET module is a highly sophisticated particle physics detector using newly developed technology. This module will be accomplished by several production sites over 5 different institutes. A quality control document will be

written in order to cover all technical domains from design steps up to data acquisition runs. In particular:

- Validation of technical specifications & drawings (Electronics, Silicon Wafers, Carbon Fiber Structures, Conducting Glue, Signal & High Voltage Interconnections, Cooling, Integration…) ;
- Destructive and non-destructive tests, thermal agents analysis & selection ;
- Production Procedures (Acceptance Criteria, Inspection, non-conformity, return for rework damaged components) ;
- Electrical Measurements and Dimensions (Temperature Controlled Room, 50% relative humidity), certified instruments & templates (go/no-go step gages) ;
- Packaging, Transport and Storage ;
- Documentation, Traceability, parts identification and indication of status ;
- Module demonstrator (integration and thermal management aspects, training with real scale slab, validation of the interconnection method).

Most of the integration tasks are subject of dedicated technical specifications in order to describe input/output data, additional tooling, test setups and detailed drawings (operating schemes). European and International standards (ISO 9001) as well as the solid experience of similar existing projects will be the basis of the EUDET integration procedures. These procedures will be used to examine the full slab unit (inside alveolar structure including cabling + services) and its compliance with technological and performance requirements.

11 FIRST VALIDATION STEPS: THE DEMONSTRATOR

As indicated in the introduction the construction and the exploitation of the demonstrator is an important step towards the realisation of the EUDET Module. Apart from the Front End Electronics as described in Chapter 5 and 6, all techniques introduced in the previous chapters will be applied as will be outlined in this section.

11.1 STRUCTURES AND MOULDS FOR THE DEMONSTRATOR

The alveolar structure and the H structure for the demonstrator have already been built. These have been already shown in Chapter 3. The main difference is the width of an individual H structure and alveolar which is 124 mm instead of 182 mm as foreseen for the EUDET module.
Still, this proves already now that long structures for an electromagnetic calorimeter at the ILC in general and for the EUDET module particular can be built. The alveolar structures have been subject to destructive (i.e. tensile and compressive) tests as described in [7].

11.2 SLAB MODEL FOR HEAT DISSIPATION TESTS

The demonstrator will be equipped with slabs which mimic the final slabs and which are conceived to perform comprehensive studies on heat dissipation (see Figure 12.1). For this slab several kind of cards will be produced:

- PCB cards acting as a heat source capable to simulate heat dissipation between 14.4 mW and 1 W, corresponding to 1 up to seven PCBs ;
- Cards to model the Adaptor and DIF card, these cards will dissipate up to 1 W each ;

- Several PCB cards for the temperature monitoring ;
- Card to steer the heat dissipation of the source and the DIF/Adapter Card model.

The number of ordered PCBs allows for the construction of two slabs.

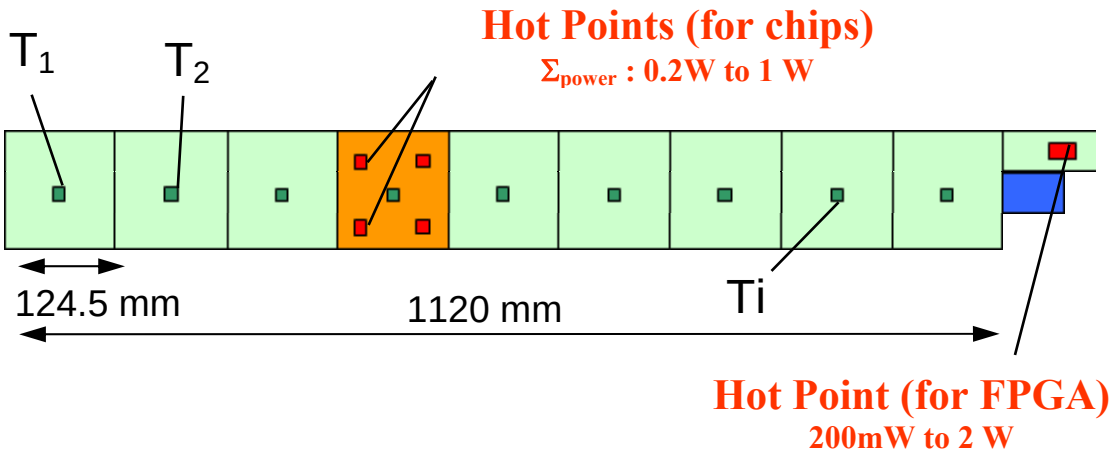


Figure 12.1 - Schematic view of slab for the demonstrator

The PCBs will be glued to glass plates following the procedures describes in Chapter 8. The glass plates represent the Si Wafers for the demonstrator tests. The interconnection between these ASU will be made in two ways:

- By a flat kapton cable soldiered using the halogen lamp technique as described in Chapter 6 ;
- An interconnection with manually glued wires, where the interconnections can be fully mastered.

This slab cooling tests (1 Hot ASU + 8 thermal ASU) to perform on the demonstrator will allow a correlation with simulations (transfer coefficients, contacts, design of copper foils …), and will check a thermal dissipation behaviour close to EUDET design.
All thermal tests with the thermal setup are to be carried out on October, 2008. Thermal tests on demonstrator will be performed by the end of year 2008.
Mechanical aspects and performances will be validated, allowing an optimization of simulations: conductivities, materials, geometries, and valid the cooling system for EUDET, by November, 2008.

11.3 DEMONSTRATOR INTEGRATION

During the assembly of thermal demonstrator, it is proposed to use a simplified integration cradle with vacuum pads tooling. The subject is to point out handling difficulties of extremely fragile Si wafers over ~1.5 meter with accurate alignment and positioning. The handling and placing of HV kapton feeding inside the H structure as well as copper foils on the interconnected ASU slab will also be better understood.
The copper shielding and thermal drain will be integrated to the demonstrator slab according to EUDET prototype design. Two configurations are going to be tested, brazing of Cu shielding (100 µm) with Cu drain (300 µm) giving total thickness of 450 µm ±25 µm and floating joint with total thickness of 500 µm (Cu shielding 100 µm + Cu drain 400 µm). As for the final prototype assembly, all these mechanical components will be cleaned up by

using ultrasonic bath (150liters, temperature range 30-85°C, transducers power 3600W, adjustable frequency 35-130 kHz). Two brazing methods under vacuum atmosphere will be investigated, low temperature domain (~240°C, mechanical properties unchanged) and high temperature domain (~760°C, hardening treatment to restore mechanical properties is necessary).

12 CONCLUSION AND OUTLOOK

This note concludes to a large extent the design phase of the EUDET prototype and constitutes therefore a milestone within the JRA3 EUDET program. The note describes the base line for the construction of the module and demonstrates the technological challenge to construct a compact and highly granular calorimeter. This concerns in particular the integration of the Front End Electronics into the layer structure of the calorimeter, which has to be embedded in slits of the order of 1mm. All elements of the detector represent technology reaching beyond nowadays state-of-the art.
The demonstrator allows for the validation of important engineering issues such as the fabrication of large size H-Structures and Alveolar structures but also for studies of the heat dissipation together with the potential of mainly passive cooling of the front end electronics embedded into the calorimeter layers. Results from studies employing the demonstrator are expected for the end of 2008. Parallel to the latter study the construction of the 'real' EUDET module will be pursued. This comprises the ordering of the necessary material and the clarification of the open issues such as the final layout of the PCB glued onto the Silicon wafers and housing the readout chips.
According to the schedule of the EUDET program the ECAL prototype is expected to be completed by the 30th of June 2009. Subsequently a rich testing program will be initiated. This program comprises:

- Long-term electronic tests to ensure the functionality of all readout channels of the module. Here the equipment used during the R&D phase will be used for the measurement will be used.
- Parallel to that the mechanical rigidity will be monitored, taking aspects like deformation due to the heavy weight but also thermal expansion of the slabs into account. Here, also the demonstrator will play a significant role in understanding these issues.
- The module is to be interfaced to the DAQ system which is developed in parallel by other groups within the EUDET program. Initial data taking of cosmic ray particles is to be performed.

After this initial commissioning phase foreseen to be completed by the end of 2009 the module will be exposed to test beams at DESY, CERN, two partners of the EUDET consortium. Here the main objective is to determine key parameters of the calorimeter such as energy and spatial resolution of the module. These test beam measurements will be conducted within the R&D program of the CALICE collaboration that, as mentioned above, currently operates the physical prototype in test beam. The data collected with the latter will be an important reference for the results obtained with the EUDET Module. These results in turn will be very useful for the full simulation of the ILC detector leading to a realistic estimation of the precision which can be expected from such a detector. Test beam results can be expected to be available by the end of 2011. The support for the exploitation of the module will comprise also the development of software for the data processing of the prototype. Here members of the CALICE collaboration will work closely together with the

main developers of the ILC Software. This work will benefit from existing software packages as they are currently developed within the NA2 package of the EUDET program. Beyond that the test beam results will allow for the improvement of simulation software packages such as GEANT4. This is in particular true for the response of the calorimeter versus hadrons. Again, the progress in this context will benefit from the collaboration between CALICE and the GEANT4 collaboration which is already initiated within the EUDET project.
In conclusion the EUDET Module will constitute a significant step towards the realisation of a SiW electromagnetic calorimeter for a detector of the ILC. With a strong emphasize on the engineering aspects the construction and exploitation of the prototype will be followed by a considerable physics program too.

13 ACKNOWLEDGEMENT

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14 REFERENCES

[1] The CALICE Collaboration, "*Design and Electronics Commissioning of a SiW Electromagnetic Calorimeter for the International Linear Collider*", JINST (2008) arXiv:0805.4833

[2] T. Behnke et al. (ed.), *Reference Design Report*, Volume 4: Detectors (2007), available at http://lcdev.kek.jp/RDR

[3] TEXIPREGR CC120 / ET443, http://www.saatiamericas.com/Seal/index.html.

[4] HEXTOOL / M61, http://www.hexcel.com

[5] M. Anduze, R. Poeschl, *"Design and Fabrication of moulds for the EUDET Module"*, Eudet-Memo-2008-07 (2008), http://www.eudet.org

[6] R. Cornat on behalf of the CALICE collaboration, *"Semiconductor sensors for the CALICE SiW EMC and study of the cross-talk between guard rings and pixels in the CALICE SiW prototype"*, Proceedings of the 13th International Conference on Calorimetry in High Energy Physics, 26 - 30 May 2008, Pavia (Italy), to be published in Journal of Physics: Conference Series.

[7] M. Goodrick, *"ECAL slab interconnection"* Talk given at the CALICE Collaboration Meeting;
http://ilcagenda.linearcollider.org/conferenceDisplay.py?confID=2757

[8] N. Seguin-Moreau, *"HARDROC1, Readout chip of the Digital Hardronic Calorimeter of ILC"*, talk +proceedings (2007), TWEPP07 Prague.