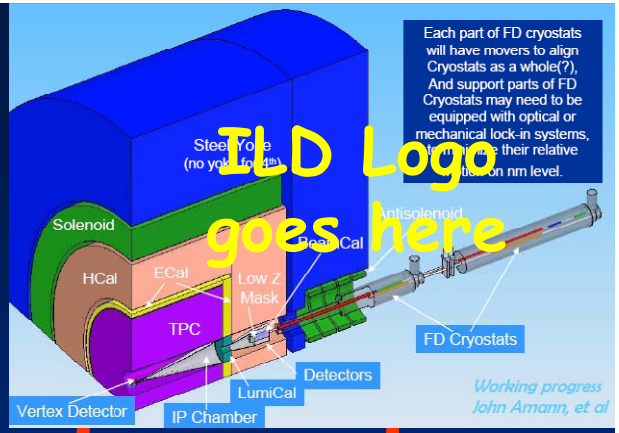
Worldwide Study of the Physics and Detectors for Future Linear e^+e^- Colliders



Continuation of LCTPC "advanced-endcap" planning for the ILD LOI

Ron Settles MPI-Munich

LCTPC advanced-endcap studies for the LOI

LCTPC engineering model for LOI

- "Advanced endplate" meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate. There were three meetings in 2007.
- The proposal for next steps (email 31.10.2008):

Reverse order today

DAQ issues added

--CERN 10 Nov. 14:00 (room to be announced):
-I will give an overview of the issues.
-Alain Herve will review the cooling strategy for all subdetectors, boundary conditions for the gas and how some of the CMS subdetector are cooled.
-Luciano will review the ideas he showed at Paris/2007 and maybe come up with first ones for the power pulsing.
-AOB

--LCWS 15-20 Nov (day, room to be announced):
-Summary the CERN 10 Nov. meeting.
-Dan has been interested in the LCTPC endcap material/layout and will show some ideas.
-Jan will tell us some pixel thoughts how an endcap for a large pixel TPC might look.
-AOB

--Meeting somewhere in Europe in Jan.2009 (time, place to be announced) Organized by Takeshi and possibly involving experts from other technologies.

--ILD Korea Feb. 2009:
-Review the previous three meetings above.
-Depending who goes to Korea, iterate on respective issues.
-Come up with a "to-do" list of things to be covered at the final meeting before the LOI, namely at the

--TIPP meeting on 11 March 2009
-This agenda can be made up depending on the outcome of the above and should envisage an iteration on critical topics.
-Finally conclude what should go into the LOI about the lctpc (advanced) endcap.

LCTPC engineering model for LOI

• Endplate, electronics, power

- This is about "standard" electronics (CMOS pixel-electronics require a separate study).
- "Advanced endplate" meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate.
- The (sometimes self-contradicting) requirements:
  - Number of pads: as many as possible
    (
  - Power to cool: as small as possible
    (
    (
  - Endplate material: as stiff and as thin (X_0) as possible
    (

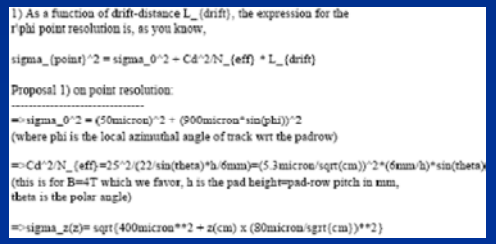
LCTPC engineering model for LOI

• Endplate, electronics, power

- This is about "standard" electronics (CMOS pixel-electronics require a separate study).
- "Advanced endplate" meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate.
- The (sometimes self-contradicting) requirements:
  - Number of pads: as many as possible
    (~10^6 channels per endcap?)
  - Power to cool: as small as possible
    (0.5mW/channel with power pulsing?)
    (cooling medium liquid or gas?)
  - Endplate material: as stiff and as thin (X_0) as possible
    (purpose of the present exercise)

LCTPC performance: 3-slides-overview from Cambridge ILD-LOI meeting

- continuous 3-D tracking, easy pattern recognition throughout large volume
- ~98-99% tracking efficiency in presence of backgrounds
- time stamping to 2 ns together with inner silicon layer
- minimum of X_0 inside Ecal (~3% barrel, ~15% endcaps)
- σ_pt ~ 50⊕diffμm (rφ) and ~ 500μm (rz) @ 4T
- 2-track resolution <2mm (rφ) and <5mm (rz)
- dE/dx resolution <5% -> e/pi separation, e.g.
- design for full precision/efficiency at 10 x estimated backgrounds


1) As a function of drift-distance L_{drift}, the expression for the r'phi point resolution is, as you know,

sigma_{point}^2 = sigma_0^2 + Cd^2/N_{eff} * L_{drift}

Proposal 1) on point resolution:

=>sigma_0^2 = (50micron)^2 + (900micron*sin(phi))^2
(where phi is the local azimuthal angle of track wrt the padrow)

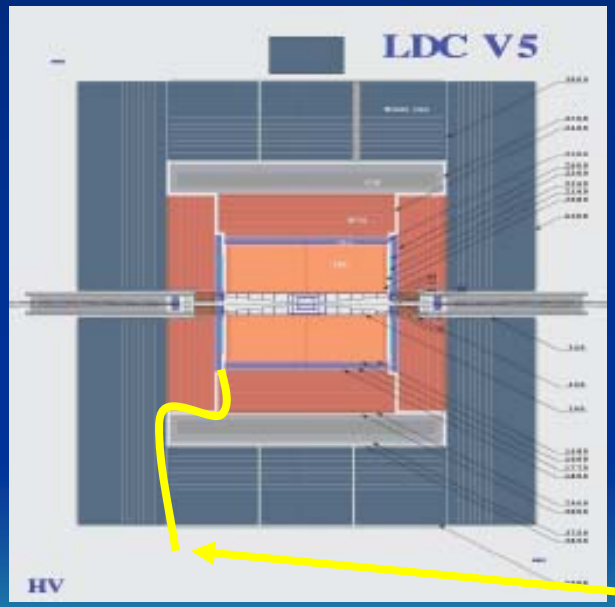
=>Cd^2/N_{eff}=25^2/(22/sin(theta)*h/6mm)=(5.3micron/sqrt(cm))^2*(6mm/h)*sin(theta)
(this is for B=4T which we favor, h is the pad height=pad-row pitch in mm,
theta is the polar angle)

=>sigma_z(z)= sqrt{400micron**2 + z(cm) x (80micron/sqrt(cm))**2}

LCTPC engineering model for LOI

- Size, weight, support, dead areas

- Dead areas:
  - 10 cm in z at each endcap for "standard" electronics/cables (may be increased later)



2) Endplate thickness:

Proposal 2) on Endplate thickness:

=>X_{tpcendplate}/X_0 = 0.15

New Mokka list (** mark changes wrt old list):

dz (mm)	material	% X_0	
0.003	copper	0.02	gating
0.03	kapton	0.01	
0.003	copper	0.02	
1.964	TPC_gas	0.002	
0.003	copper	0.02	mpgd
0.03	kapton	0.01	
0.003	copper	0.02	
1.964	TPC_gas	0.002	
0.003	copper	0.02	mpgd
0.03	kapton	0.01	
0.003	copper	0.02	
3.964	TPC_gas	0.004	
0.05	copper	0.35	pads
2	g10	1.03	
0.5	silicon_2.33gccm	0.53	ROelectr
2	epoxy,etc	1.932	
1	kapton	0.35	
**2	aluminium	2.24	cooling
1	kapton	0.35	
**3	carbonfibre	1.59	stiffness
80.45	Air(0.85)+G10(0.15)	0.02	air+
	+6.22 g10 space/ROboards		

summa (new model)

100mm 14.77 %X_0

- Space needed for φ≈1cm^2-cables here ~10^3 cables/side thru 5cm rings≈1m^2/side

LCTPC engineering model for LOI

• Endplate, electronics, power

- Endplate material on preceding slide: GOAL ~ 15% X_0
- With 0.5mW/channel with power pulsing, estimated by a EUDET development of a generalize TPC RO chip based on a further development of the Alice Pasa/Altro ⇒ 0.5kW/endcap (Luciano report)
- Cooling (liquid or gas) under study (Alain report)
- DAQ issues (Xavier report)
- Mechanical structure (next meeting at LCWS2008)

LCTPC engineering model for LOI

- Endplate: how was it done in Aleph?

- Sandwich structure for stiffness
- 22000 channels, 1.3kW per endcap
- Air/water cooling
- 25% X_0 without cables

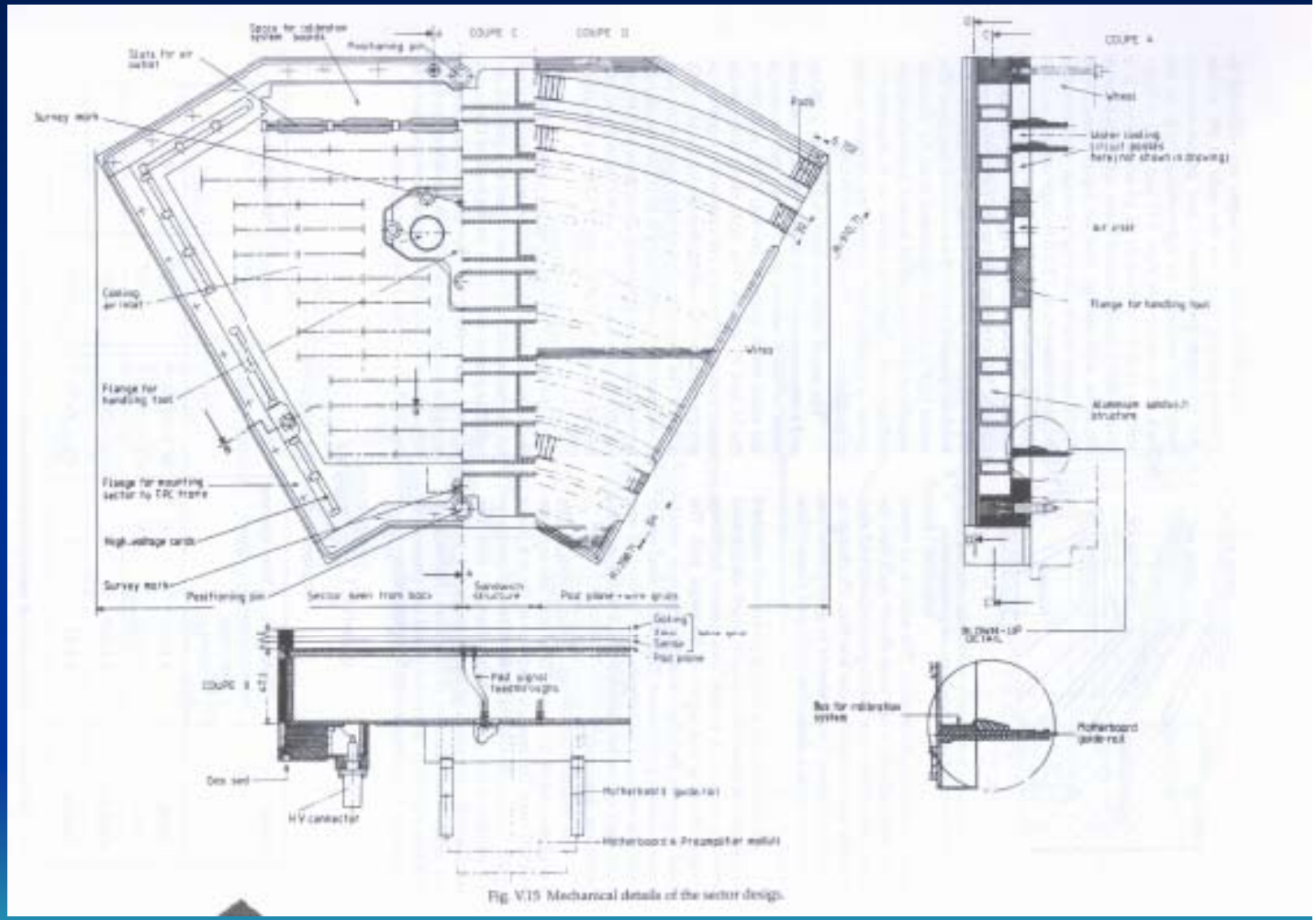


Fig. V.15 Mechanical details of the sector design.

LCTPC engineering model for LOI

- Endplate, electronics, power

- Endplate material: GOAL ~ 15% X_0
- Mechanical structure (next meeting at LCWS2008)
  - Aleph concept no longer possible for LCTPC
  - What can we do if electronic density too high?

    -- Reduce # of channels

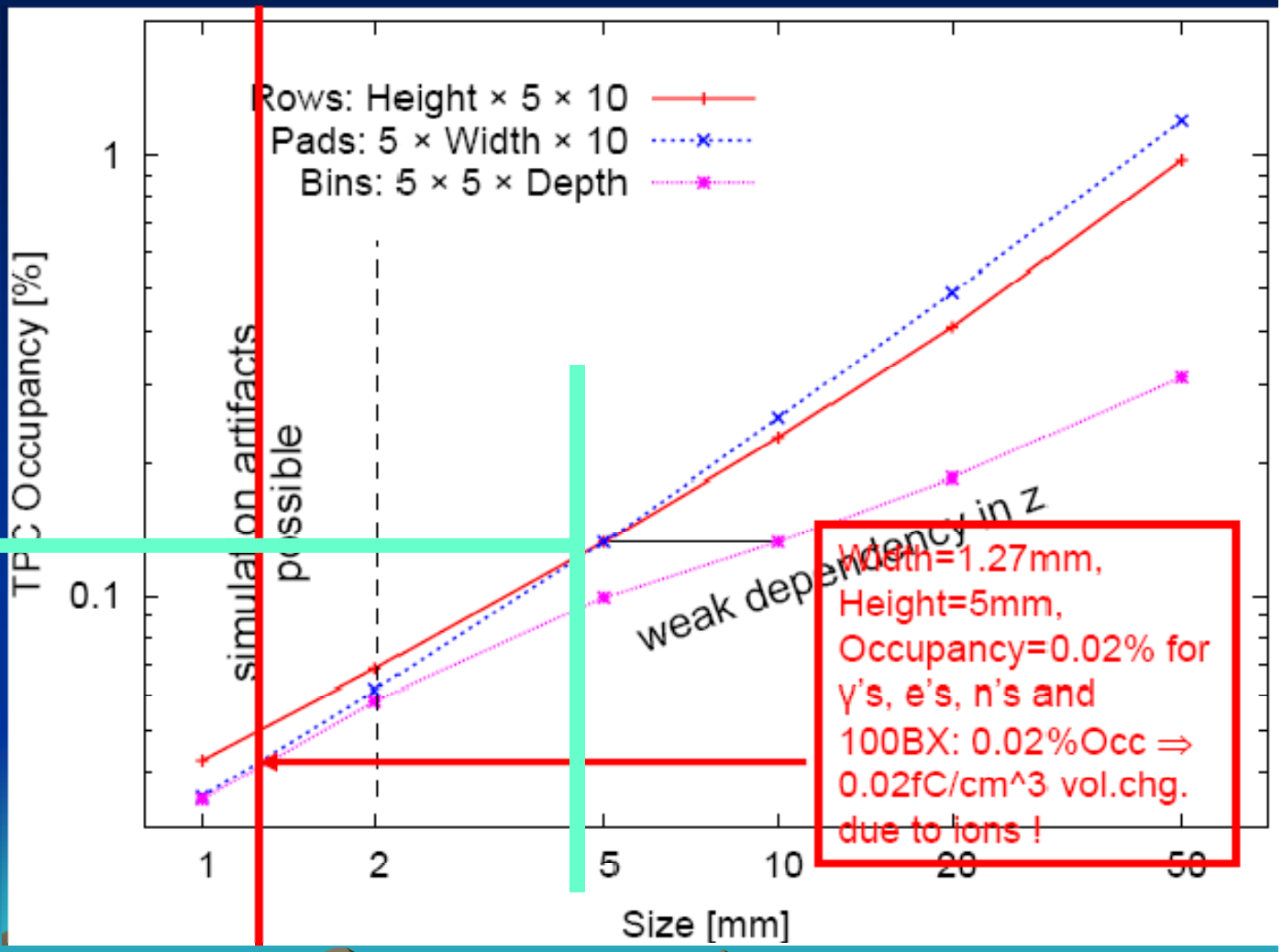
    Gluckstern: δ(1/p) indep. of pad height when σ_pt diffusion dominated

    Price you pay is…

2. LCTPC sensitivity to backgrounds

See talk#3 in opening session at Cambridge by Adrian Vogel:

Higher occupancy



LCTPC engineering model for LOI

- Endplate, electronics, power

- Endplate material: GOAL ~ 15% X_0
- Mechanical structure (next meeting at LCWS2008)

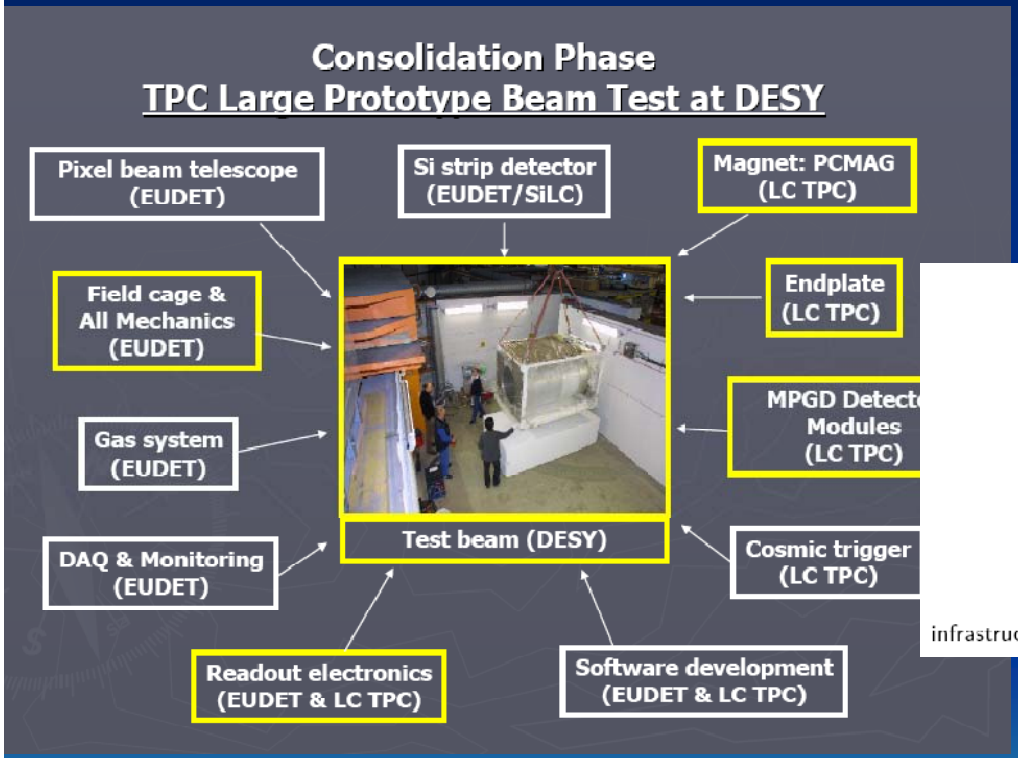
Continued next meeting…

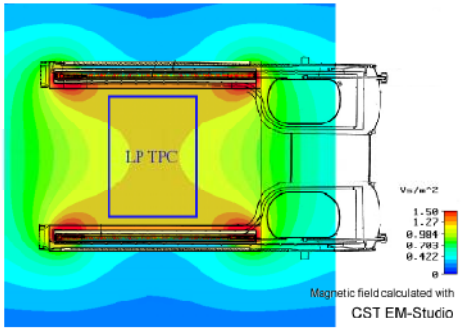
Back-up slides

LCTPC performance goals

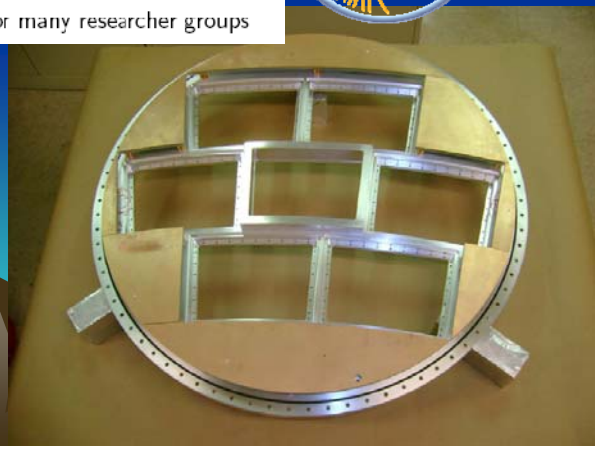
- R&D plans/risks

…to be verified (or revised) after tests on the Large Prototype:





infrastructure for TPC R&D, available for many researcher groups



LCTPC MOA to R&D/design a TPC: Status August2008

Americas

BNL √
Carleton √
Montreal req
Victoria √
Triumf √
Cornell √
Indiana √
LBNL prom
Louisiana Tech req

Asia

Tsinghua √
CDC:
Hiroshima req
KEK √
JAX Kanagawa req
Kinki U √
Nagasaki InstAS req
Saga √
Kogakuin √
Tokyo UA&T req
U Tokyo req
Minadano SU-IIT req

Europe

Brussels √
LAL Orsay req
IPN Orsay req
CEA Saclay √
Aachen √
Bonn √
DESY √
EUDET √
U Hamburg √
Freiburg req
Karlsruhe req
MPI-Munich √
Rostock √
Siegen prom
NIKHEF √
Novosibirsk √
St. Petersburg prom
Lund √
CERN √

Observer groups

Iowa State
MIT
Purdue
Yale
TU Munich
UMM Krakow
Bucharest

Signatures 24

Promised 3

Requested 11

New groups welcome

LCTPC engineering model for LOI and simulation

- Fieldcage, chamber gas

- Based on experience (Aleph, Star, Alice) and recent fieldcage for the LP:

  we estimate ~ 3-4% X_0 total for the inner and outer fieldcages.

- Gas properties have been rather well understood by our many small-prototype R&D tests. The choice for the LCTPC will be a BIG issue which would require a long discussion for which there is no time here. This has no effect on the simualtion. For the engineering, the boundary condition is that we must use a non-flammable gas.

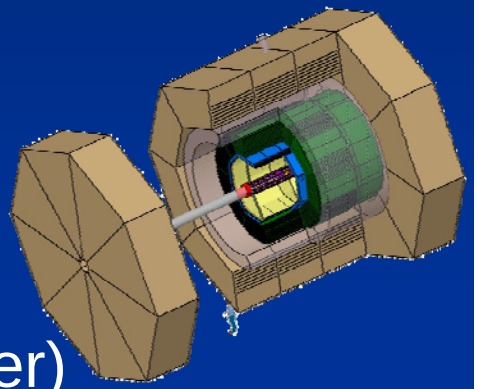
5. Push-pull ability

- At start, guess need 1/pb Z-peak calibration after each push-pull.
- This can probably be relaxed as experience is gained.
- Preliminary hardware discussion at IRENG07, SLAC Sept. 07:

Services **Detector ←→ Trailer**

TPC :

- **500 W per end plate**
- HV/service/data cables: ~ 10^3 per side
- Gas/cooling supply
- Alignment laser
- 50-200kW racks in the counting house (trailer)



Considerations on readout plane
Luciano's talk @ Paris Eudet mtg

IC Area (die size)

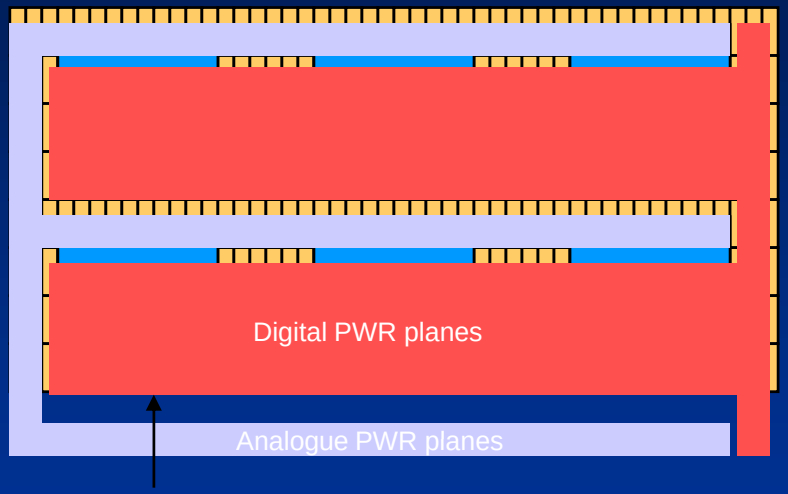
- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.6 mm^2 (estimate)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

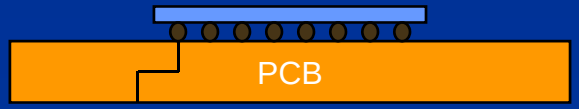
PCB dimensions < 40 x 40 cm^2 ⇨ ~53000 pads, ~800 FE chips / board

Considerations on readout plane

PCB topology and layer stack-up

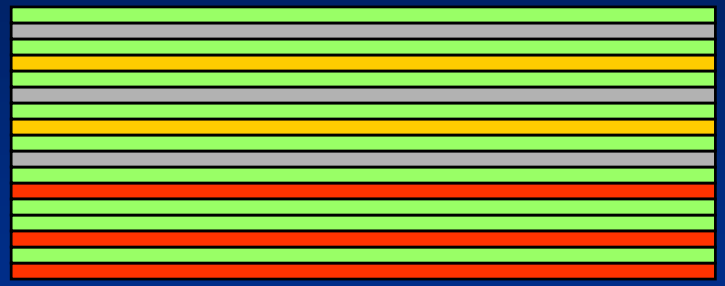


Flip-chip mounted

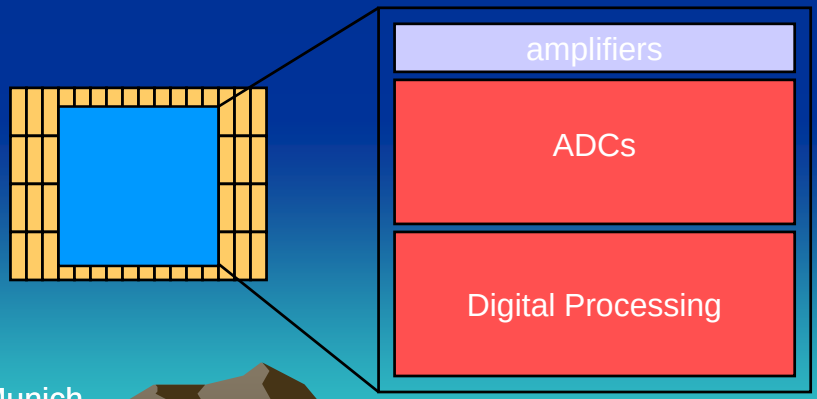


8-layer PCB

vdd
Digital signals II
gnd
Digital signals I
gnd
det gnd
Pad signals routing
Pad layer



Chip floorplan



Considerations on readout plane

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- average power / m^2 167 W