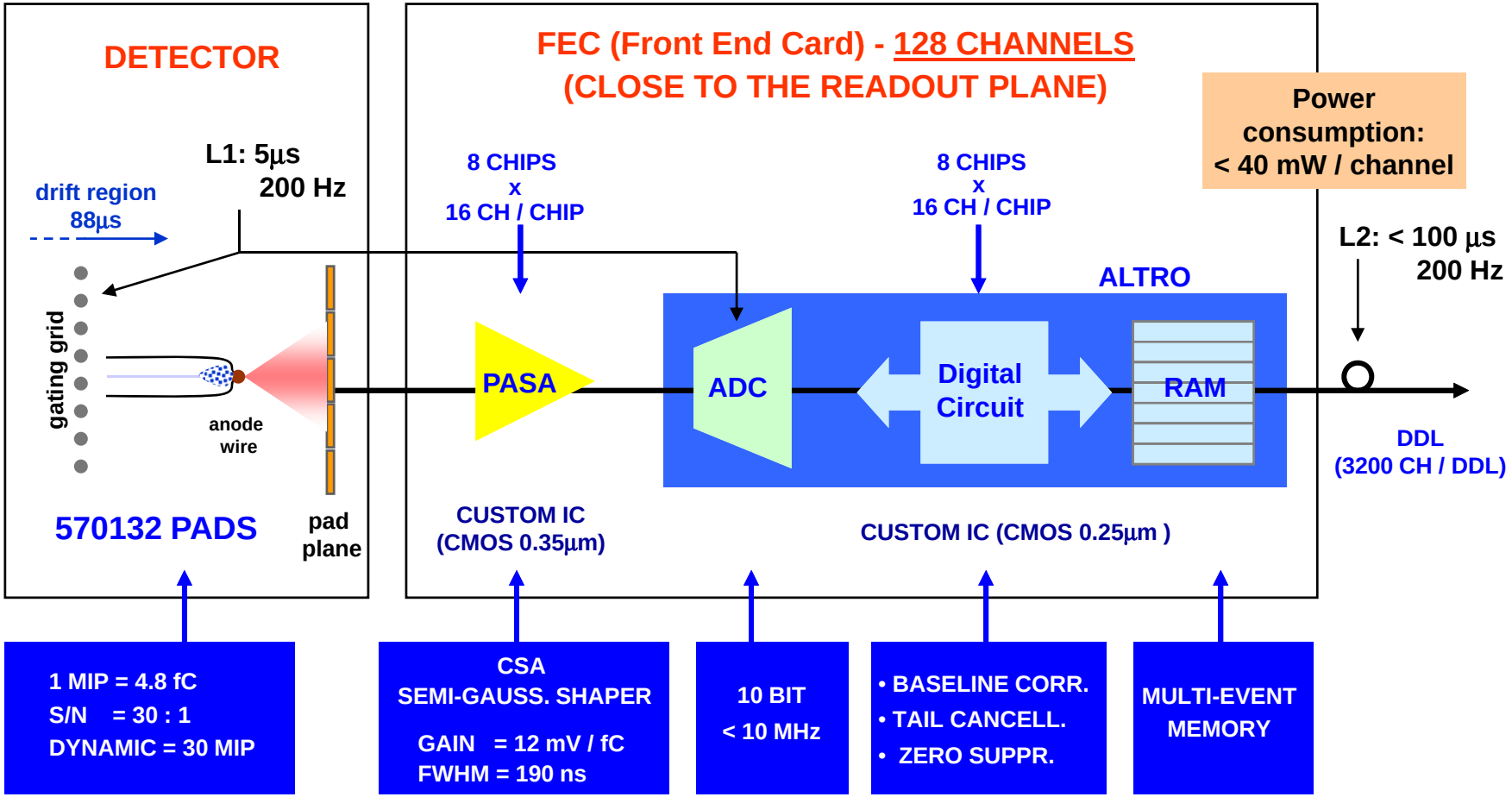
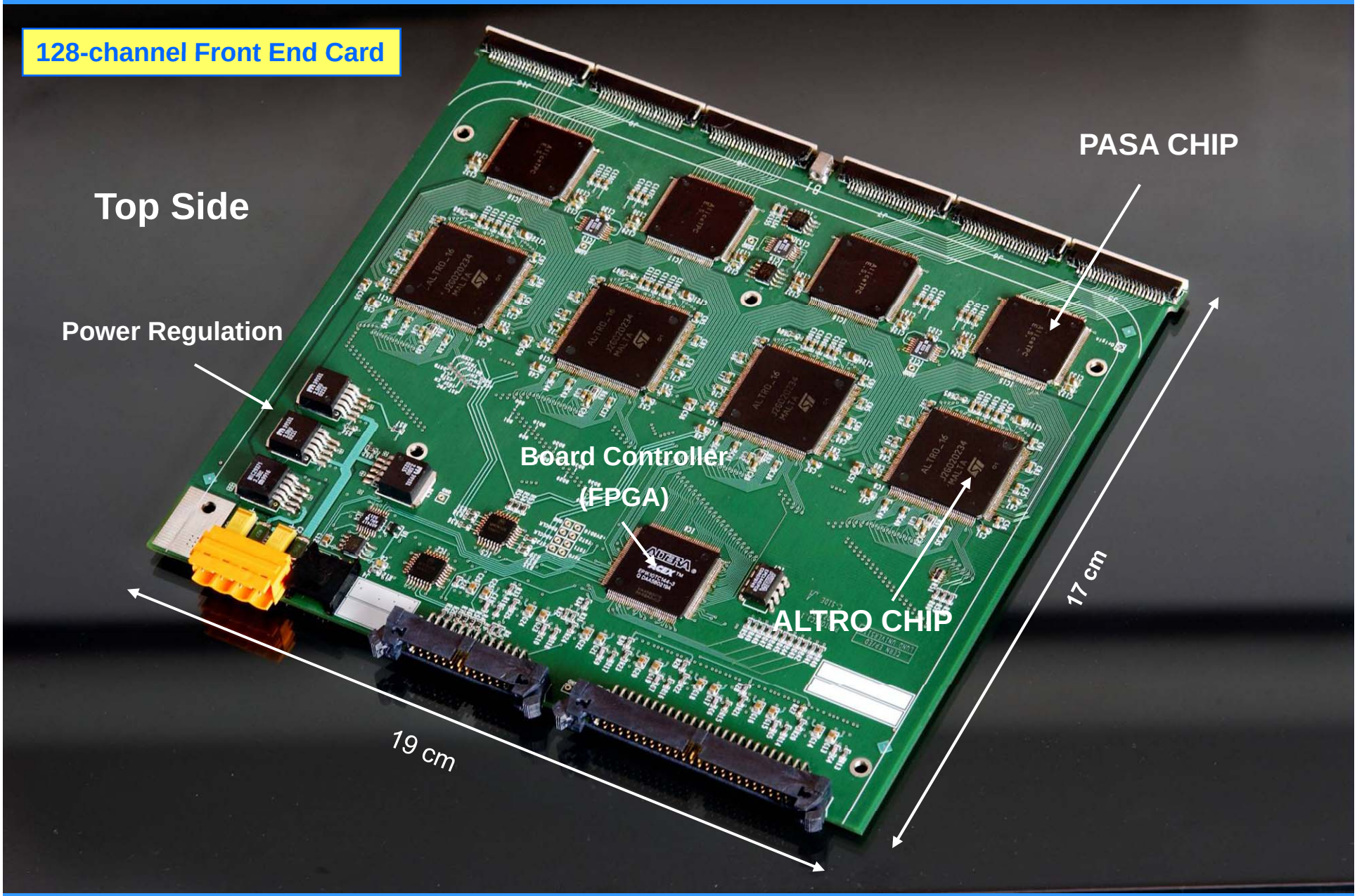
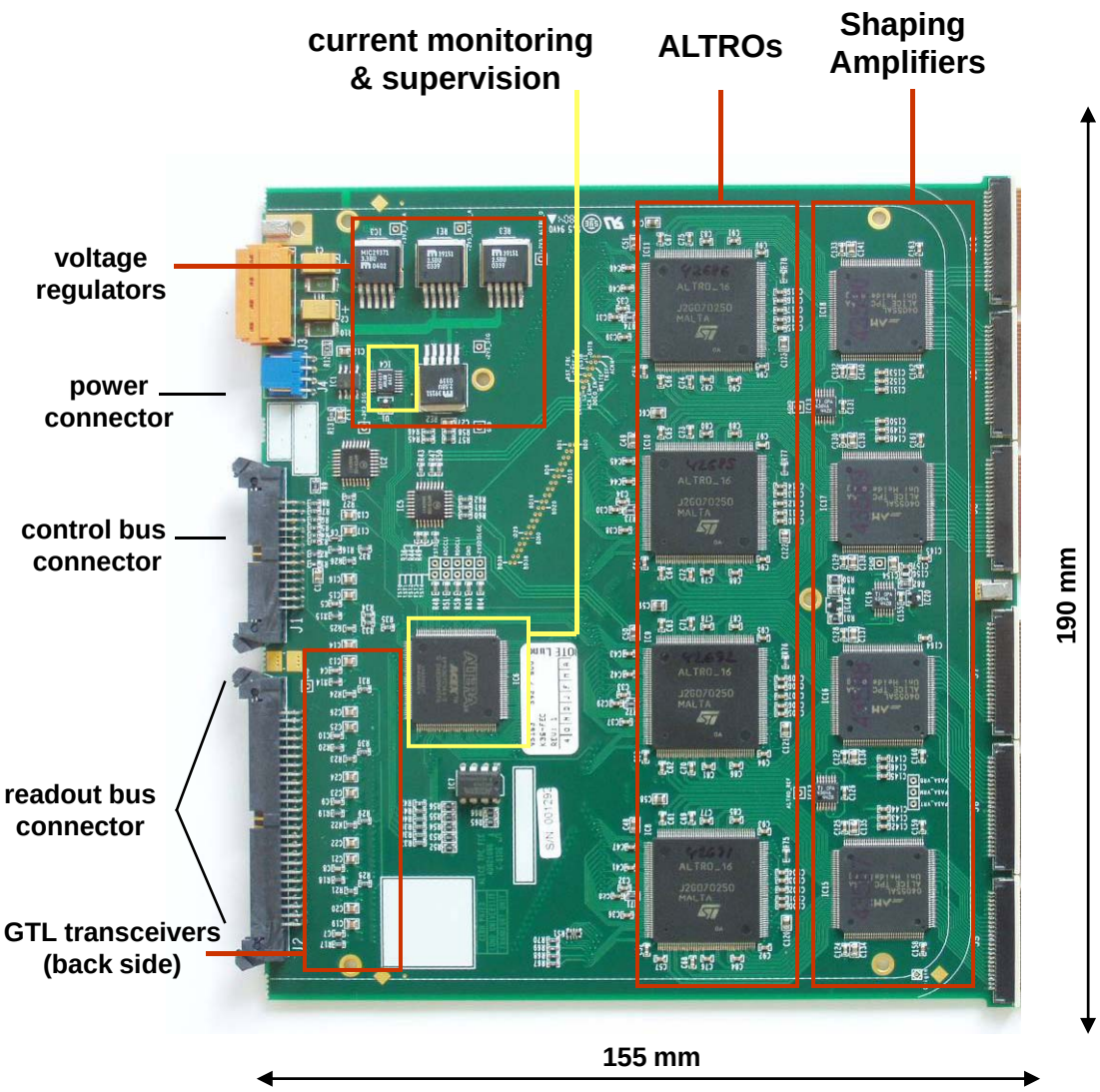
Front End Electronics Architecture

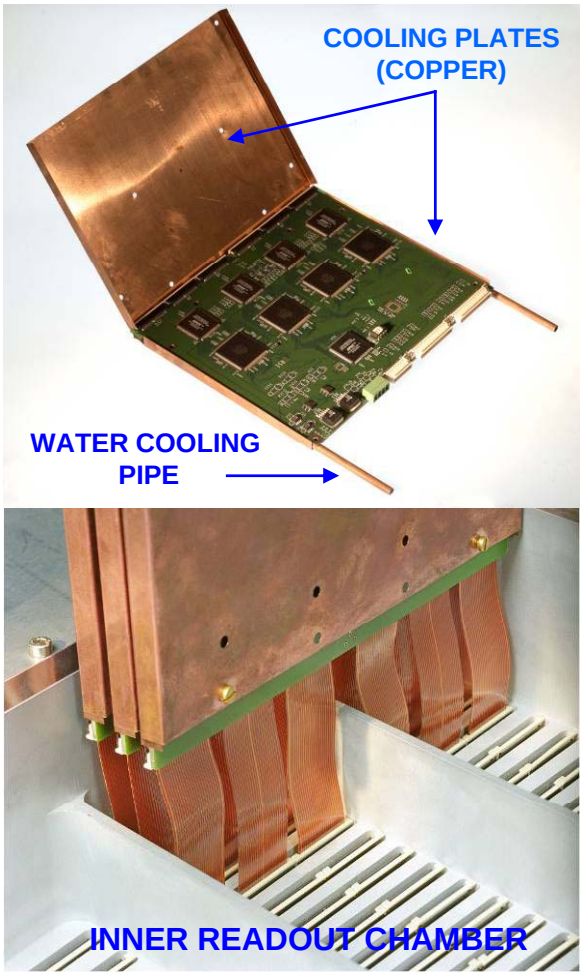


Alice TPC FEE – MWPC Readout



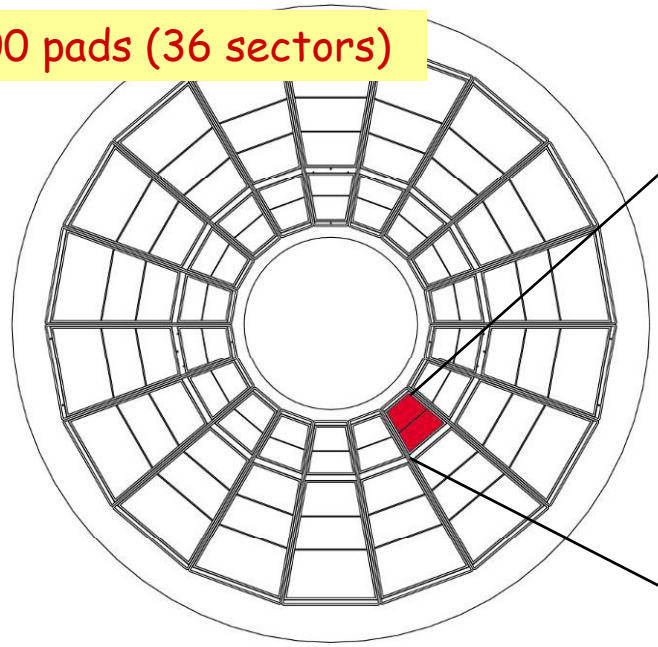
ALICE TPC Front End Card: Layout, Cooling and Mounting



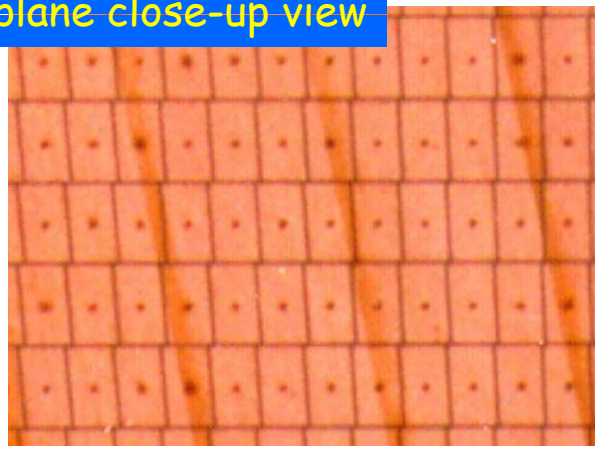


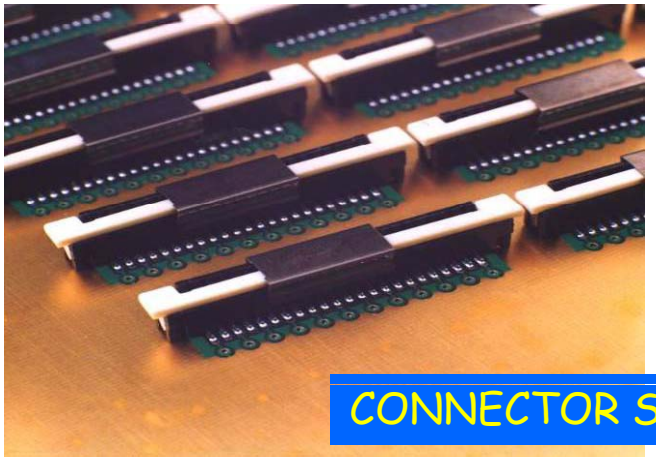
ALICE TPC - Readout Chambers

≈ 570 000 pads (36 sectors)

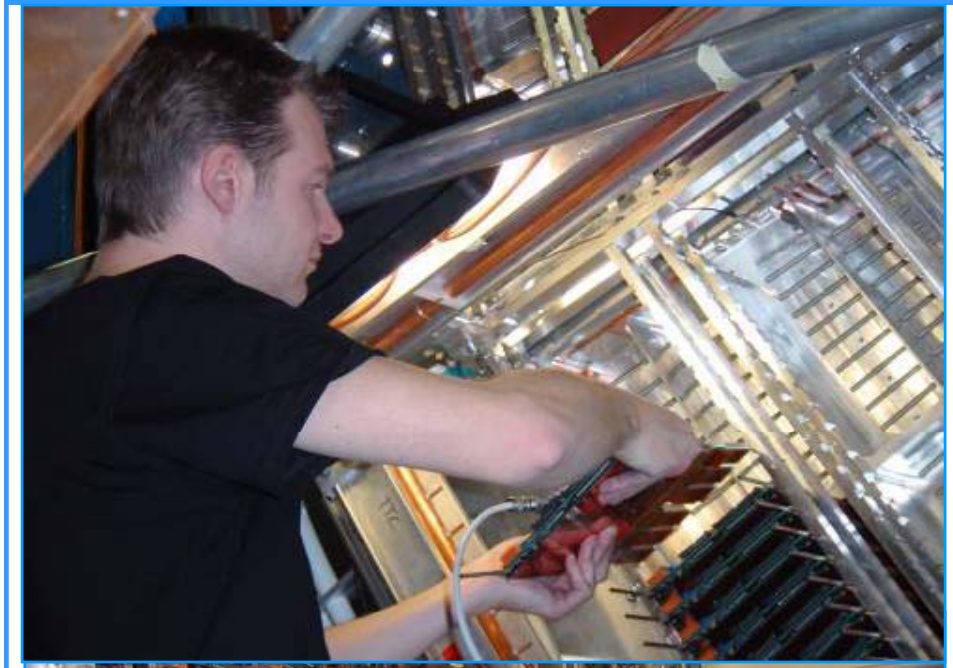


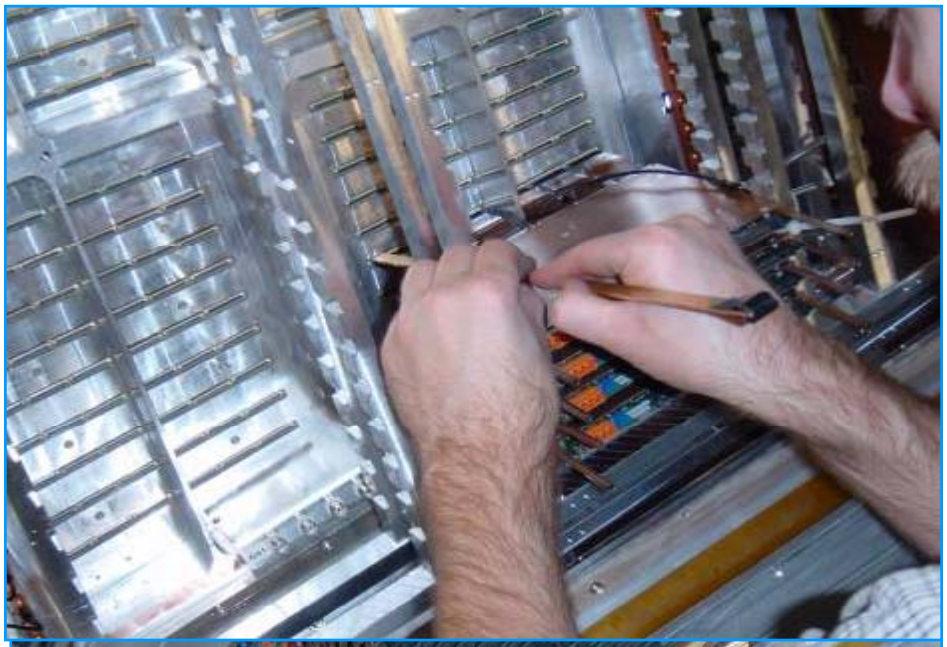
Pad plane close-up view





Installation of ALICE Front End Electronics (Feb-May '06)





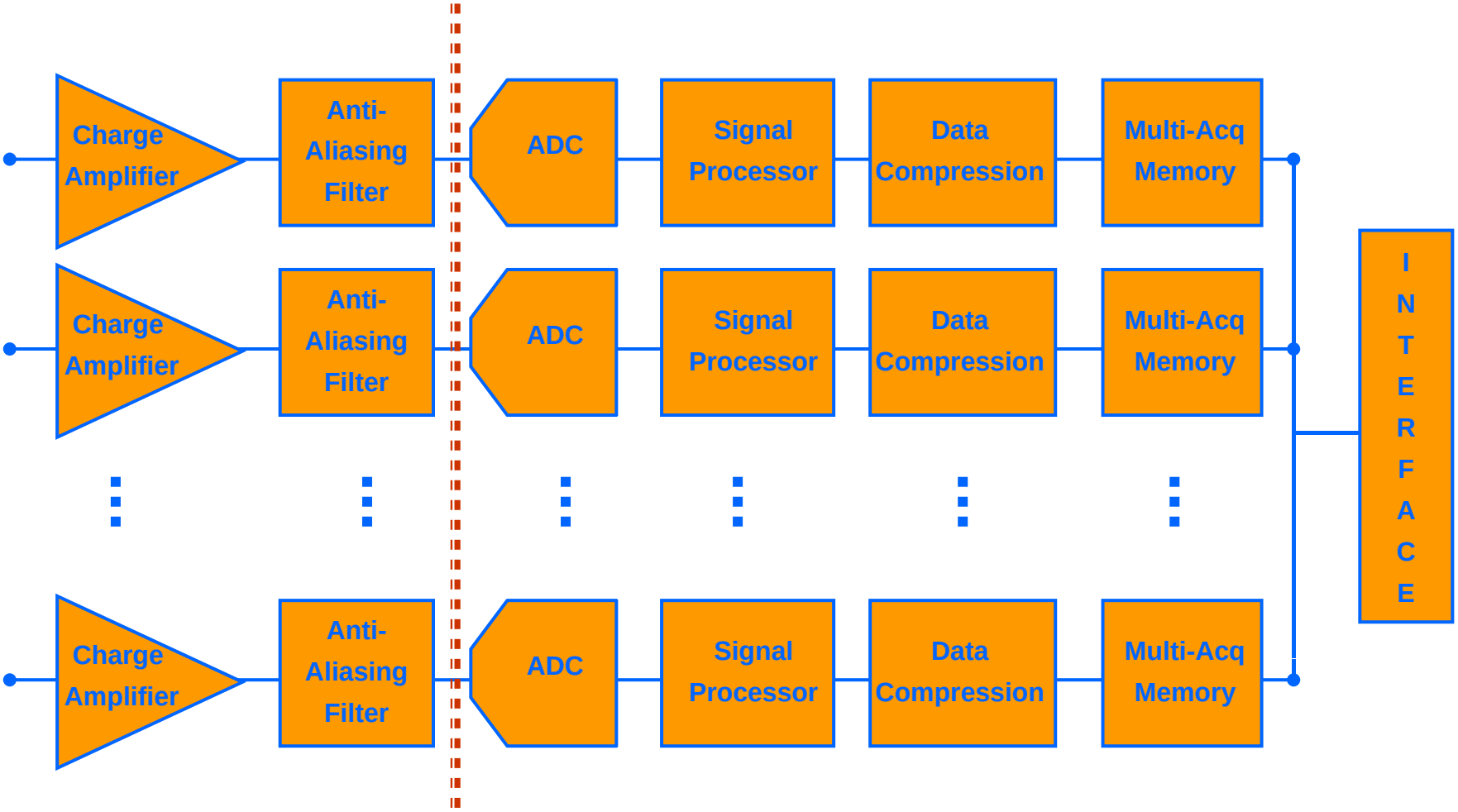

ALICE TPC in June '06

A general purpose charge readout chip for MPGDs

- ✓ number of channels: 32 or 64
- ✓ programmable charge amplifier
  - sensitive to a charge in the range: ~10^2 - ~10^6 electrons
  - Peaking time: 20ns – 100ns
- ✓ high-speed high-resolution A/D converter
  - sampling rate: 40MHz
- ✓ programmable digital filter for noise reduction and signal interpolation;
- ✓ a signal processor for the extraction and compression of the signal information (charge and time of occurrence).
- ✓ Two readout modes: external trigger or self-triggered
- ✓ Trigger can have any position wrt the acquisition window
- ✓ Standby mode

Charge Readout Chip Block Diagram

32 / 64 Channel



Considerations on readout plane

IC Area (die size)

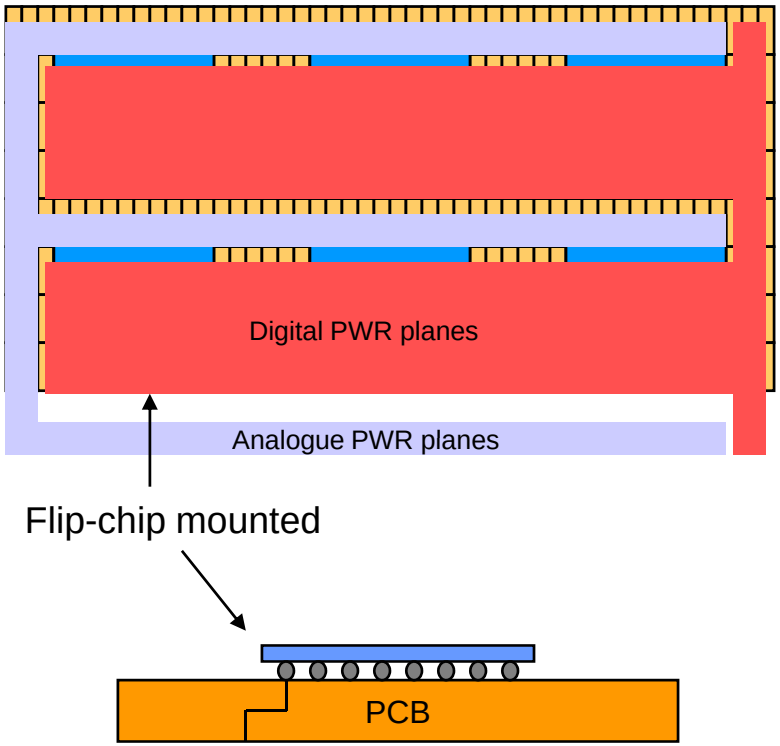
- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.7 mm^2 (prototype ➡room for improvement)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

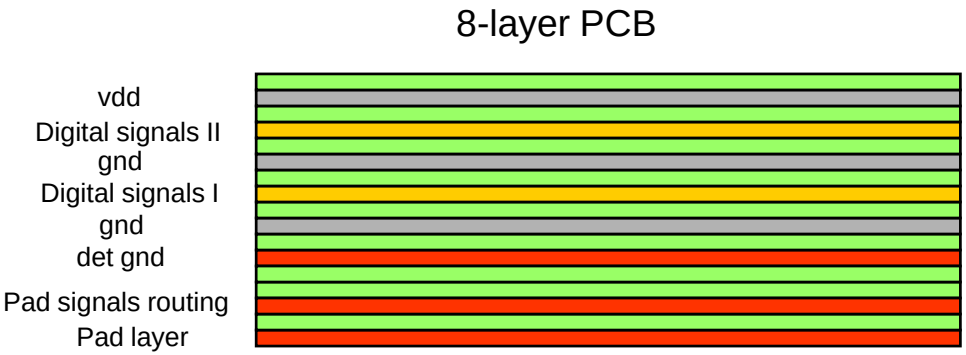
Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

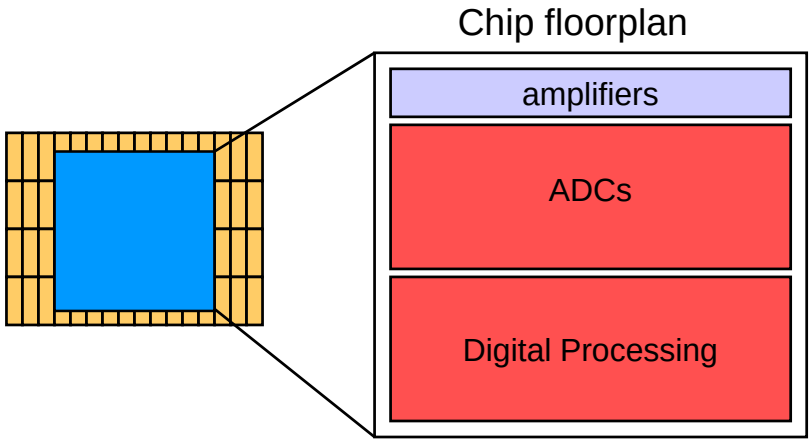
PCB dimensions < 40 x 40 cm^2 ⇨ ~53000 pads, ~800 FE chips / board

Considerations on readout plane

PCB topology and layer stack-up

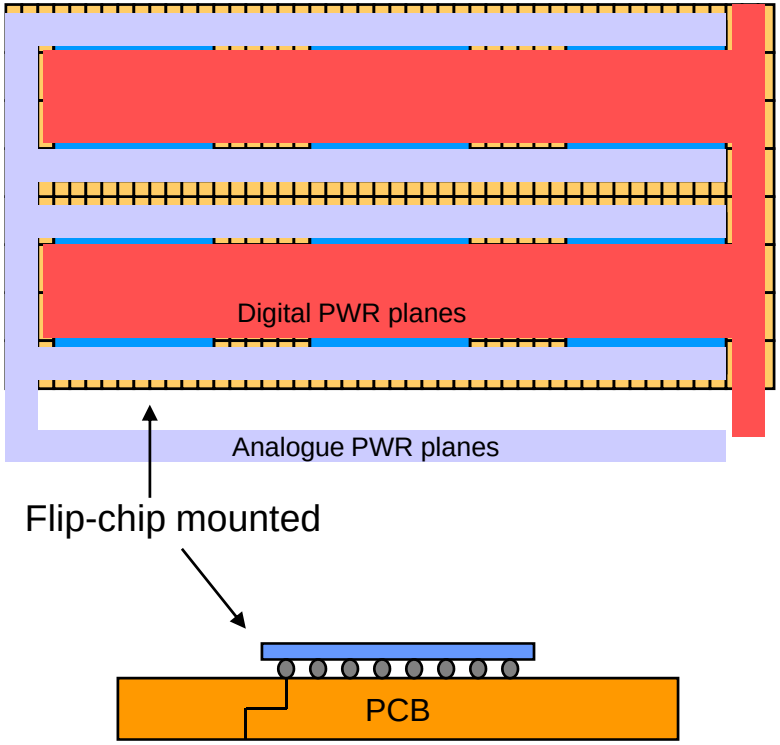




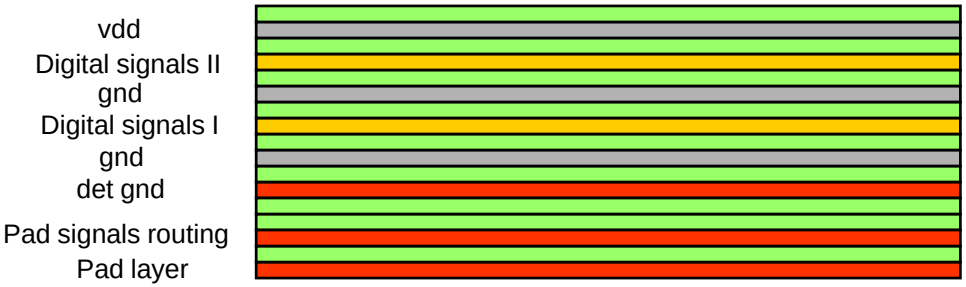


Considerations on readout plane

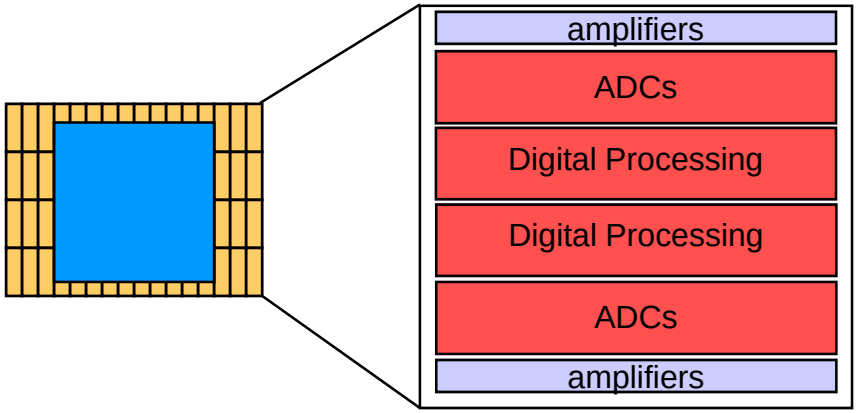
PCB topology and layer stack-up



8-layer PCB



Chip floorplan



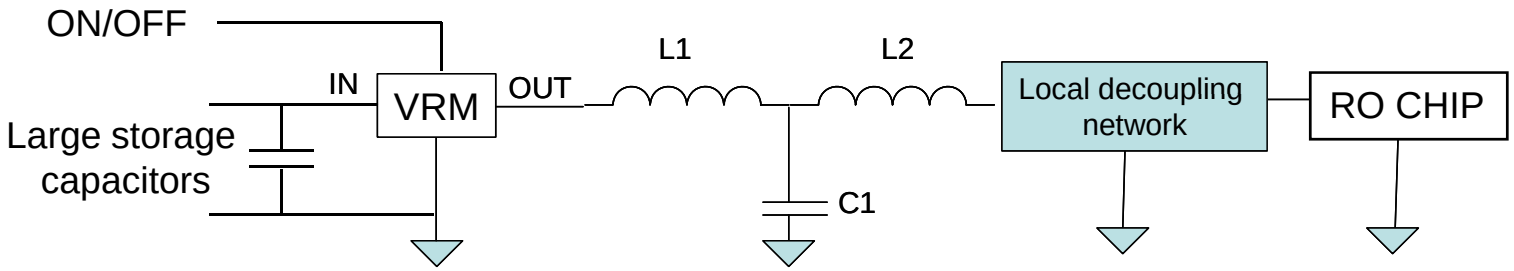
Considerations on readout plane

Power consumption

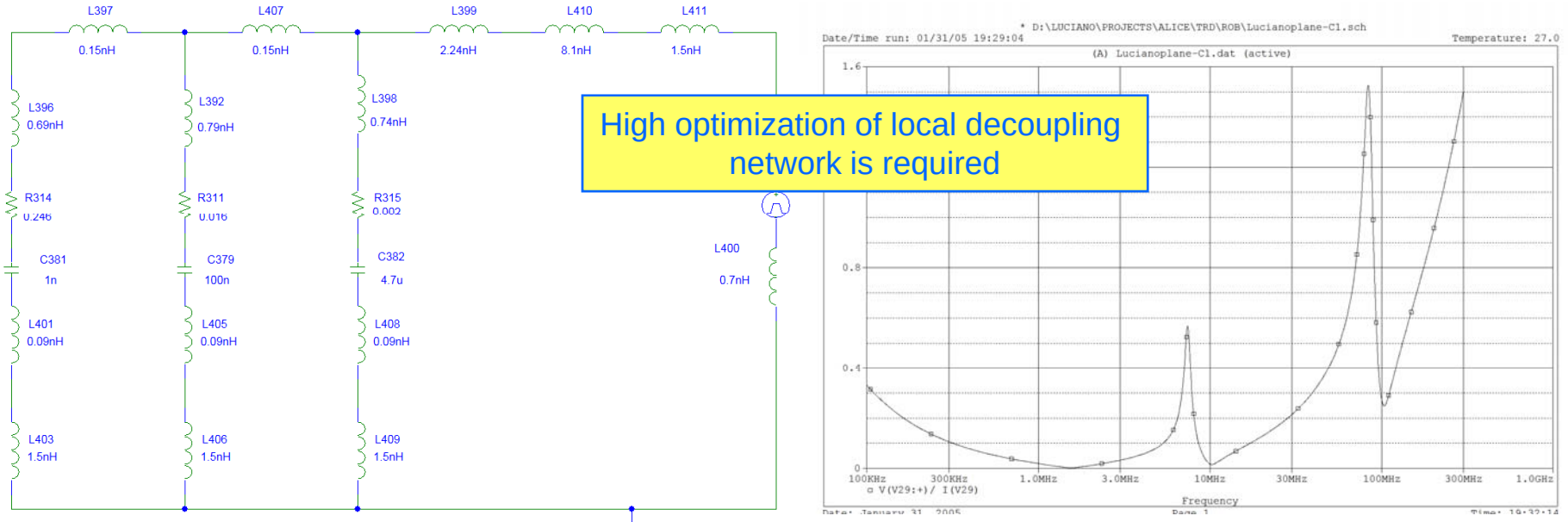
- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- average power / m^2 167 W

Considerations on readout plane

Readout Board power delivery network



Model used to evaluate the impedance of the local power delivery network



Impedance (W) versus frequency for the local power delivery network connected to the RO chip through a power
plane with zero inductance.