RS232 control of new FONT4 board

- New FONT4 firmware controlled by software over RS232 connection
- ‘Proof-of-principle’ signal generator designed and implemented

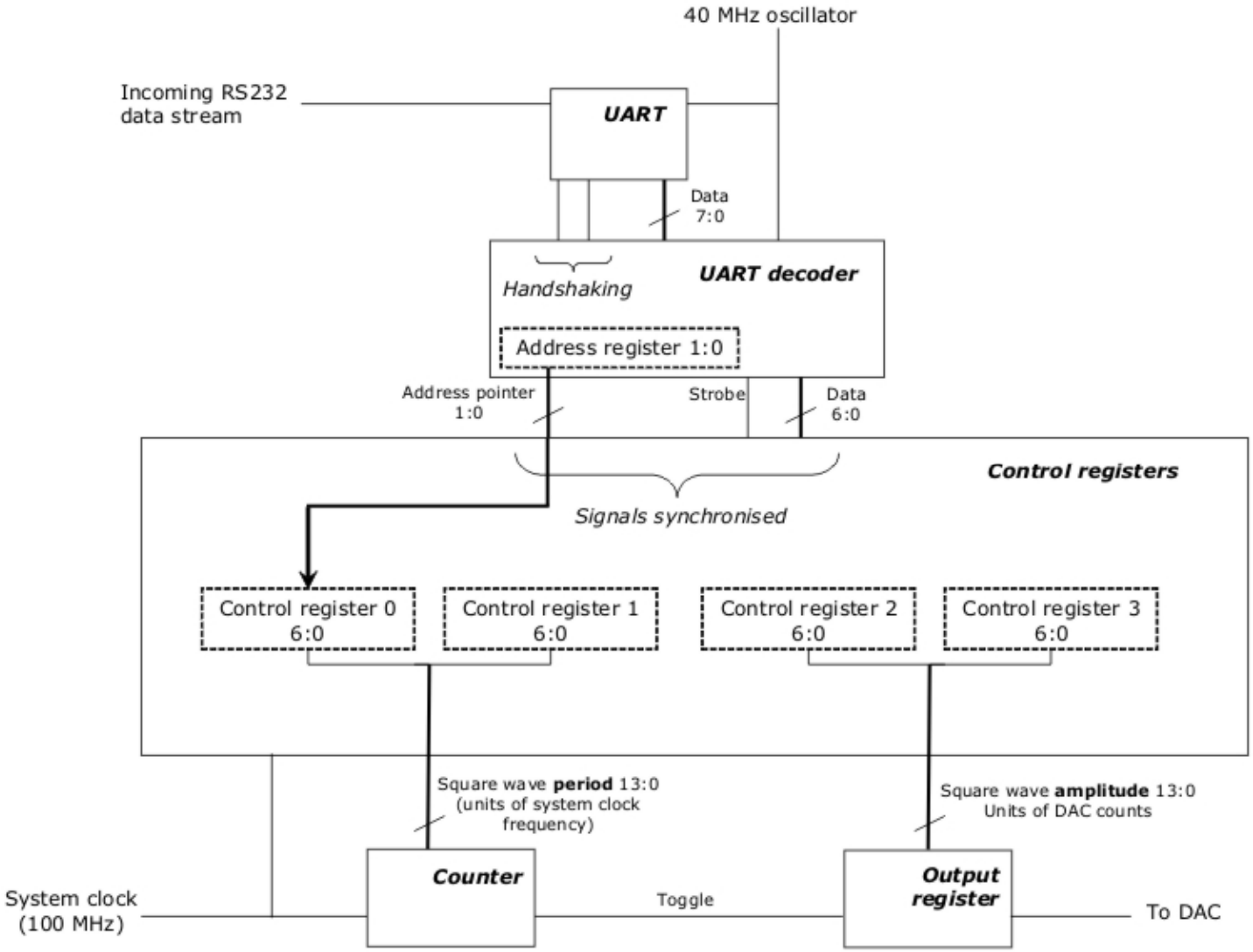
- Signal generator
  - Implemented on existing FONT4 board
  - Produces square wave output from DAC
  - Has variable period and amplitude
  - Variable parameters are stored in **control registers**
  - Control registers set over RS232
  - UART and control register architecture is modular, expandable and directly applicable to new FONT4 firmware

Control register architecture modules

- Control of signal generator utilises three modules:
  - UART
  - UART decoder
  - Control registers
- UART
  - Standard UART clocked at 40 MHz
  - Converts serial RS232 stream into 8-bit bytes
- UART decoder
  - Logic clocked at 40MHz
  - Interprets byte as either a command or 7 bits of data
  - A set MSB implies data
  - Contains a register which holds the address of the active control register
  - A ‘command’ simply changes the value of the address register

- Control registers module
  - Clocked at the system frequency of 100 MHz (357 MHz for FONT4 firmware)
  - Signals from decoder are synchronised via DFF metastability guard
  - Contains four 7-bit control registers
  - Received data are written to the register specified by current address
  - Control registers are concatenated in pairs to form two 14-bit outputs corresponding to period and amplitude
  - (Note 14-bit chosen as this is appropriate for FONT4 firmware)
  - Square wave generated by 100 MHz logic based on these outputs

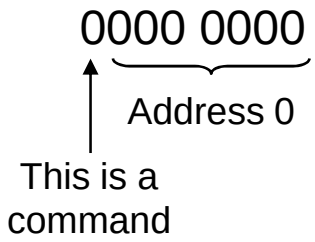
Signal generator schematic



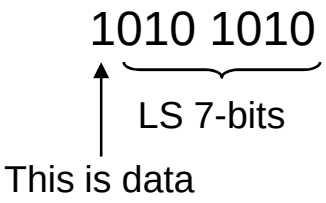
Example of setting signal period to 6,186 cycles

- In binary, 6,186 is 0110000 0101010
- Setting signal period requires transmission of 4 bytes over RS232

1. Specify 0th control register (contains least significant 7 bits of period)

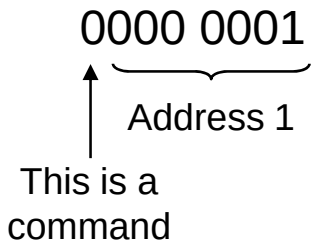


2. Send least significant 7-bits of period as data

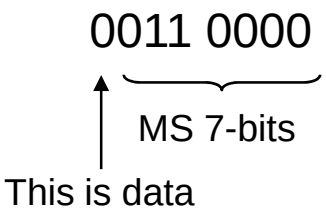


Example of setting signal period to 6,186 cycles

3. Specify 1st control register (contains most significant 7 bits of period)

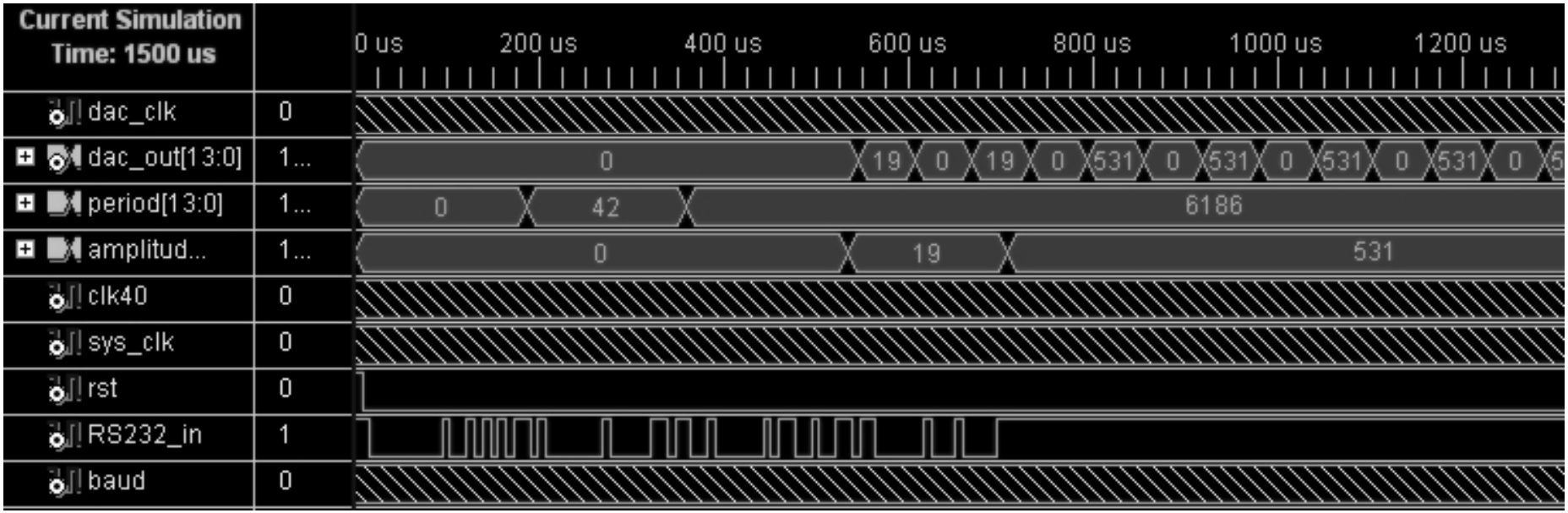


4. Send most significant 7-bits of period as data



Signal generator simulation

- Control registers module
  - First, period is set to 6186 cycles of 100 MHz (note it's actually ½ period)
  - Then amplitude is set to 531 DAC counts
  - DAC output is seen to alternate between 0 and 531 at correct frequency



Signal generator implementation

- Source of the ‘teething problems’ discovered
- FONT4 board 1 appears to have faulty RS232 chip (I really don’t have a vendetta against this board!)
- Outgoing data is correctly converted to RS232 by chip
- Incoming RS232 data produces no TTL signal (confirmed by scoping chip)
- Signal generator was downloaded to board 2 and everything worked as in simulation
- C++ code used produce appropriate RS232 streams
- Tested for both positive and negative amplitudes (i.e 2’s complement is handled correctly)

Current modification for use with FONT4 firmware

- Basic premise easily expanded for FONT by increasing number of control registers and size of address register
- Some technical details with input and output delay values (must increment to desired value)
- Possible source of undefined behaviour when used with FONT:
  - All control parameters must be correctly set during the ring clock cycle with bunches
  - Cannot have, for example, the MS 7 bits unmatched with the LS 7 bits
- Solution
  - Add another level of buffering for control registers
  - Require a special ‘update’ command to be sent over RS232 before buffers are copied
  - Allow FONT4 sampling logic to veto updates until after ring clock cycle
  - Ongoing work at present