1m2 GRPC Acquisition System

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Overview

- Glass RPC and semi-digital calorimetry
- DAQ
- Data format
- DAQ tests
- Injection with test capacitor functionality
- Cosmic run
- What next?

Glass RPC and (semi) digital calorimetry - 1

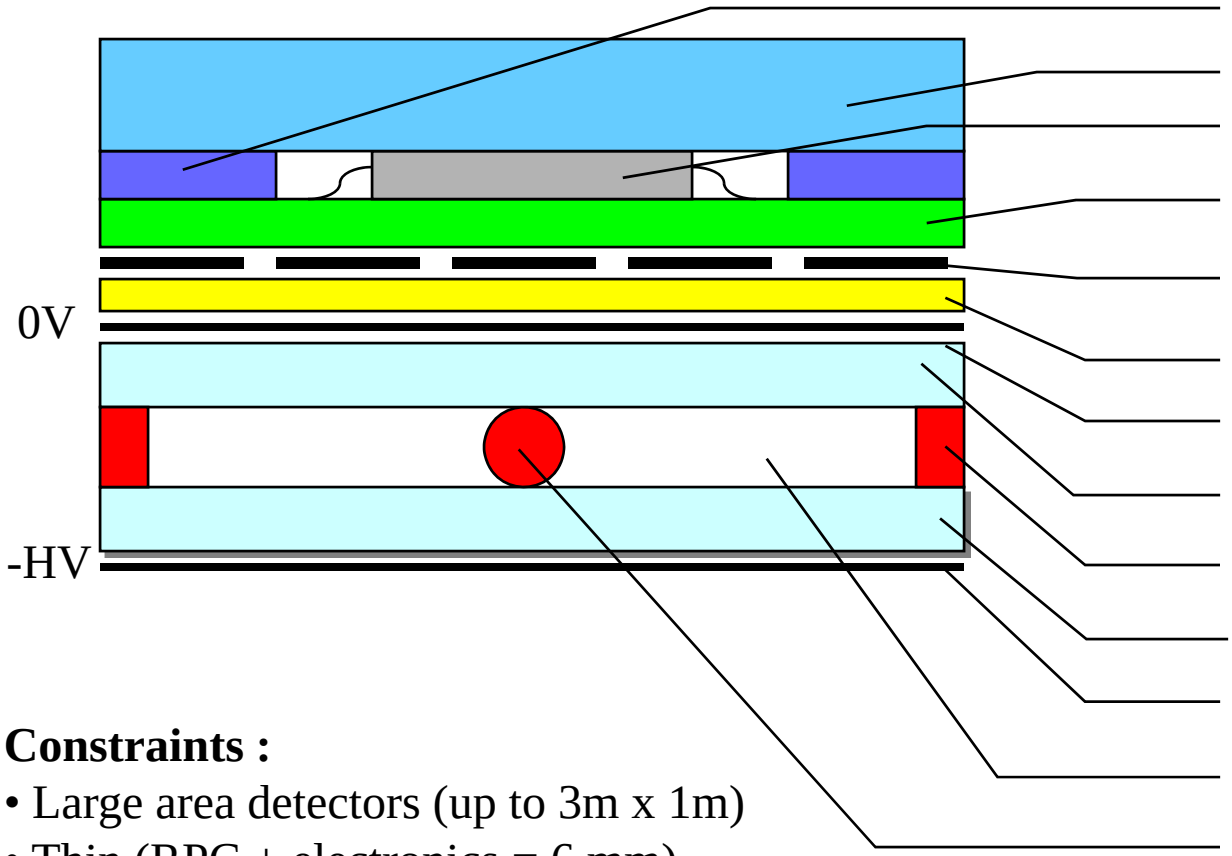
Glass RPC

- Very thin detector (< 3 mm)
- Efficient, cheap, well known from previous experiments
- No magnetic field effects
- High granularity (1cm^2 pads)

Electronics

- Embedded
- Thin (< 5 mm)
- Reduced connectivity to outside detector
- Very tight power budget

GRPC and semi-digital calorimeter -2
Detector proposed for ILD

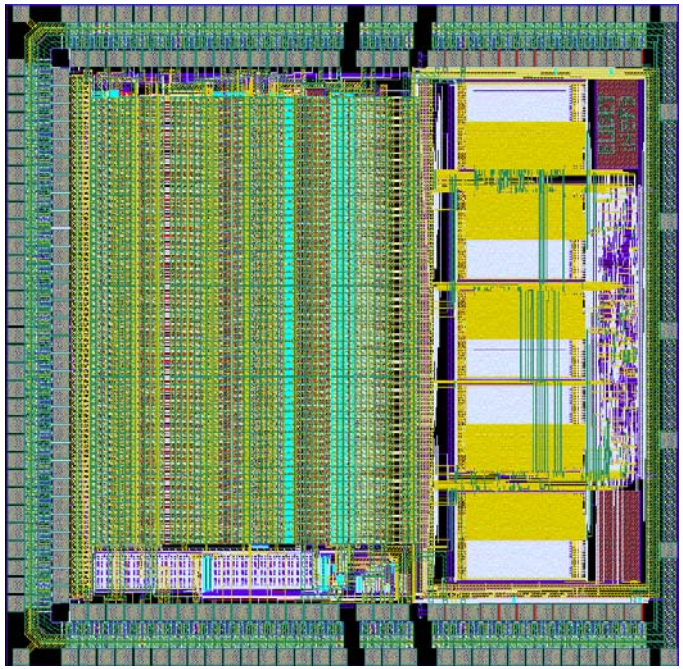


Grid (Steel)
Absorber (2 cm)
ASIC (HARDROC1)
PCB
Pads (copper, 1 cm2)
Insulation (Mylar)
Anode coating(~10 MΩ/□)
Glass plate (0.7mm)
Chamber wall (1.2mm)
Glass plate (1.1mm)
Cathode coating(~10 MΩ/□)
Gas
Spacer (ceramic ball)

Constraints :

- Large area detectors (up to 3m x 1m)
- Thin (RPC + electronics = 6 mm)
- Low cost
- Industrialized easily

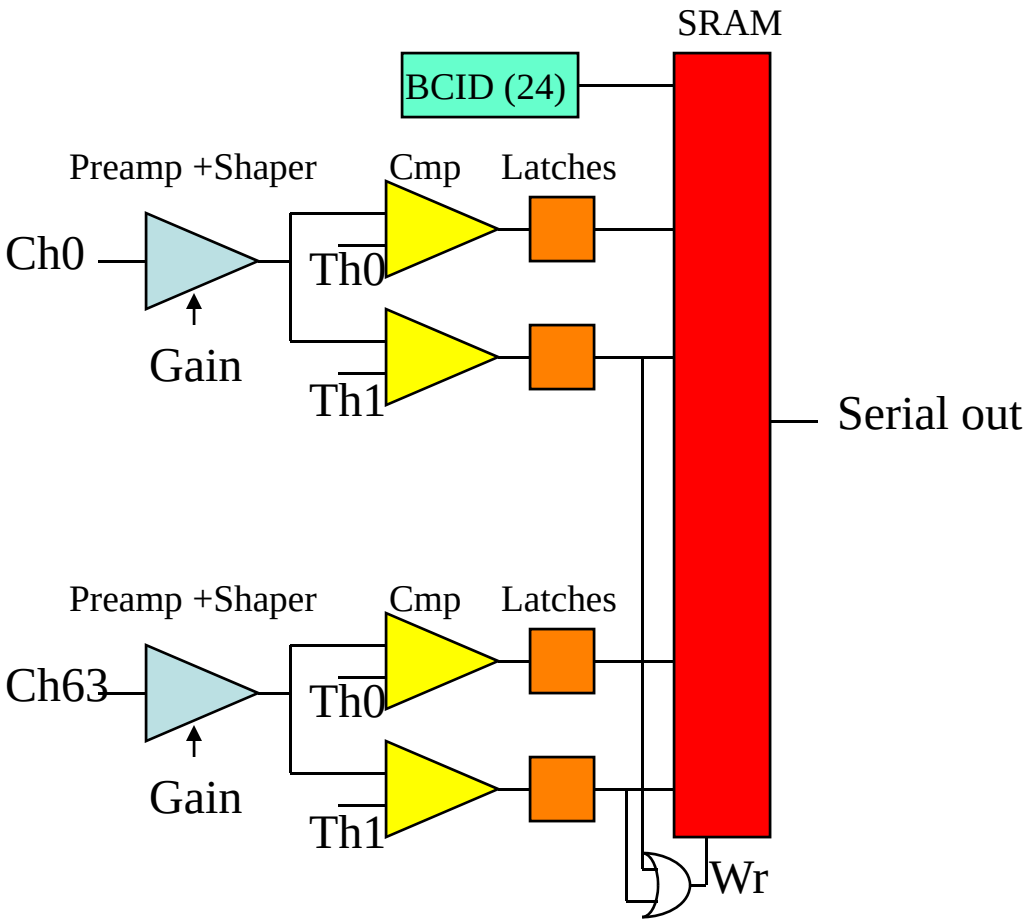
Glass RPC and (semi) digital calorimetry - 3
Hardroc v1 ASIC



Hardroc1 chip
(LAL - Orsay)

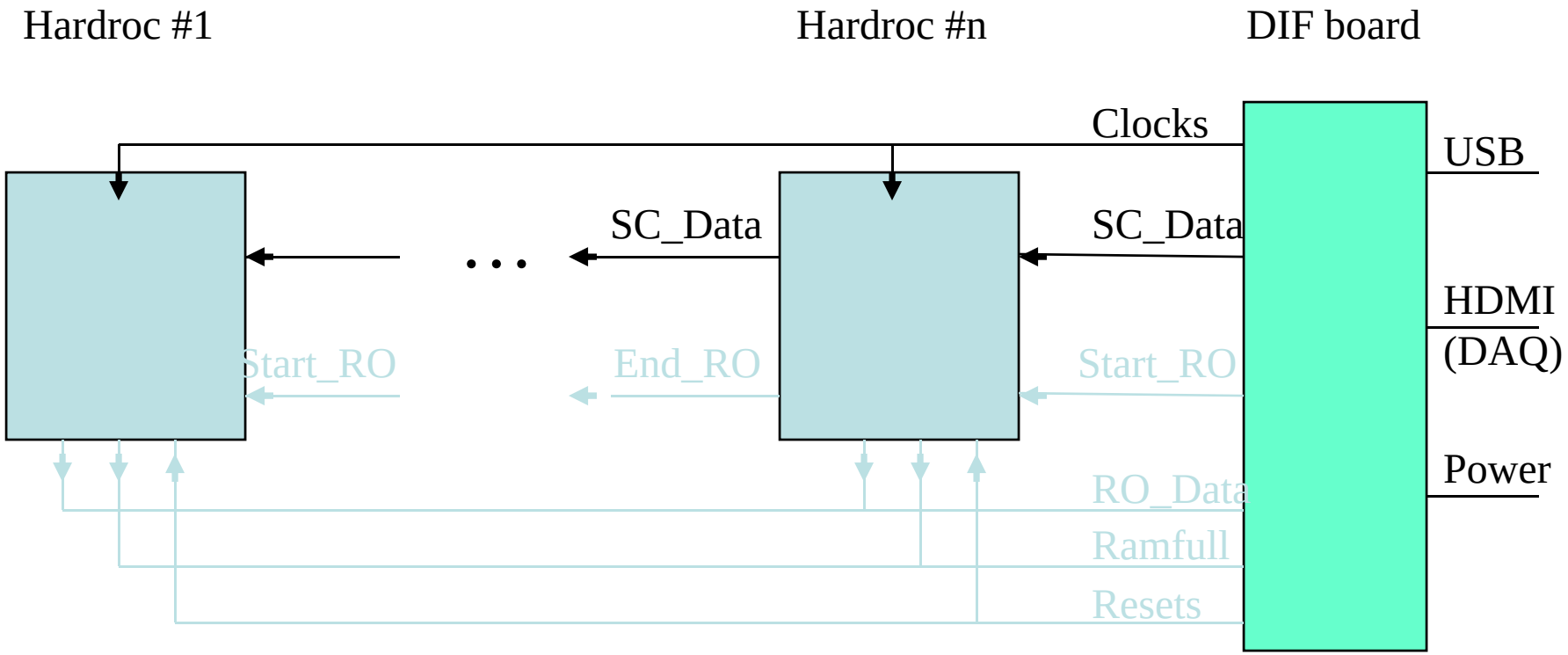
All parameters are programmed by slow control (serialized)

Memory depth = 128 events
64 channels
2 bits per channel



(Very) simplified view of Hardroc 1

Glass RPC and (semi) digital calorimetry - 4
ASICs slow control

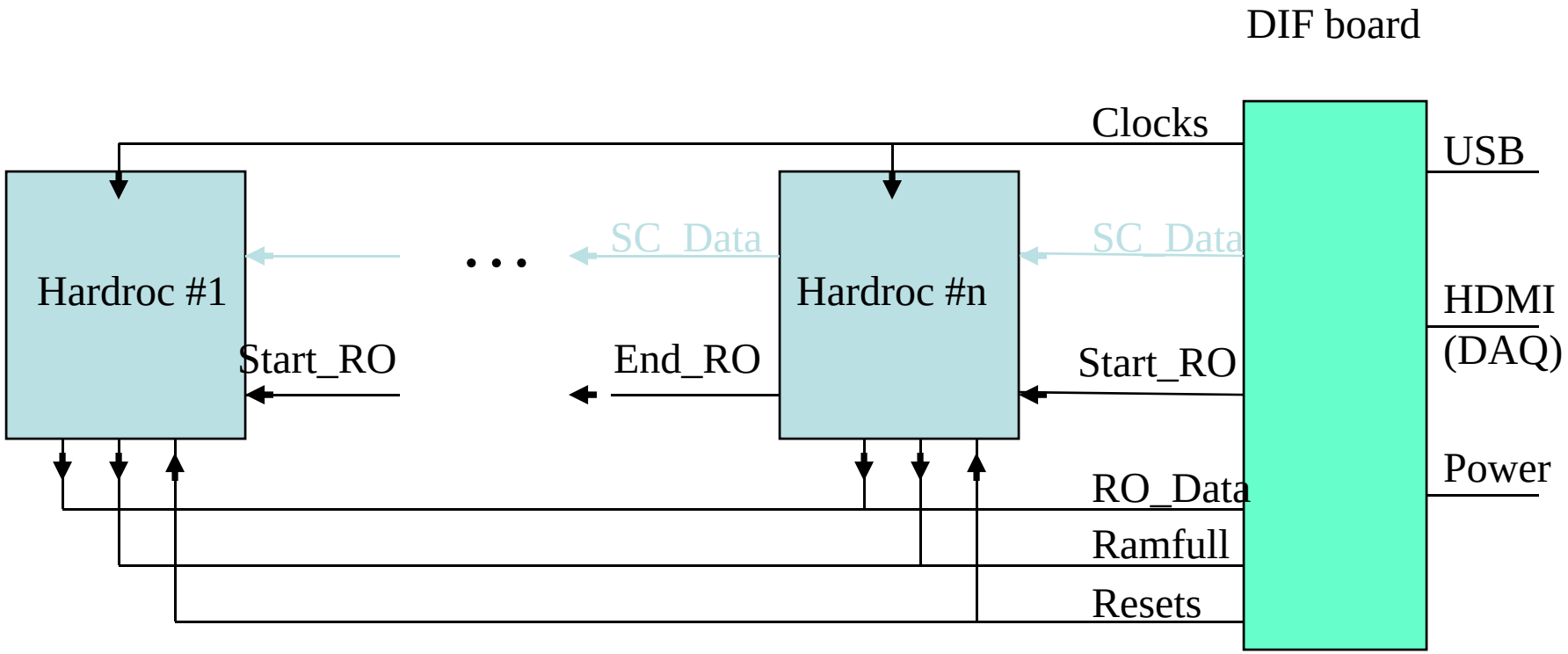


Slow control is daisy chained (shift registers)

Each Hardroc asic = 571 slow control bits

→ functions enable/disable, gains, thresholds, DAC levels

Glass RPC and (semi) digital calorimetry - 5
ASICs digital readout



Digital readout is chained (open drain lines)
Each ASIC can be externally or internally triggered
Each ASIC has an internal BCID counter to time stamp each recorded event

Glass RPC and (semi) digital calorimetry - 7
View of one chain

1 m = 1 slab = 48 Hardorc ASICs

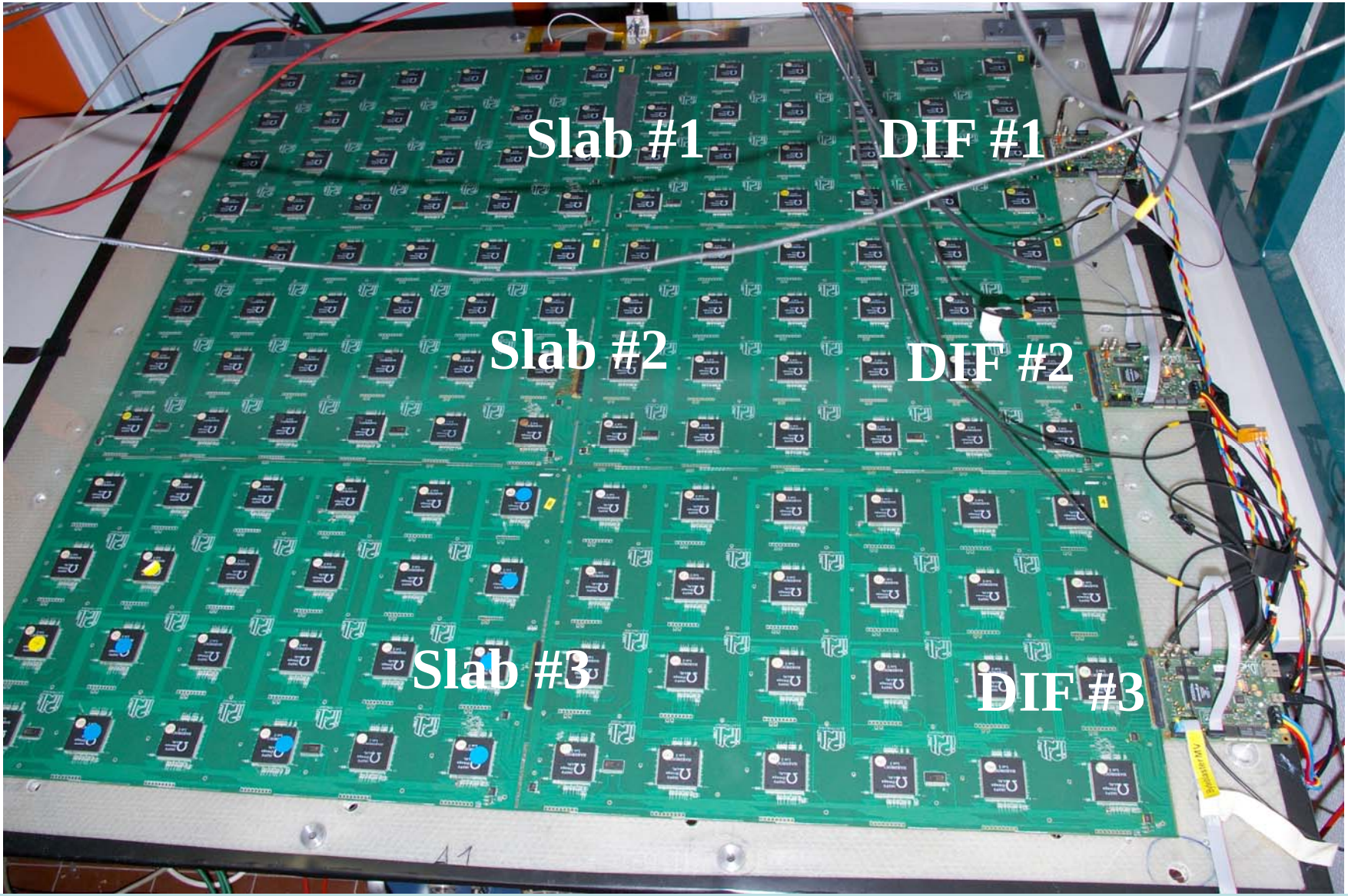
PCB 1
24 hardrocs
(IPNL - Lyon)

PCBs connected with
0 ohms resistors (and
aluminium tape…)

PCB 2
24 hardrocs
(IPNL - Lyon)

DIF board
(LAPP - Annecy)

Glass RPC and (semi) digital calorimetry - 8
1 m2 of equipped detector



DAQ presentation

Developed within the Xdaq framework

(https://twiki.cern.ch/twiki//bin/view/XdaqWiki/WebHome)

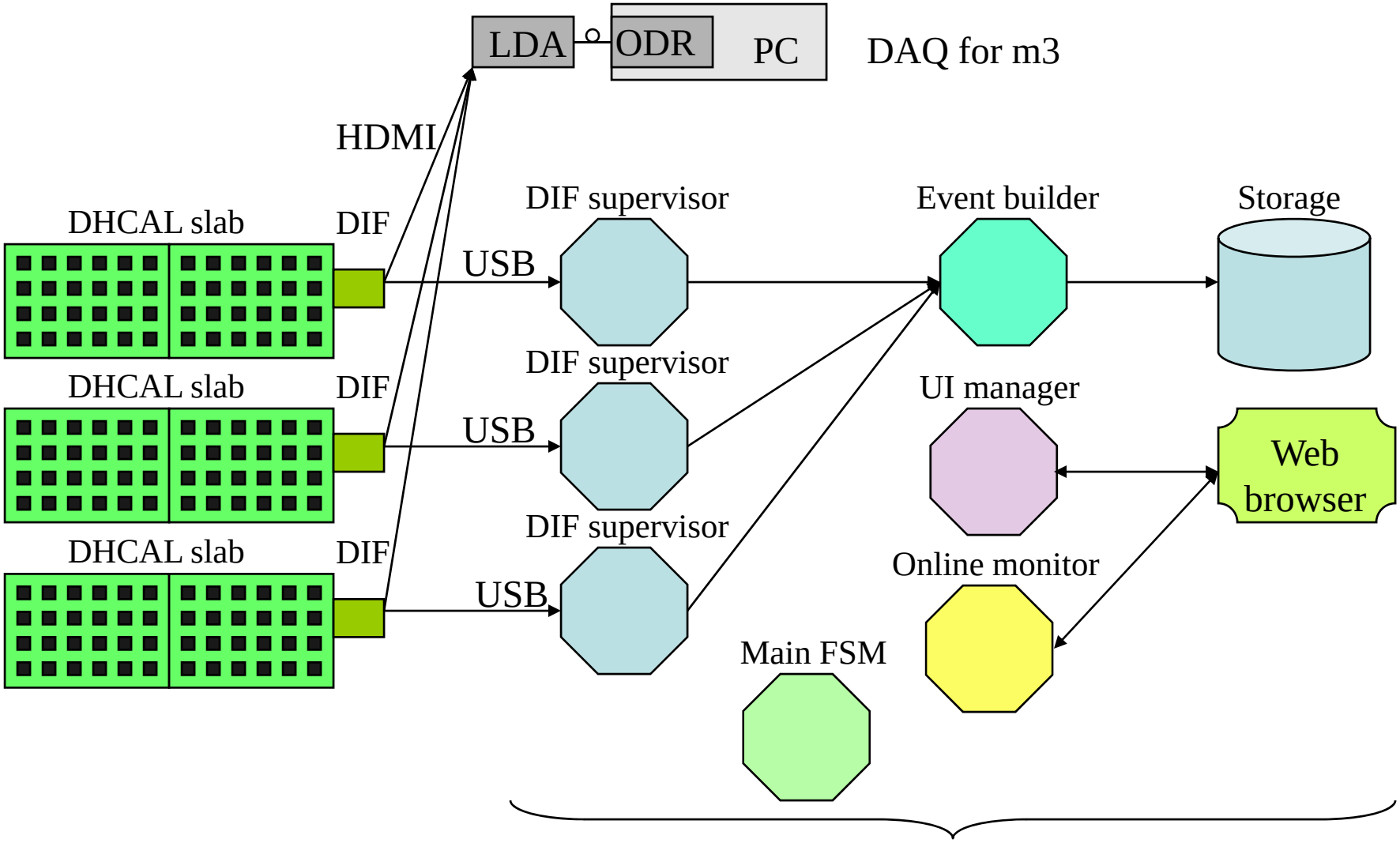
Running on one or several DAQ PCs (running on scientific linux 4)

User interface is a web page

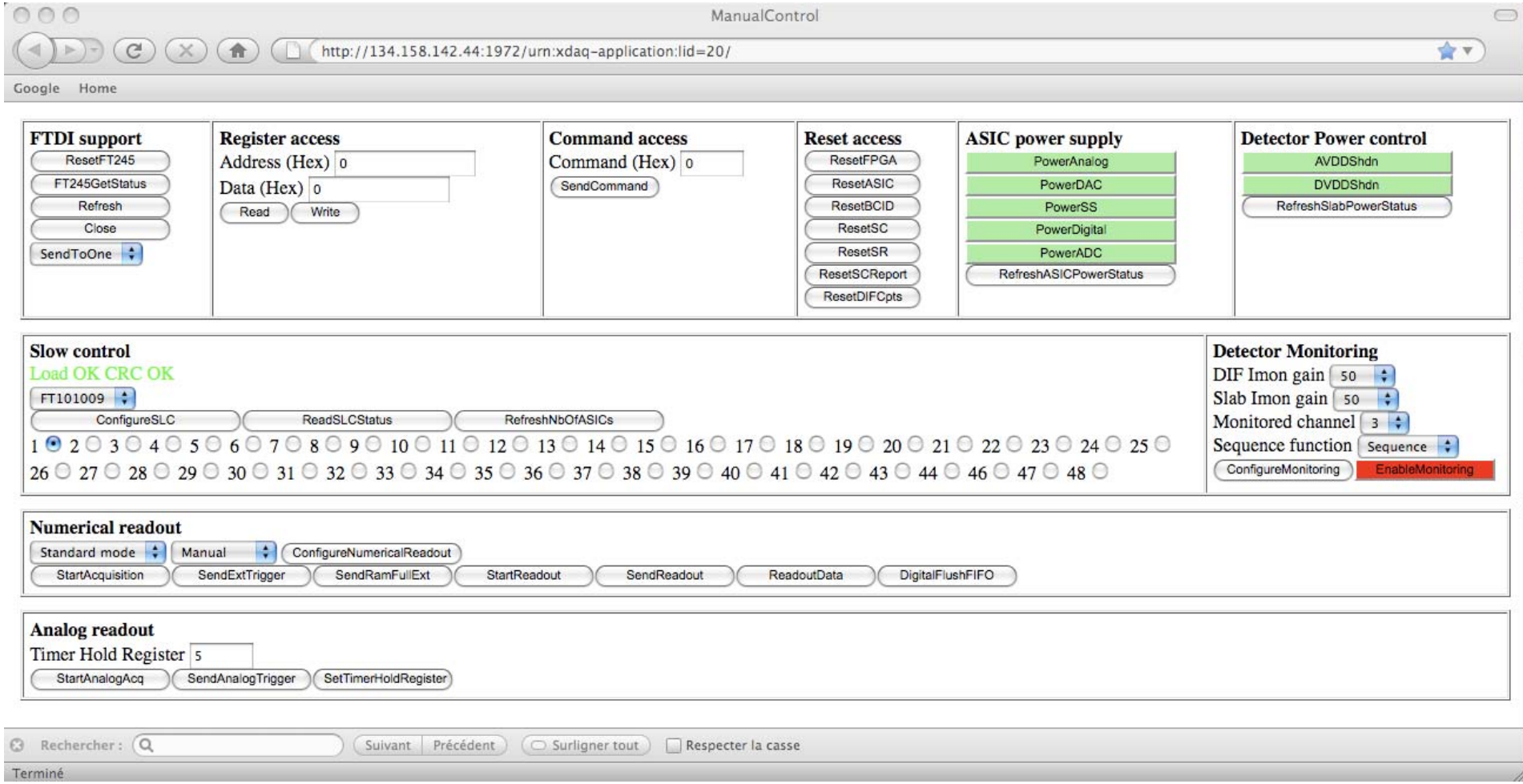
Can be easily accessed from any PC in the network (ie DAQ PC(s) in experimental area and laptop(s) in control room)

Security procedures and access restriction can be obtained with standard network tools

DAQ
Schematic view



DAQ
sample screen shot (manual mode)



DAQ capabilities

3 modes to operate the DAQ :

• *Manual mode* : all functions, commands and registers of one or several DIF(s) are accessible one by one (mainly used for debug purpose)

• *Semi Automated mode* : More complex functions of one or several DIF(s) can be performed, ie send slow control, start acquisition

• *Automated mode* : All behavior is driven by main finite state machine

2 trigger modes :

• *Standard mode* :

Hardrocs store data on the external trigger
Data are sent to the DAQ PCs when RAM is full

• *Beamtest Mode* :

Hardrocs store all valid data (internally autotrigged)
Hardrocs stop storing on external trigger (i.e. common stop) and send data to DAQ PCs

DAQ
Data format

data format version (8b) ← Today version 4

timestamp (32b)
millitm (32b) } ← Time and date (millisecond precise)

global Header (0xB0)
DIF ID (8 bits)
DIF Trigger counter (32 bits,MSB first) ← Triggers that arrive when DIF is not busy
Acq Trigger counter (32 bits, MSB first) ← Triggers that arrive when Software is not busy
Global Trigger counter (32 bits, MSB first) ← All Triggers
Time DIF (24 bits , MSB first) ← BCID-like counter inside DIF
{
  Beginning of frame : Frame_Header = 0xB4 (8 bits) ← Tag
  {
    Hardroc Header : 8 bits
    BCID : 24 bits (3 bytes)
    Data : 128 bits (16 bytes) ← 2 bits per channels, 64 channels
  } --> Sent i times according to status of memory of current Hardroc chip (max = 128)
  End of frame : Frame_Trailer = 0xA3 ← Tag
} --> Sent j times according to number of Hardrocs with data
Global trailer (0xA0)
CRC (16 bits) ← Cyclic redundancy check

Functional, convenient for tests but needs to be a bit more complex for long term runs (slow control parameters in the header, precise time stamp …)

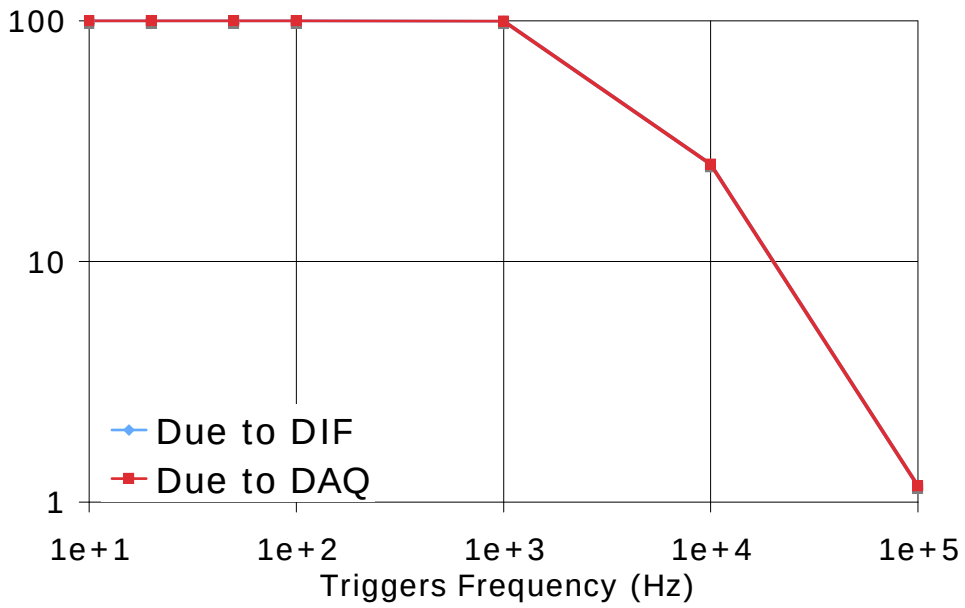
DAQ Test

The 3 counters in each data frame's header can be used to evaluate electronics and DAQ efficiency (in beam test mode) :

Global trigger counter (GTC) : Counts all triggers received by the DIF

DIF trigger counter (DTC): Counts triggers received when the DIF is ready to acquire

Acq trigger counter (ATC): Counts triggers received when the DAQ software is ready to receive data

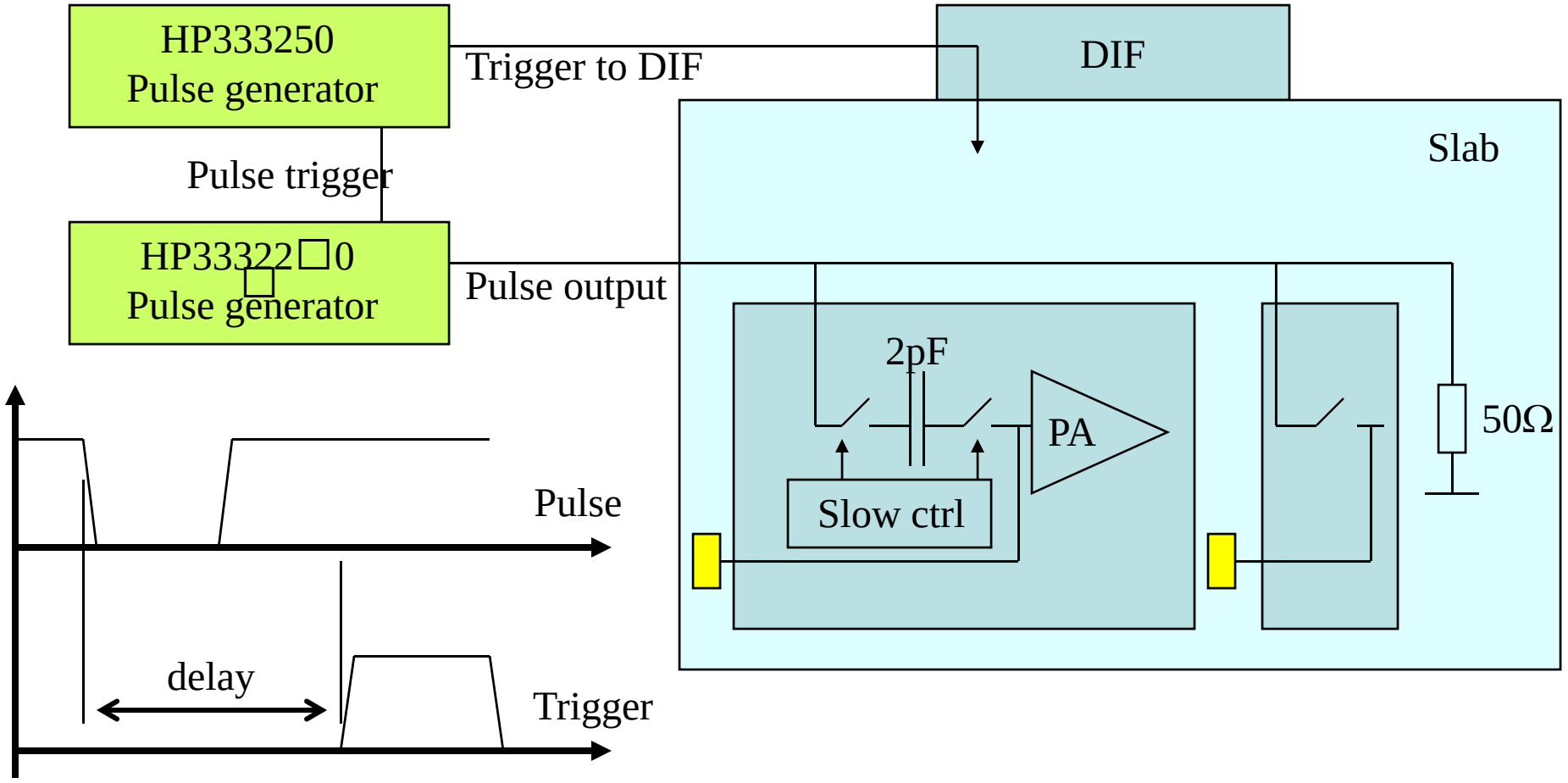


Conditions :
All channels of one ASIC are hit
Trigger is periodic (pulse generator)

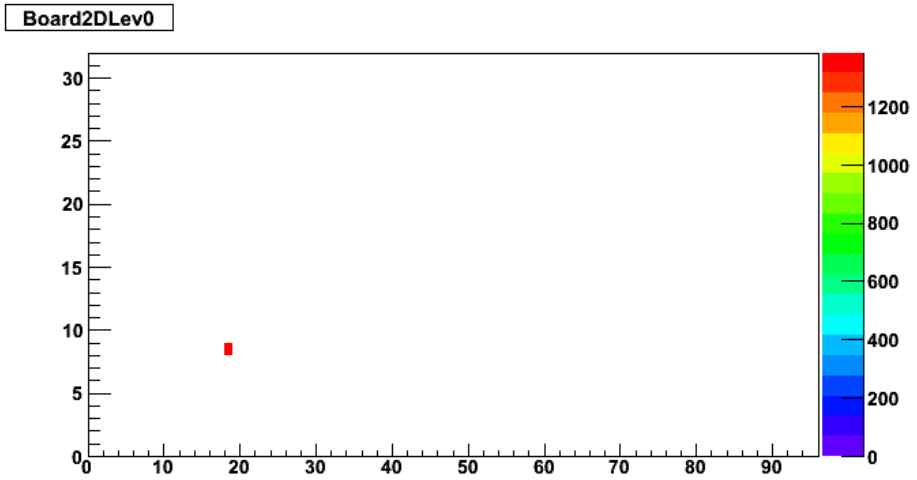
Transfer time :
170µs from slab to DIF
100µs from DIF to PC through USB (close to 1MB/s)
--> 3.7kHz limit due to data transfers

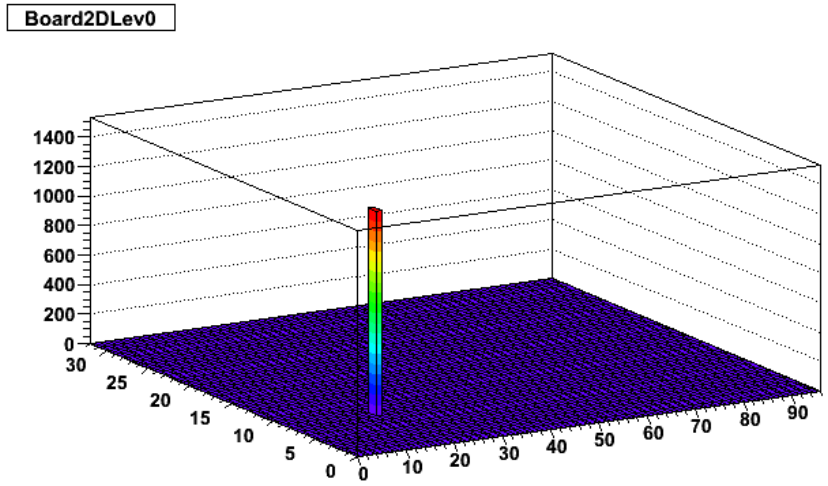
Injection with test capacitor functionality - 1

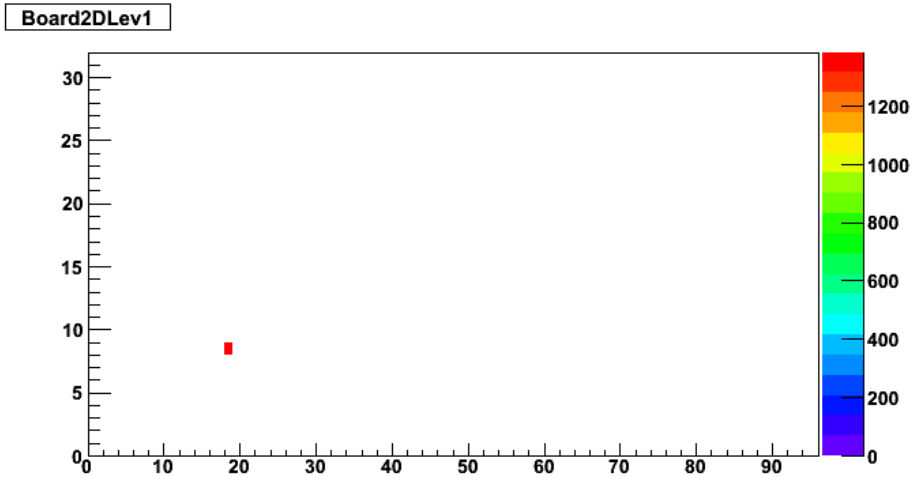
Each Hardroc has a test pin connected to an internal capacitor linked to each channel preamplifier input

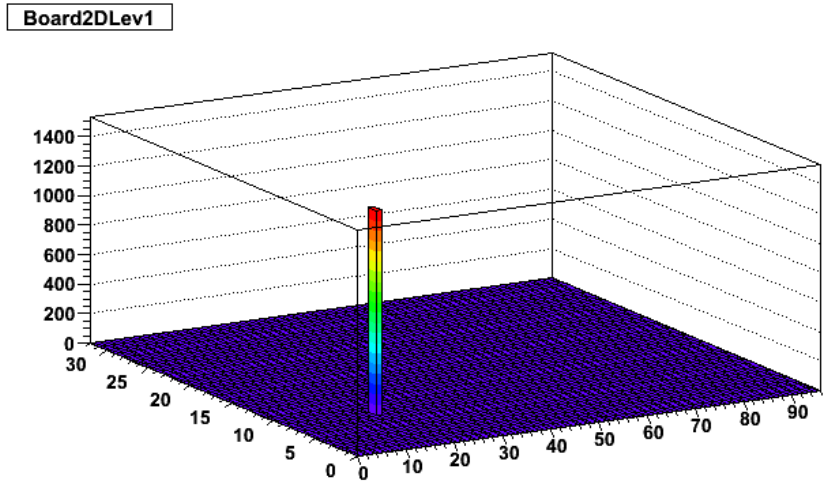


Injections with test capacitor functionality -2



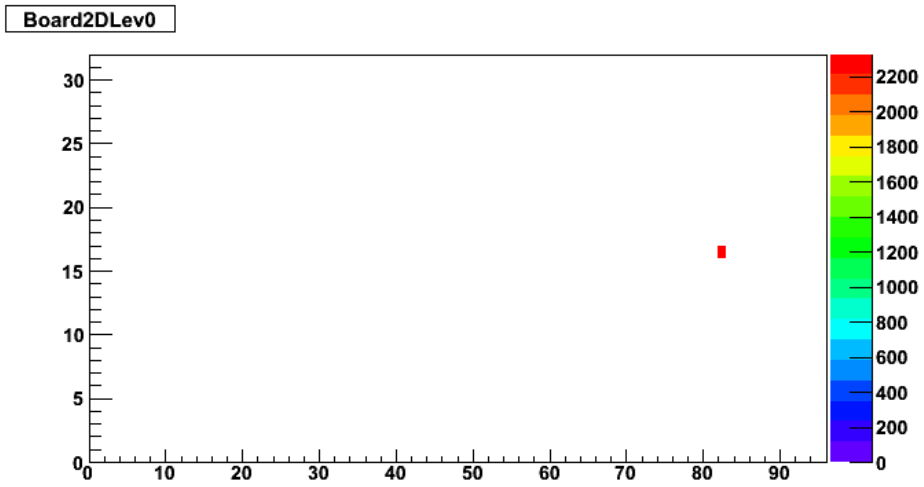


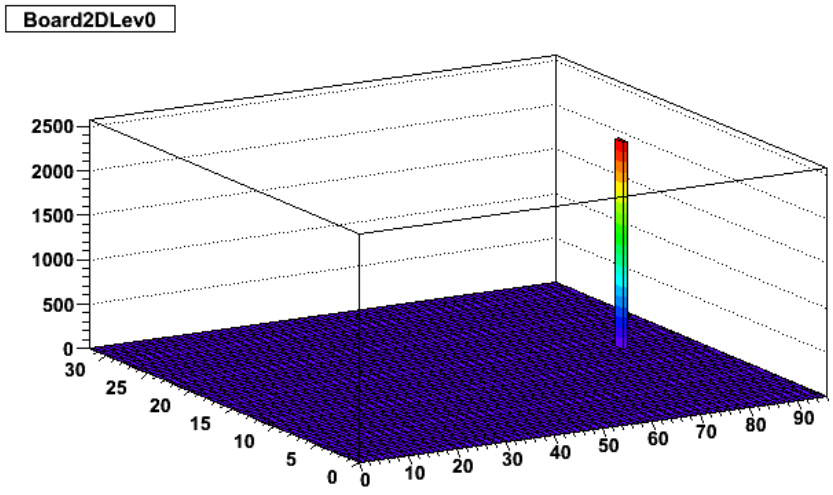


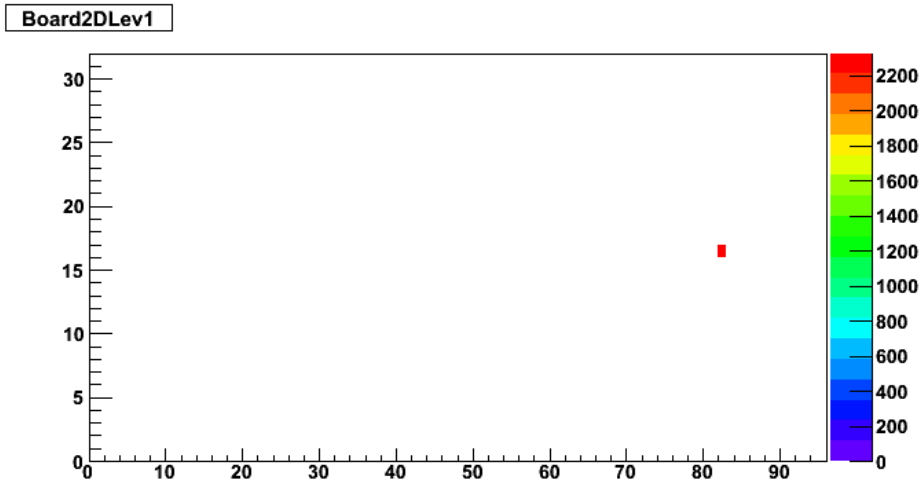


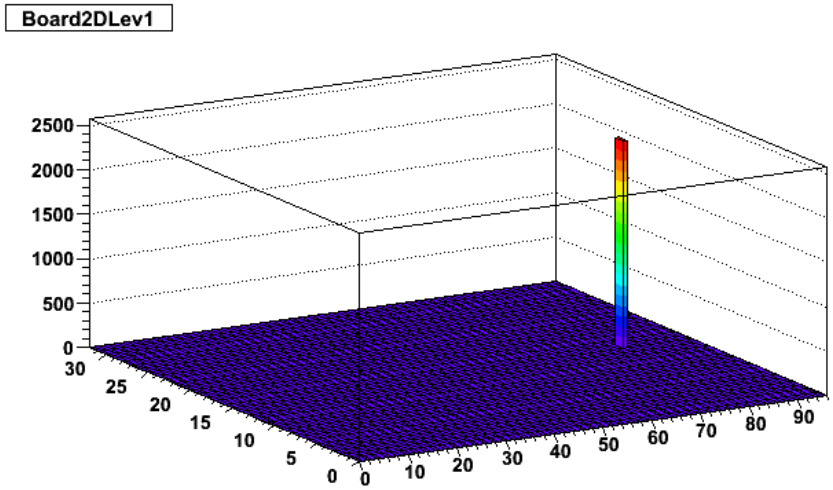
Hardroc 11 has been hit on channel 1
Charge injected is 3.2pC (1.6V on 2pF)

Injections with test capacitor functionality -3



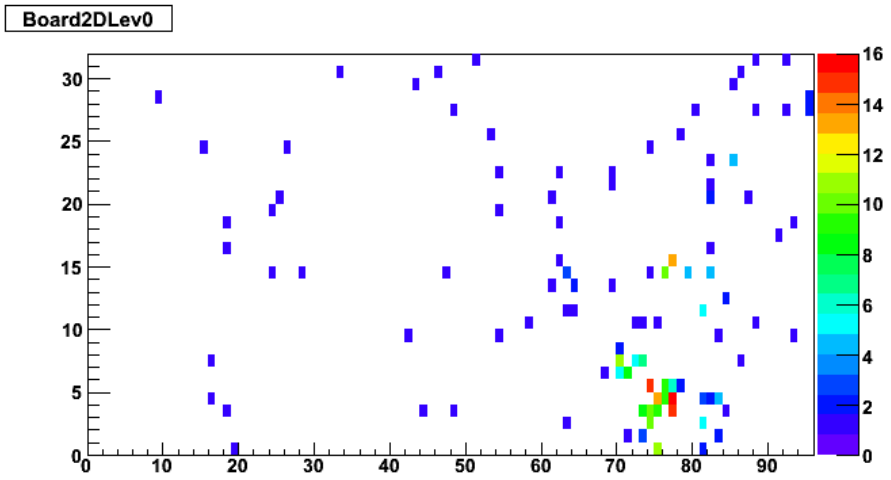


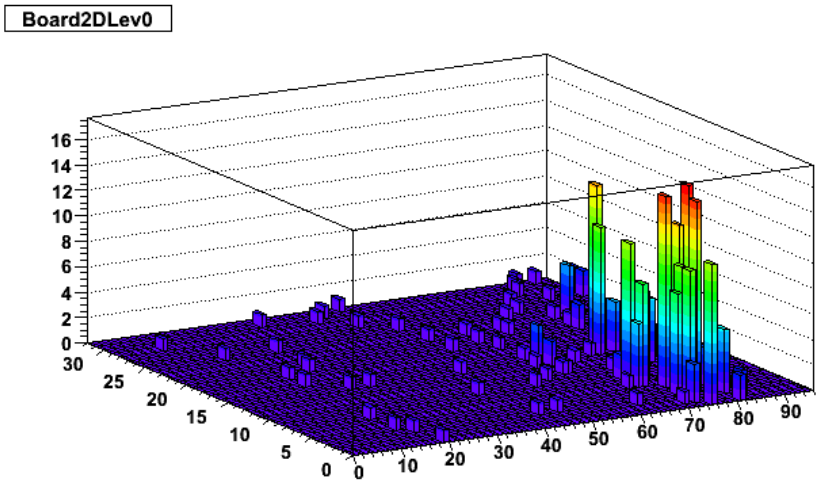


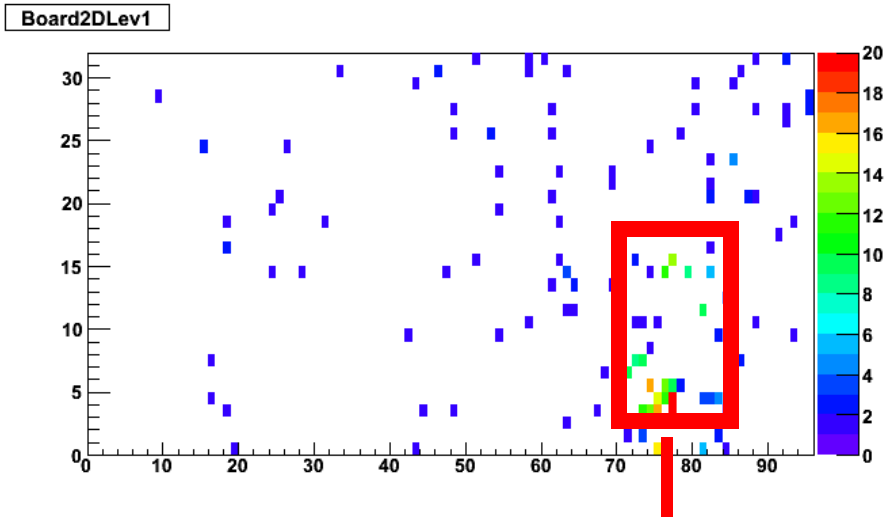


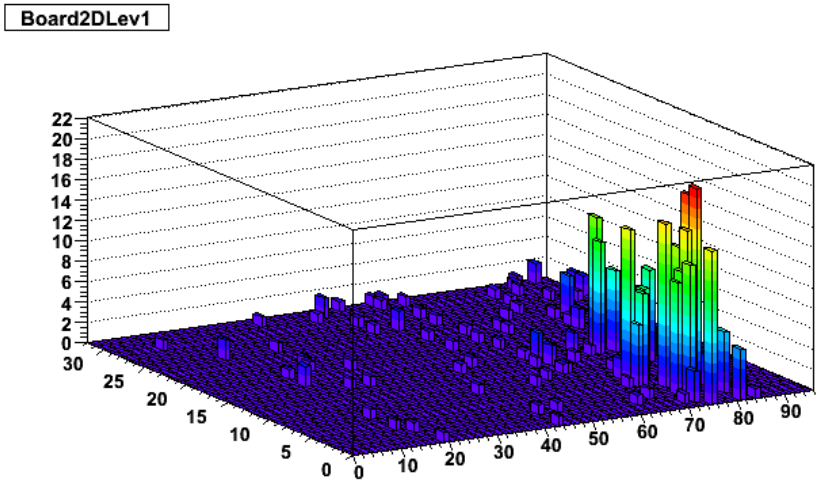
Hardroc 42 has been hit on channel 1
Charge injected is 3.2pC (1.6V on 2pF)

Cosmic run taken one 1 slab









Area covered by Photomultiplier
used for cosmic trigger

What next?

We have a stable and reliable setup with :
A 1m2 GRPC detector
A 1m2 readout electronics
A DAQ software successfully running and stable overnight

In the very near future :
Test , test and test again to eliminate every bugs
Go to CERN for a beam test in june
Develop useful but not vital functionalities (advanced online monitor, database for ASICs configuration)
Perform extensive cosmic tests

Afterwards :
Implement support for Hardroc2
Test power pulsing
Go for the m3!

Thank you for your attention

Backup slides

ASICs calibration - 1

Aim : Adjust thresholds according to each channel pedestal

Reduce dispersion

Mean : Inject a known charge to each input of each ASIC and record the threshold at which an information has been stored in memory