SLAC ILC Damping Ring Kicker High Availability Modulator R&D Program

TILC09

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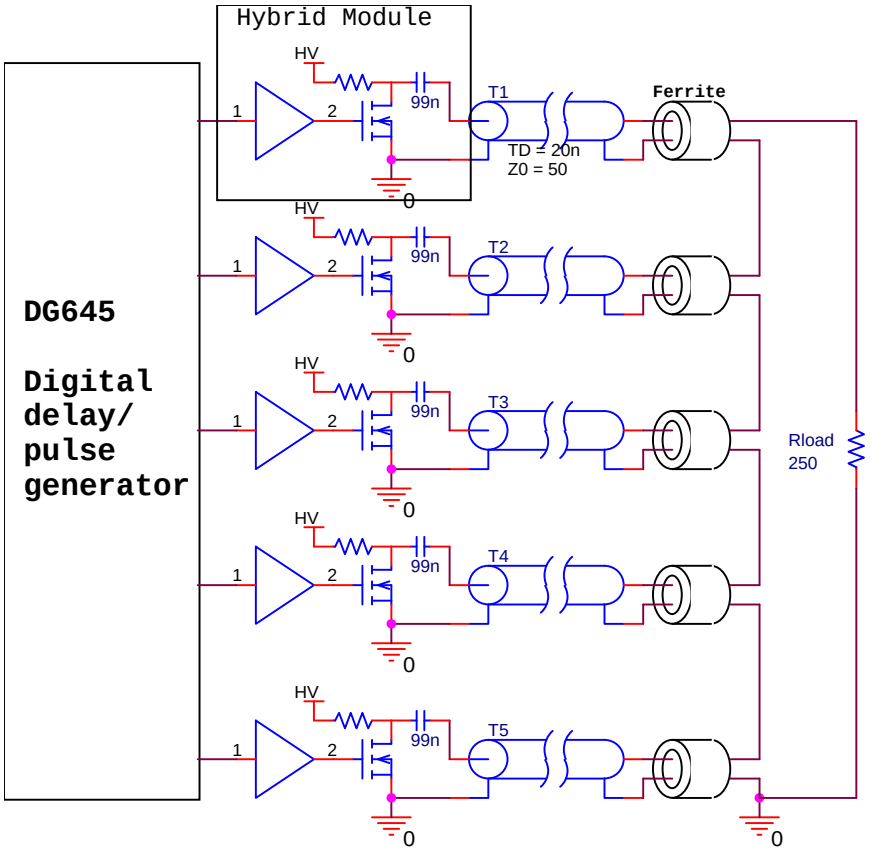
SLAC DR Kicker Modulator R&D

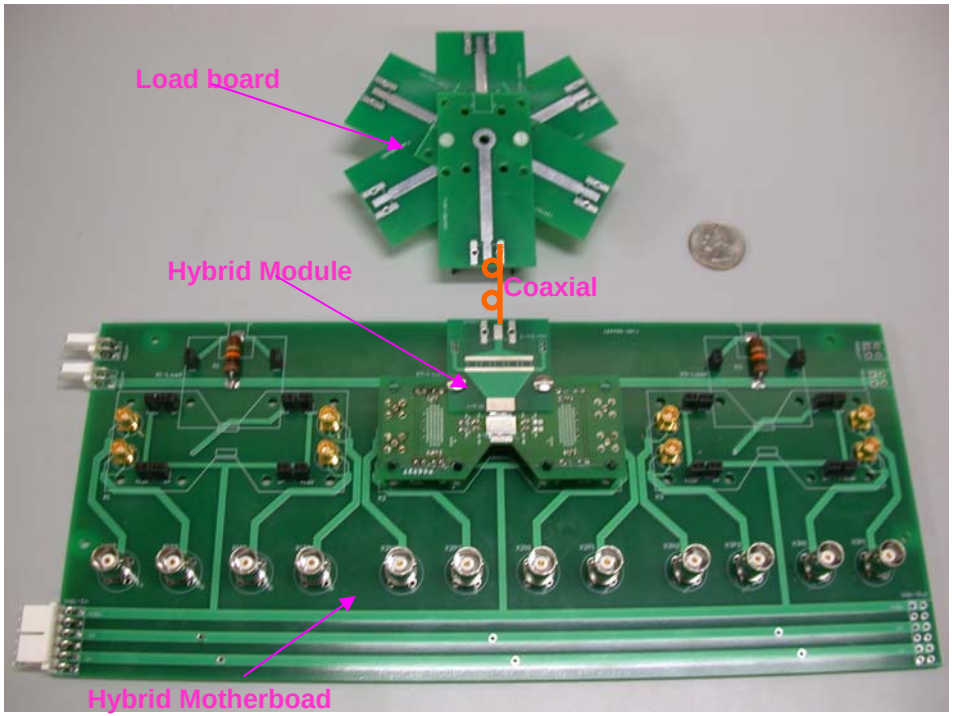
- SLAC program is investigating two approaches
  - Adder topologies: array ultra-fast MOSFET switches
  - Opening switch topologies: DSRD switch
- Adder Program
  - Hybrid MOSFET/driver
    - ~1 ns switching time (FY08)
    - Improve assembly technique
    - Evaluate thermal stability
  - Investigate high bandwidth adder topologies
    - “Scale assemblies” using MOSFET/Driver hybrid switches
    - Verify preservation of pulse fidelity
    - Inspect for reflections/residual energy
- Opening Switch Program
  - Functionally similar to DSRD systems marketed by FID GmbH
  - “Open source” design
  - 2-ns prototype demonstrated (FY08)
  - Developing 4-ns modulator for ATF2

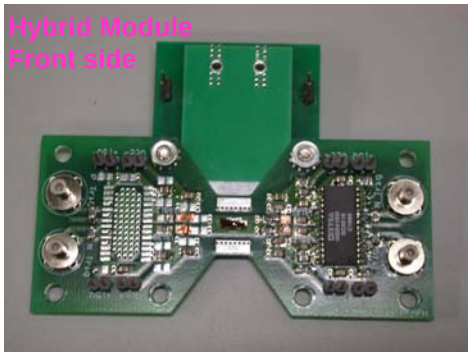
High Bandwidth Adder Test

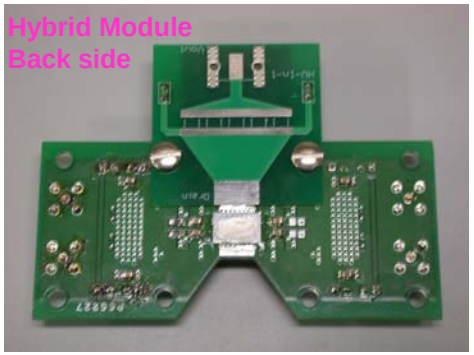
- Transmission line (TL) adder configuration
- Inductive isolation (alternative inductive adder configuration)
- Modules incorporate MOSFET/driver hybrid
  - 1 kV
  - 50 Ω
  - ~1 ns switching time
- 5 stages
- Output
  - 5 kV (uni-polar)
  - 250 Ω
- Status
  - Undergoing assembly
  - Initial results at PAC09

TL Adder Assembly



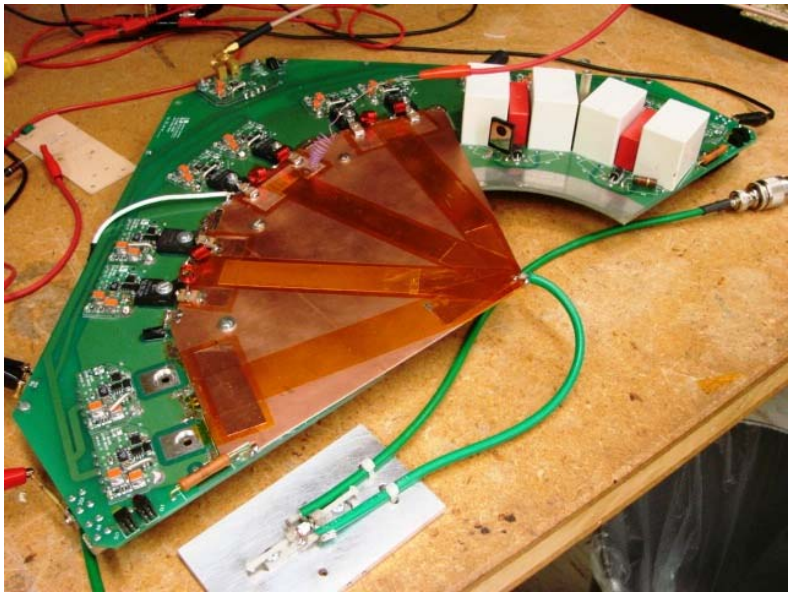


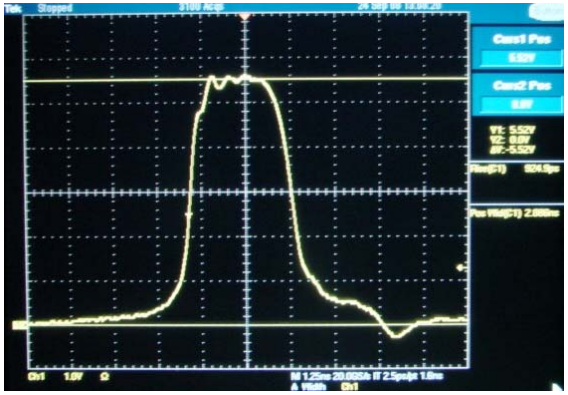




DSRD 2-ns Prototype Tests

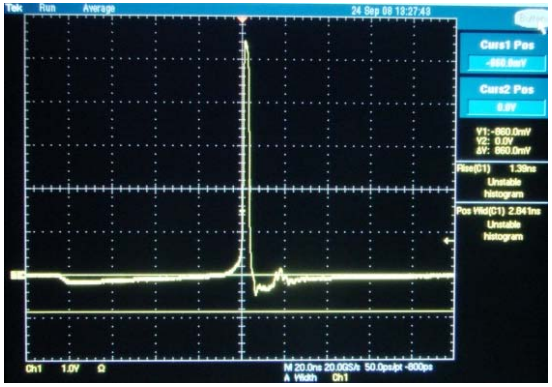
Amplitude	kV	4.4
Impedance of Feeder	Ohm	50
Rise Time	nsec	<1
Pulse Width	nsec	2.9





Waveform detail:

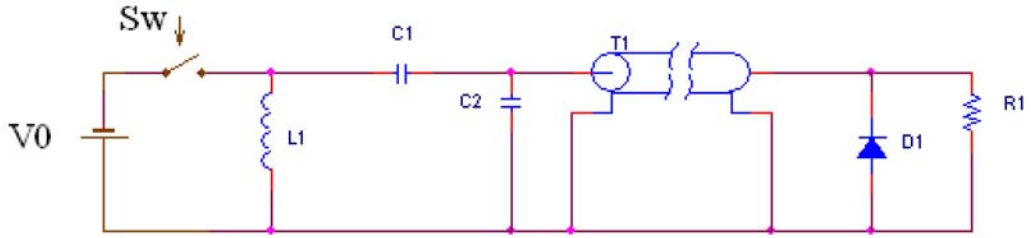
1.25 ns/div

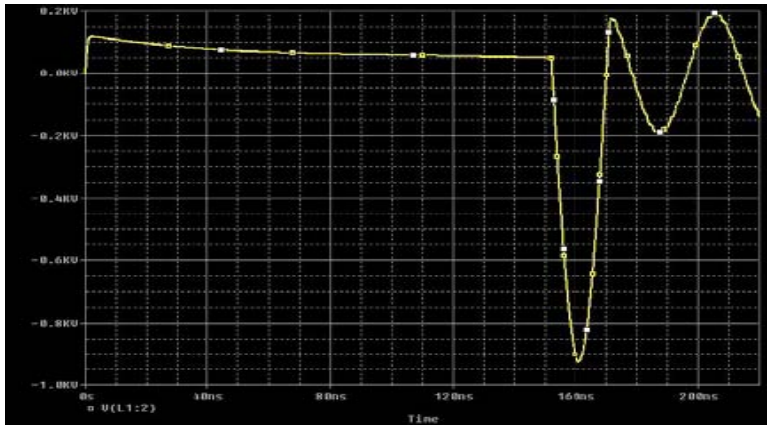


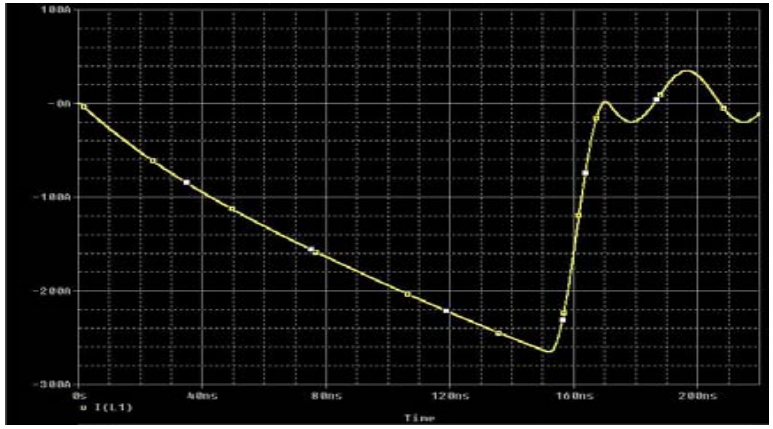
Pre/post pulse:

20 ns/div

DSRD Modulator Energy Transfer Sequence

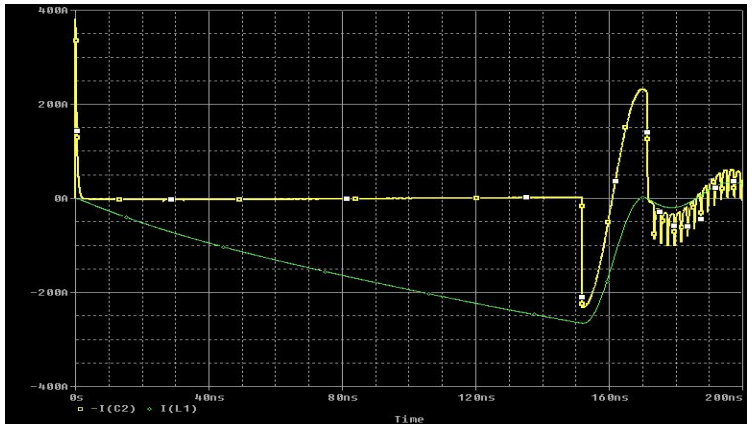




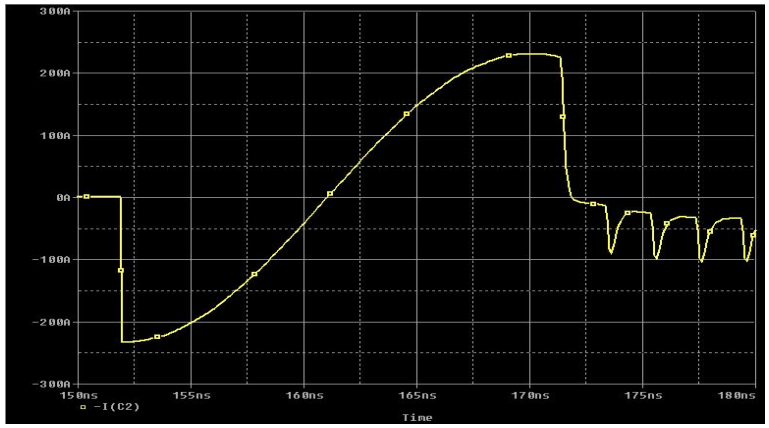


- Voltage (left) and current of L1 during charging period (SW closed)

DSRD Modulator Energy Transfer Sequence



(a)



(b)

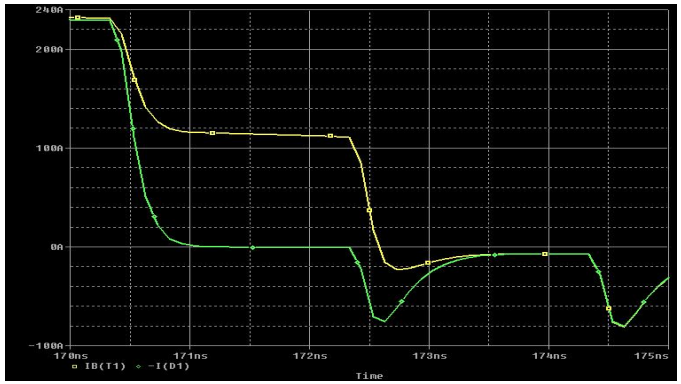
(a): Current in L1 (green) and C2 (yellow) during charging of L1 (t<154 ns) and transfer to T1

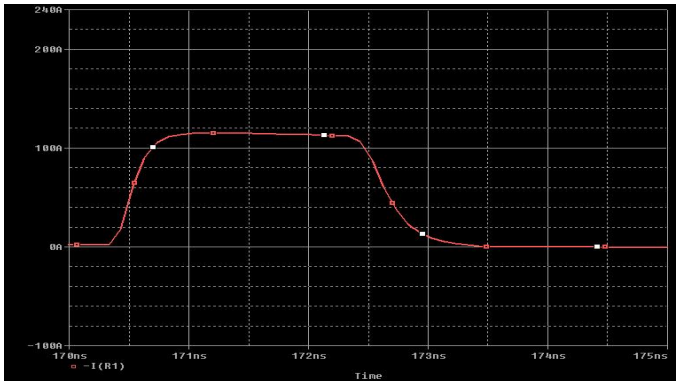
(b): Detail of C2 current during energy transfer to T1 (t<170.5 ns) and discharge into load, note current through C2 until halfway through T2 discharge (t=171.5 ns)

(c): D1 current (green) and T1 current, load end, (yellow)

(c)

DSRD Modulator Energy Transfer Sequence



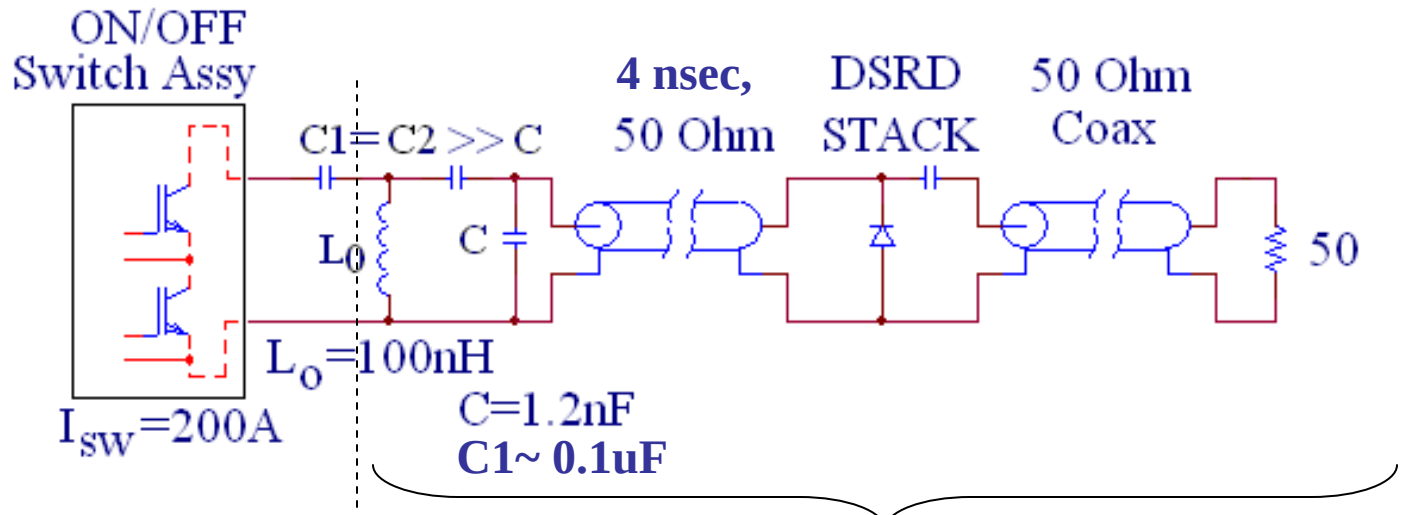


- Detail of D1 current (green) and T1 current, load end, (yellow) during transfer of energy to load (above right)
- Load current during discharge of T1 (above left)
- Challenges
  - Pre-pulse: finite DSRD turn-on time and forward-voltage
  - Post-pulse: residual energy will “bounce around” and come out at later time
  - Optimum timing dependent on precise DSRD properties that depend are temperature dependent

ATF2 DR Kicker Modulator

- Parameters
  - Kicker: 60 cm, TEM, bi-polar
  - Output Voltage: ±5 kV
  - Impedance: 50 Ω
  - Pulse Length
    - Flattop: 4 ns
    - Rise/Fall Time: ~1 ns
  - PRF
    - Burst: 3 MHz (1/308 ns nominal, 1/313.6 ns every 3rd pulse)
    - Pulses per Burst: 30
    - Burst PRF: 1.5 Hz
  - Residual Voltage: <50 V (1% of max) after 103.6 ns
- Schedule
  - Brass Board: - 4/09
  - Prototyping: - 7/09
  - Modulator: - 12/09
  - Delivery to KEK: 2010

Circuit Modifications: 4 ns Output



Increase TL to 4 ns, re-tune to minimize pre/post pulse

MOSFETs Drivers

Storage Capacitors

Charging PS

Array of MOSFETs in series and parallel

Reliability of Switch Assembly

Recent Progress

- T. Naito visit to SLAC
  - ATF2 parameters
  - KEK participation
- Derived circuit parameters for 4 nsec flattop circuit
- Developed series MOSFET switch for HV pump
  - Opto-coupled trigger (floating deck)
  - Transformer coupled trigger
- Acquired key components

Summary

- Adder Program
  - Ultra-fast switching: hybrid circuit achieves fundamental MOSFET limit w/ excellent control
  - Scale adder system under assembly
  - Test results during Q3 (PAC09)
- DSRD Program
  - Promising results with 2 ns prototype
  - Purchased optimized DSRDs and other required components
  - Focusing on higher power pump development
  - Prototype development Q3/Q4