# Status of the DAQ

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- Overview of DAQ system
- Overall status
- Component-by-component status
- DAQ Software
- Procurement plan
- Summary, issues and detector requirements

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# Overview of DAQ system

**Detector Unit**: ASICs

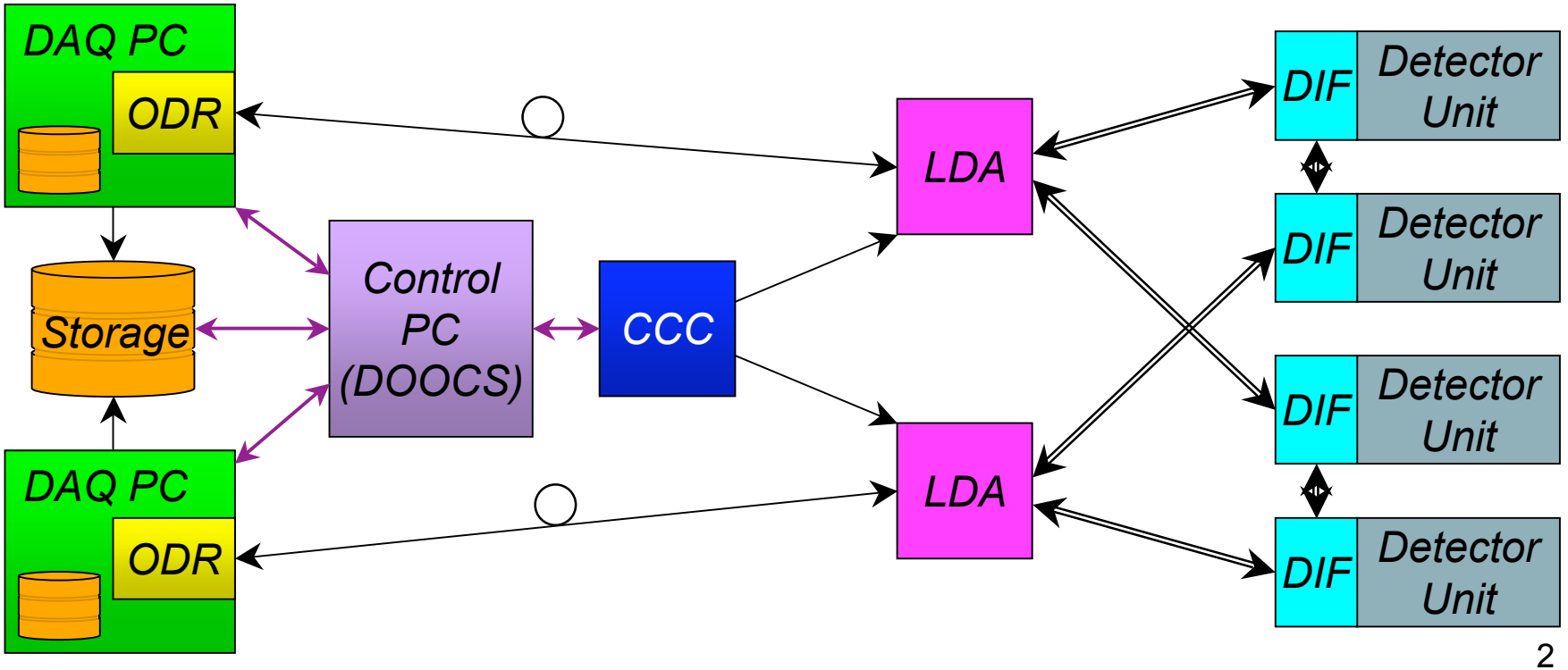
**DIF**: Detector InterFace connects generic DAQ and services

**LDA**: Link/Data Aggregator fansout/in DIFs and drives links to ODR

**ODR**: Off-Detector Receiver is PC interface

**CCC**: Clock and Control Card fans out to ODRs (or LDAs)

**Control PC**: Using DOOCS



# DAQ system links

- DIF ⇔ LDA
  - synchronous, serial link with additional asynchronous pairs. 8b/10b encoded data
  - runs at N*machine clk: frequency 5..150MHz (assume 100MHz)
  - HDMI cabling and connectors
- LDA ⇔ ODR
  - Gigabit Ethernet (and TLK2501) serial protocol
  - SFP cage connector supports optical fibre
- CCC ⇔ LDA
  - Compatible with LDA⇔DIF interface
  - CCC & DIF capable of stand-alone operation

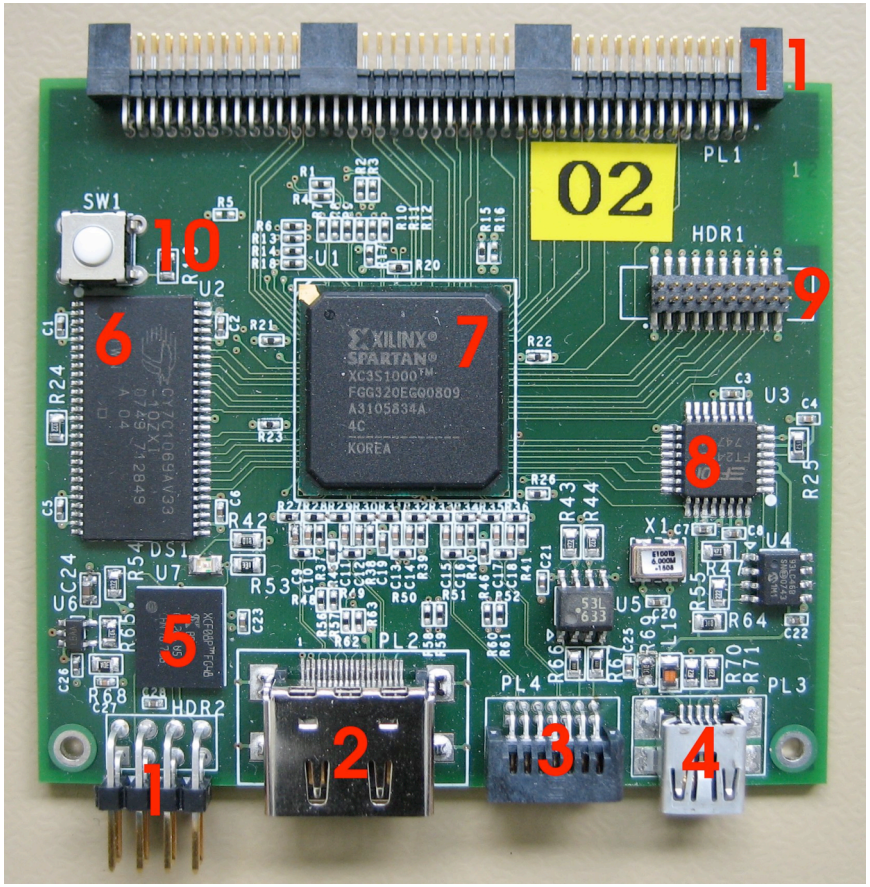
# Overall DAQ system status

- All hardware exists (independently), at different stages
- Firmware exists (independently), again at different stages
- Working on integrating components (at UCL) :
  - Links between the LDA and ODR
  - Links between the DIF and LDA
  - Generating data and sending across with some success
  - Getting all components to the same stage of readiness
- Progress on use of DOOCS as DAQ software
- Have been planning procurement of full system(s)
- Producing a lot of documentation

https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQ

# Detector Interface Card re-spin

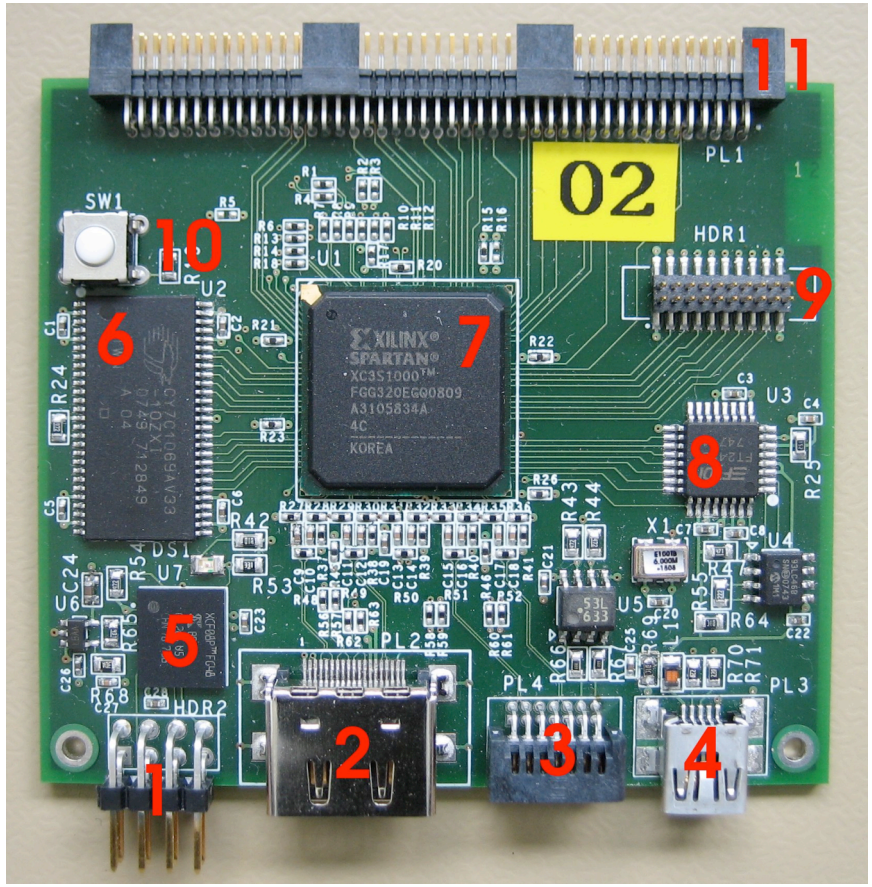
- Have 2 working prototype DIFs for test purposes.
- More can be made (have the parts).
- Board being re-spun for final EUDET version:
  - simpler, cheaper and smaller
- Dimensions 73 × 50 mm$^2$
- Should send out for manufacture of full complement of ECAL DIFs next week
- Then move onto intermediate board design



# Detector Interface Card changes

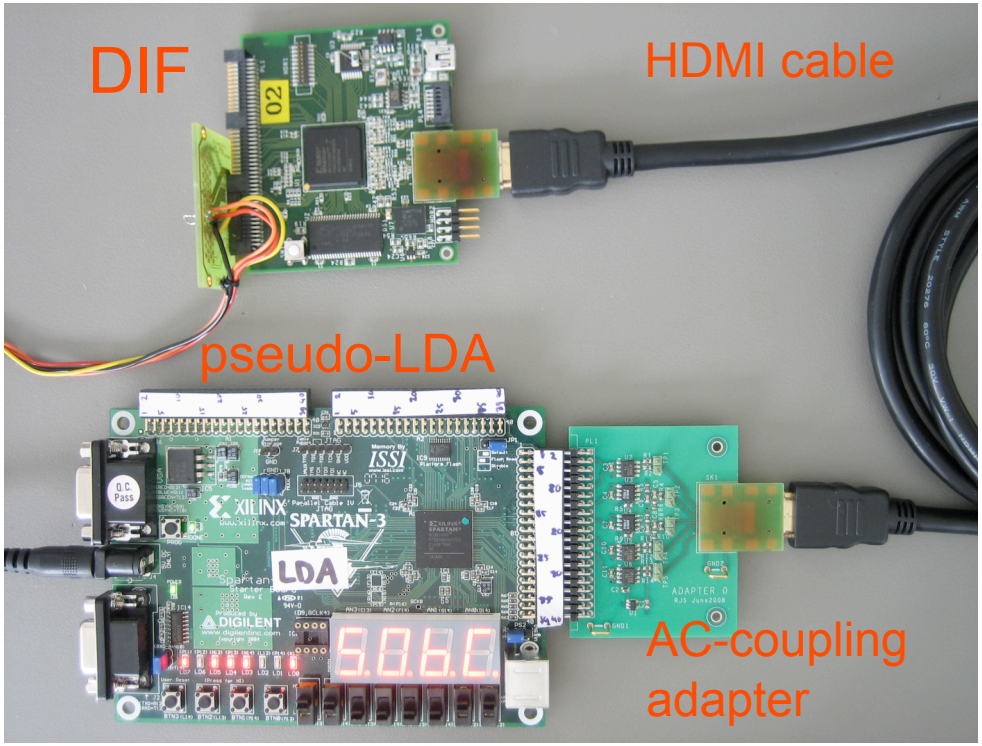
- No external SRAM (6)
- No user connector (9)
- No reset button (10)
- SPI-flash PROM (5)
- Flash RAM for VFE config

- USB kept but could be removed if space problems (4,8)



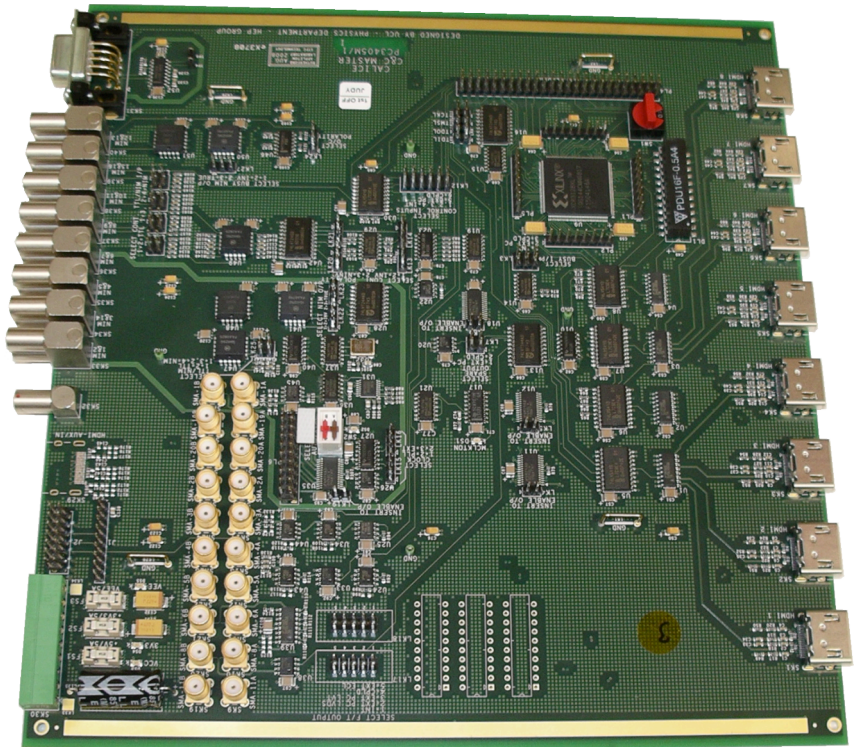
# DIF–LDA link

- Written data generator to send data to (pseudo-)LDA
- pseudo-LDA sends CLK & 8b/10b data @ 100MHz over AC-coupled LVDS lines
- Standalone DIF/pseudo-LDA system works
- Take to UCL for further tests and integration (today)



# Clock and control card

- Two prototypes tested and fully functional
- Now being boxed, given power supplies
- A further eight have are in-house giving a full complement of 10.
- Firmware for tests written and more being developed :  not yet uploaded as not time-critical.



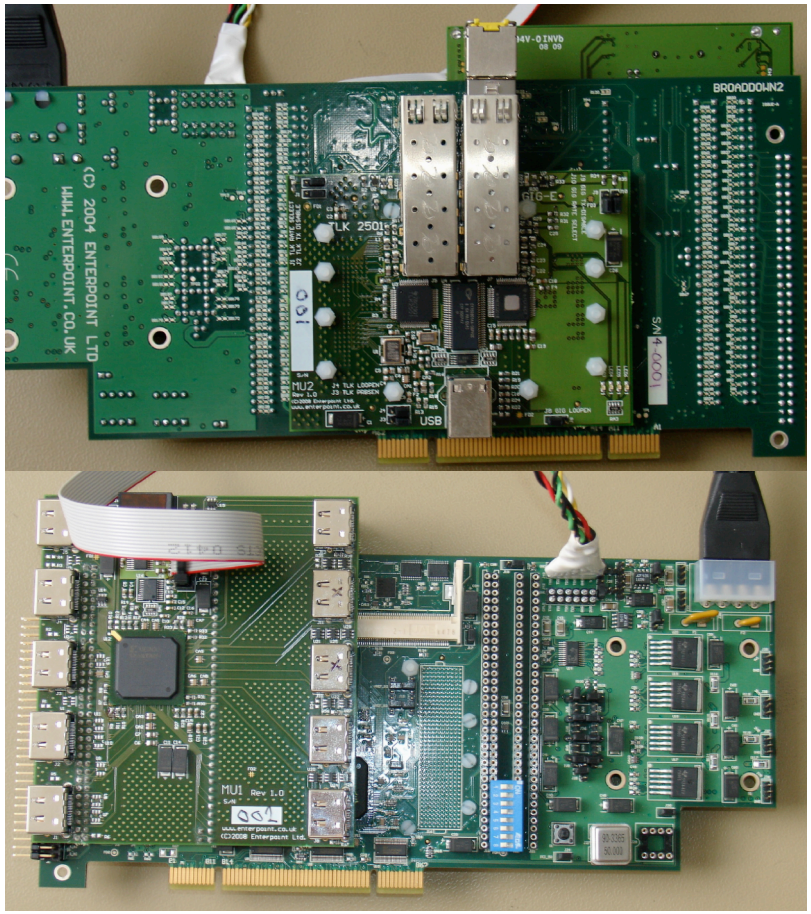
- Twiki page updated (test firmware) and an operating manual is written (not yet Twiki'ed).

https://twiki.cern.ch/twiki/bin/view/CALICE/ClockControlCard

- Interface to DOOCS being done

# Link Data Aggregator hardware

- LDA Hardware : Broaddown2 baseboard with add-on Gbit-eth and HDMI boards from Enterpoint.
- Several fixes to Gbit-eth and baseboard.
- Incorporated into new baseboard, Mulldonoch2.
- Expecting a board for testing anytime now.
- Assuming board works, then order full complement of LDAs. 8–10 weeks turnaround.

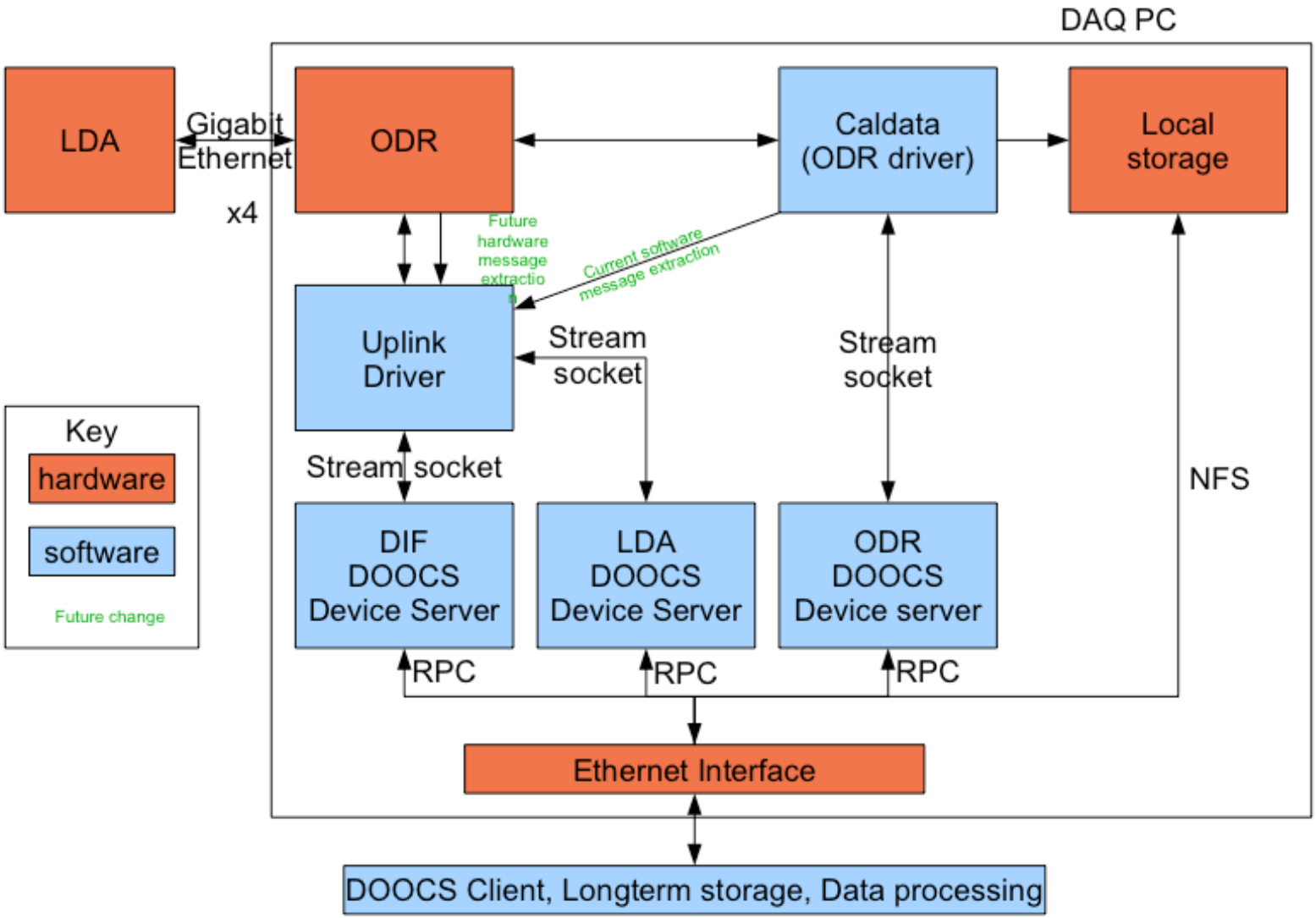


# Link Data Aggregator firmware

- Problems with hardware have not interfered with firmware development, e.g. DIF–LDA link.
- However, LDA essential for system tests : have ported LDA firmware in ODR (→ LODDAR) so we can start to build full chain.
- LODDAR ⇔ ODR data generator link advanced and being debugged.
- Extensive LDA documentation and firmware to download:

  https://twiki.cern.ch/twiki/bin/view/CALICE/LinkDataAggregator

# Off-Detector Receiver and DAQ PC



# ODR and DAQ PC

ODR

- XpressFX development board with Xilinx FPGA and PCIe link from PLDA
- 3 Virtex4 boards (V1) been working for a long time. Have 2 newer versions (V2) and 1 Virtex5 board. Assessing which board becomes standard platform.
- Problems getting V2 boards working which has delayed giving ODR+DAQ PC system to e.g. DHCAL.

DAQ PC

- Have 3 customised PCs with RAID arrays (not needed for simple lab tests)

https://twiki.cern.ch/twiki/bin/view/CALICE/OffDetectorReceiver

# DOOCS DAQ software

- Use of DOOCS as DAQ software maturing
- Previously:
  - Written device server for ODR
  - Controlling data flow through DAQ PC to ODR and LDA emulator
  - ODR and LDA client GUI interfaces
- Documentation:

https://twiki.cern.ch/twiki/bin/view/CALICE/CALICEDAQsoftware

# Current DAQ software activities

- Work concentrating on :
  - Configuration database making progress
  - CCC device server started
  - ODR state machine to start
  - Error/alarm handling done for ODR
- Will move onto when hardware development finished :
  - LDA device server
  - DIF device server
  - Full-scale state machine

# Procurement plan

- We need to provide enough components for beam-tests but also for some test-stands.
- Test-beam, a full calorimeter test, requires:
  - 30 DIFs → 4 LDAs → 1 ODR and DAQ PC with 1 CCC
- We will procure/provide
  - 30 + 6 (spare) ECAL DIFs and ECAL intermediate boards
  - 20 LDAs for 3 calorimeters + spares and 40 + spares SFPs
  - Have 10 CCCs for 3 calorimeters + spares
  - 3 + x (x>2) ODRs and DAQ PCs for 3 calorimeters + spares
- These numbers should definitely cover test-beam running and also have a reasonable number for lab-tests—we can't provide 20 ODRs to 20 labs!

# Summary, issues and detector requirements

- Within EUDET, to deliver working DAQ system by June 2009.
- Have started link/system tests : debugging and improving.
- No show-stoppers yet, on track for June2009, but some issues :
- LDA schedule is tight, but will hopefully be okay. However for detector tests, is the turnaround too slow?
  - Ask for faster production—expensive.
  - Can connect HDMI board to ODR and ODR acts as both LDA and ODR for small-scale tests.
- Different ODR versions need to be consolidated :
  - We can send the DHCAL a V1 board with DAQ PC.
- Asked before, but : when do detector groups need a system and for what? Reading out 1 DIF is different to 30!