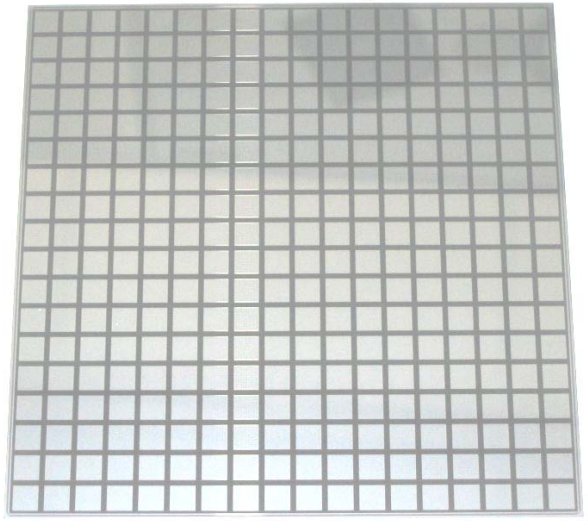
Si-W ECAL
Silicon wafers status



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Si overview

- Cz and Rus used on the prototype (low cost, standard design)
  - Ok : Depletion, current leakage, signal
  - 500 nm, 6x6 cm², 26 pads
  - Square events : understood to come from guard rings

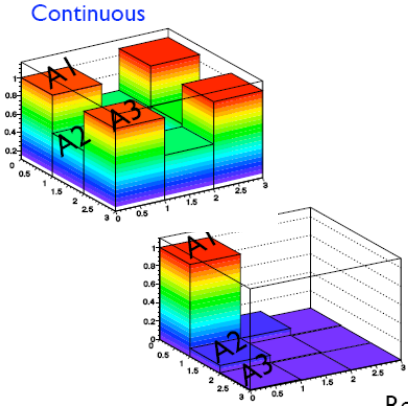
- Search for new design techniques
  - Reducing crosstalk due to the GR
    - Segmented guard rings to avoid square events
  - Lowering Dead space (at the border)

NEW : Prototypes are measured !

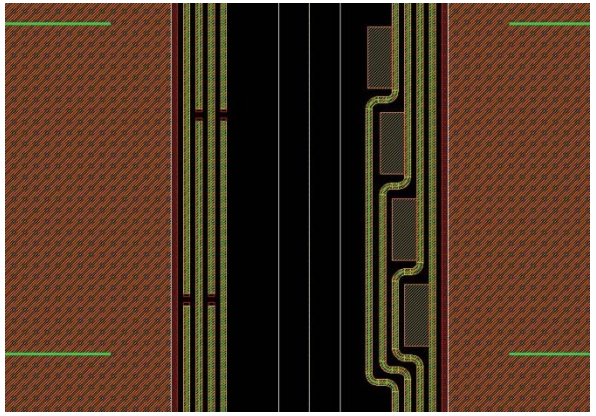
- Hamamatsu design
  - New size ordered: 300 nm, 9x9 cm², 256 pads
  - Sold as having no guard rings (thus no square events)
  - Have guard rings ! External charge injection shows square events…
  - Large dead space
  - Behavior with glue checked over 8 months : OK
  - Cost of prototypes: 70 k€ = 40 wafers, not enough for EUDET

Segmented guard rings

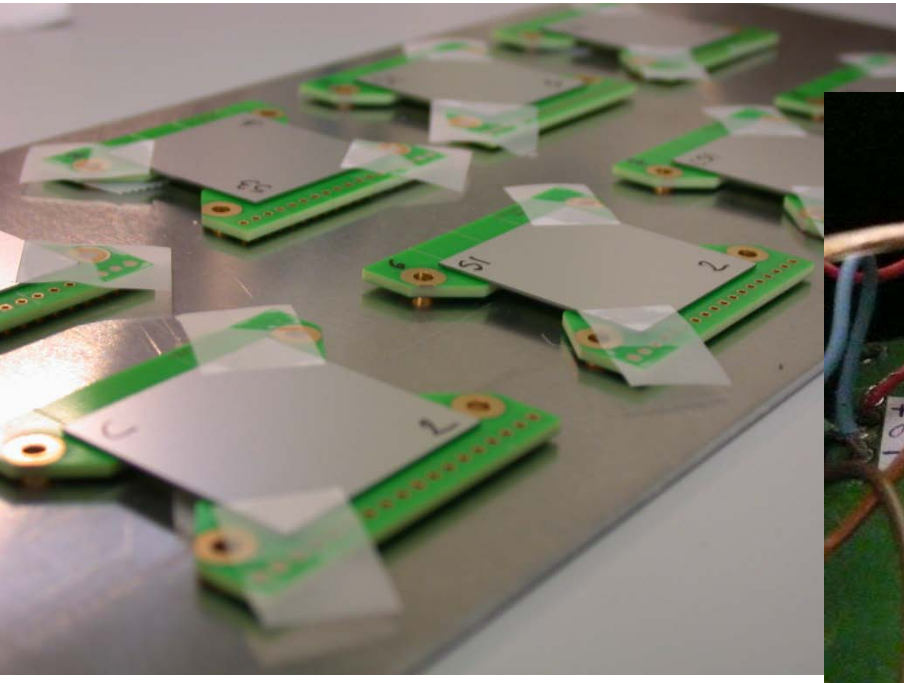
- Should avoid the signal propagation along the border of the wafer

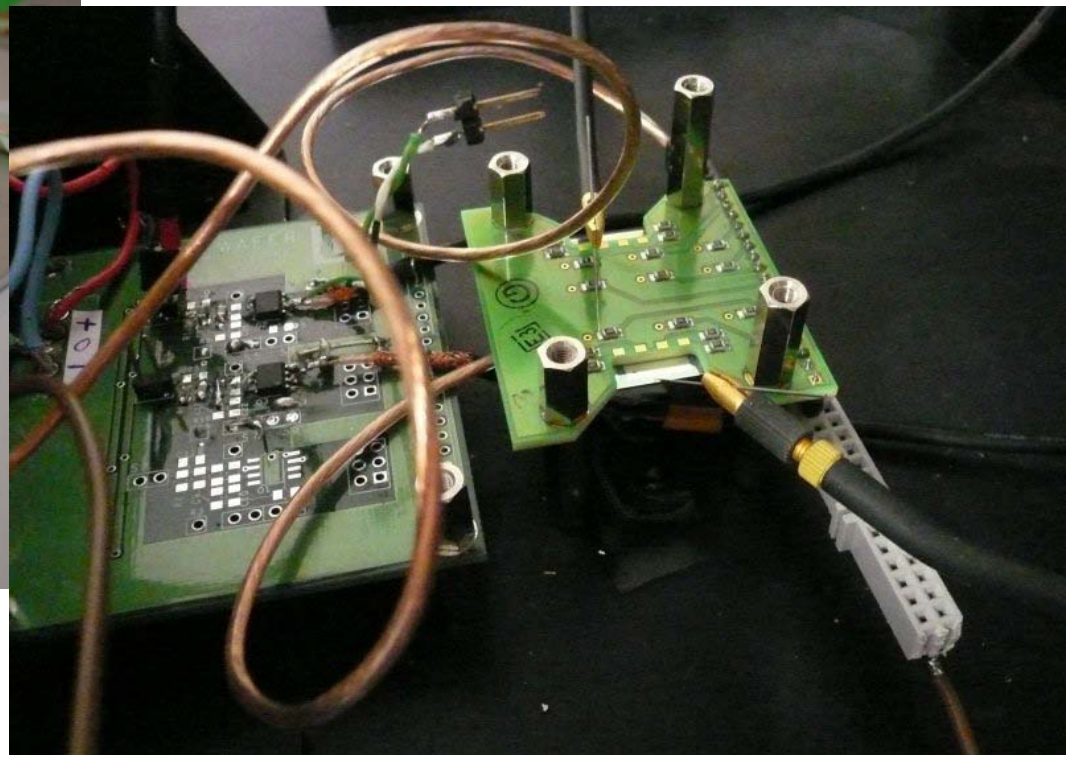


- Idea tested thanks to PCBs and test bench at LPC (CALOR'08, NSS-MIC'08 talk)
  - Segmented topology helps to prevent SqEvt
- Prototype wafers are being manufactured (LLR made layout)
  - OnSemi/Institute of Physics (Prague), Cz
  - Current leackage can now be measured
  - Together with crosstalk
- First 8 wafers were measured at LPC



Segmented guard rings prototypes





- Glued on PCB supports
- Mesured with signal injection and charge amplifiers

Segmented guard rings prototypes preliminary measurements results

- The segmentation of guard rings clearly contributes to the lowering of crosstalk along the edge of the wafers

Continuous

720		
430	220	
700	460	

1 cm segments

528	32	
50	32	31

3 mm segments

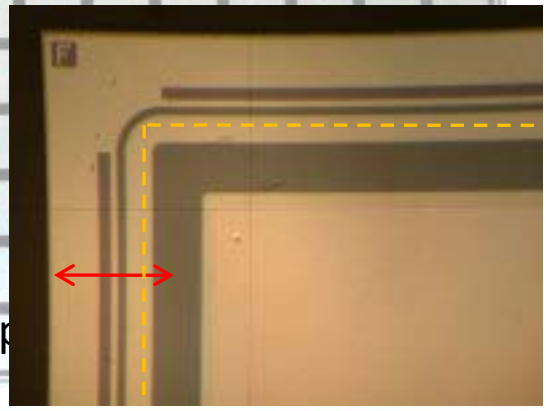
170	17	
29	14	13

- I(V) characteristics are not standard
- Breakdown occurs early, in a 100-300 V range (non segmented: >500 V)
- BUT: no optimizations were done on the layout
  - Further investigations are needed
  - Close contacts with Onsemi: agreement to share the costs

Hamamatsu wafers

- 9x9 cm2, 256 pixels ordered, 40 should be delivered on April
- Cost ! (eur/yen parity)
- 300 um (may be) gained on the edges
  - 800 um dead space (1.1 mm in previous version)

- Excellent breakdown >800 V
- Low leakage <4 nA/pixel
  - DC coupling to the chips
  - 1 nA = 1% dynamic range
- Good dC/dV at Vbias, <2pF/V (full wafer)
  - Mandatory for noise (CdV + **VdC**)
  - C= 10E-12, dV=10 mV, V=150V, dC = 20 fF => ~400 MIPs…

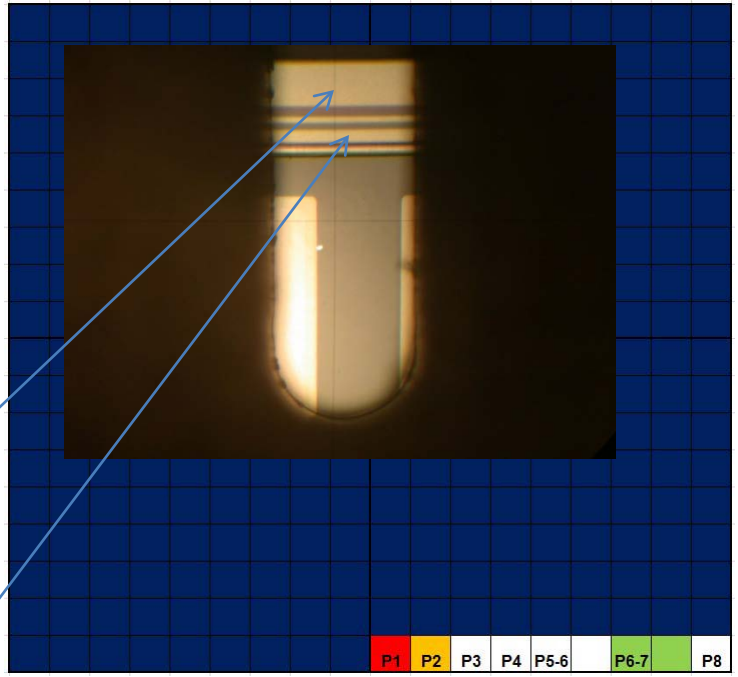


Hamamatsu wafers : crosstalk measurements

Charge is injected on the metal rings: a similar behavior as for square events is measured.
Compared to PCB models with continuous guard rings :

- Factor 4 less for the outer guard ring
- Factor 50 less for the inner guard ring

Square events are expected !



Pixel ID	Amplitude (mV)
P1	1030
P2	1060
P6-7	2080

Pixel ID	Amplitude (mV)
P1	80
P2	63
P6-7	111

But signal (charge) is injected at the surface. What if charge is generated in the volume below the rings ?

It needs further investigations with particles or laser beam

Layout: Some optimizations

In2p3

For Vertex detectors

Cost

3D sensors : lower Vbias, internal current flow, low sensibility to edge effects : can be ~edgeless (100 um)

Cut through edge

same technology as for 3D but used only at the edge
no saw cuts, 3D edges
4-side abuttable ~*no dead space,* Deep trench etch, n doped polysilicon fill provides edge doping

Integration ☹

Trenches + saw cut : cost of trenching, post processing of every sensors, bad control of current.

Dry etching cut

Current terminating ring

two rings but biased : thin contact needed, gluing not applicable
edge width less than ½ wafer thickness

Integration ☹

Double sided GR

Doped edges

Punch-through biasing

Biased GR

Integration ☹

Crosstalk + ~edgeless ☺ (300 um)

Segmented GR : need further tests

edge ☹ (800 um)

Front end board

- Hamamatsu wafer will have pads to bias the GR in order to avoid crosstalk (if necessary)
  - FEV7 to be adapted for bounding (holes)

  - Prototype for a definitive solution (additional cost) if segmented/other do not work
- FLCPHY3 should be used for crosstalk measurements
  - Instead of Op. Amp.
  - Upgrade of test bench at LPC
  - measurements with laser or beam

ECAL Silicon wafers : Conclusion

40 Hamamatsu wafers expected on Q2'09 (NRE 31k€ + 1k€/sensor)
despite some uncertainties on crosstalk (~OK)
In touch (or at least try) with other manufacturers (ONsemi, Russia, Korea,…)

Segmented guard ring to be tested on full size wafers + with beam

Funding will be an issue for 2009
120 additional sensors needed to complete EUDET : >100 k€
prototypes with segmented / other GR

Collaboration with
FZU, Prague
OnSemi (Cz)
MSU, Moscow
Korea

How to use the available sensors among the slabs ?
1 long SLAB = 14 * 4 = 56 wafers, not all usefull for the tests: ½ could be equipped
at least: capability to read-out the far-end
1 short SLAB = 8 wafers