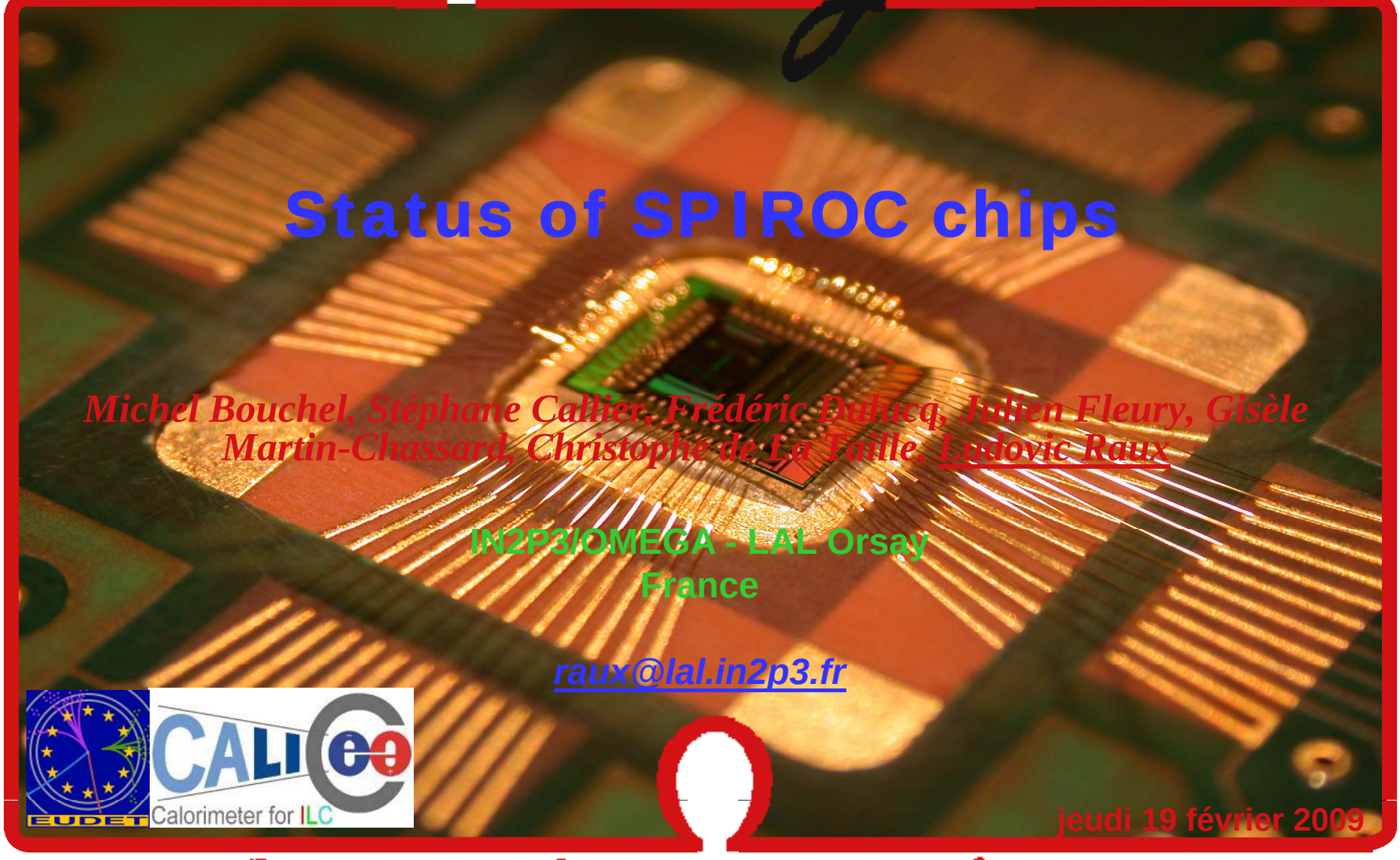

Status of SPIROC chips

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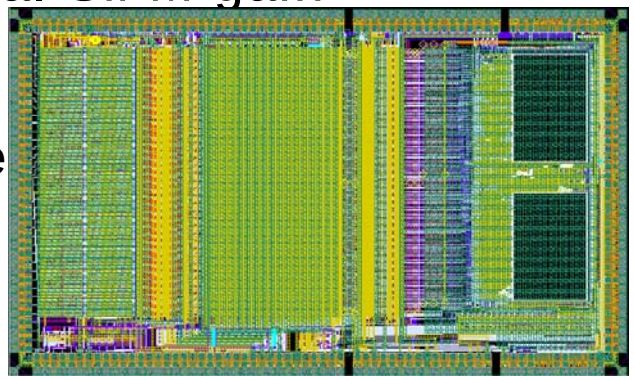
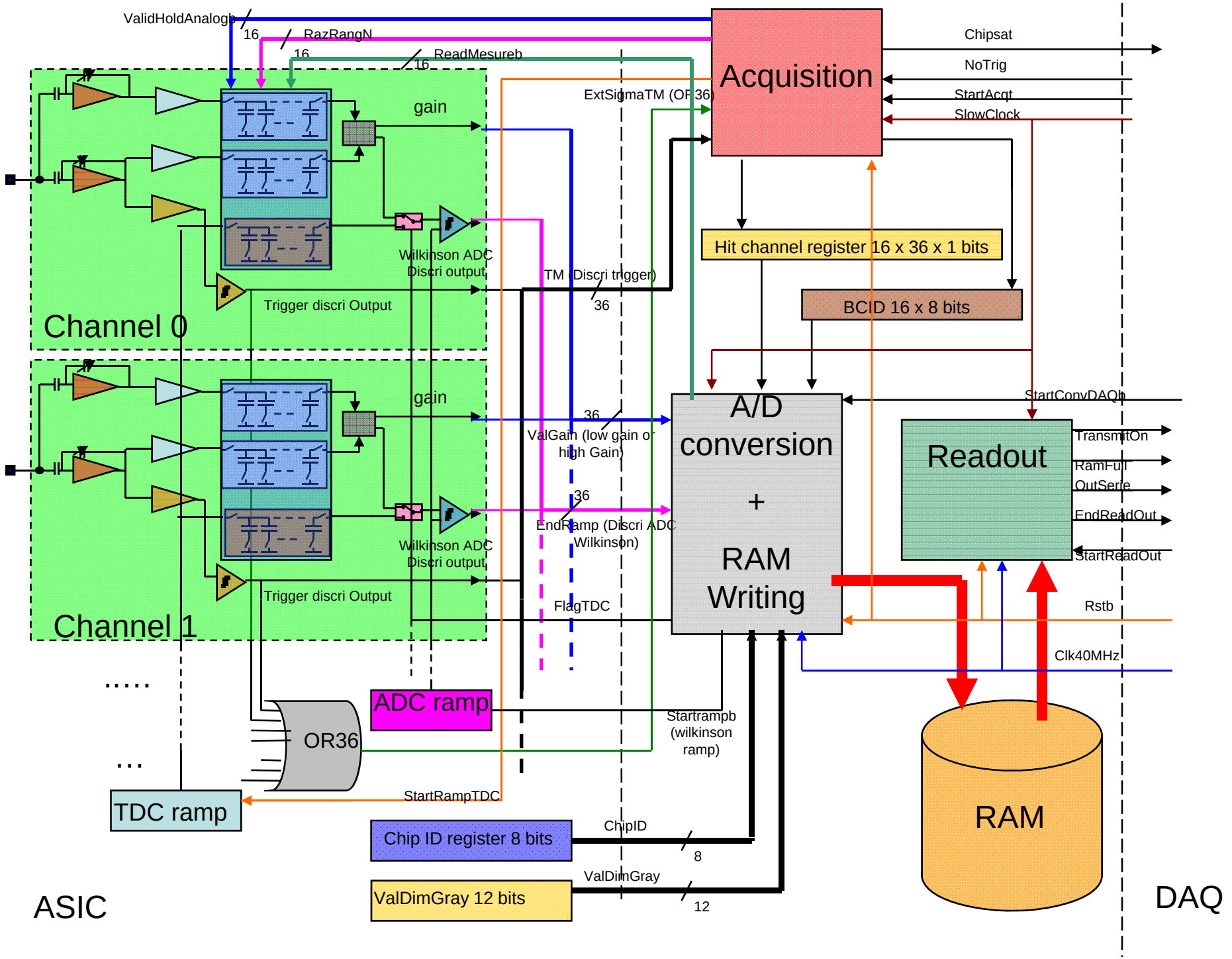
jeudi 19 février 2009

Reminder : SPIROC main features

- 36-Channel ASIC
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 25ns to 175ns
  - pe/noise ratio : 11
- Auto-trigger on MIP or spe
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on 1/3 pe (50fC)
- Time measurement :
  - 12-bit Bunch Crossing ID (coarse time measurement)
  - 12-bit TDC step~100 ps (fine time measurement)
- Analog memory for time and charge measurement: depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded features (bandgap, 10-bit DAC, etc.)
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and daisy chain readout

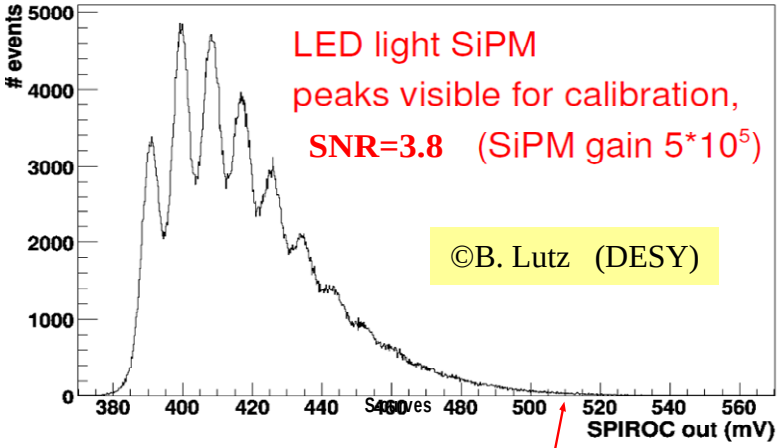


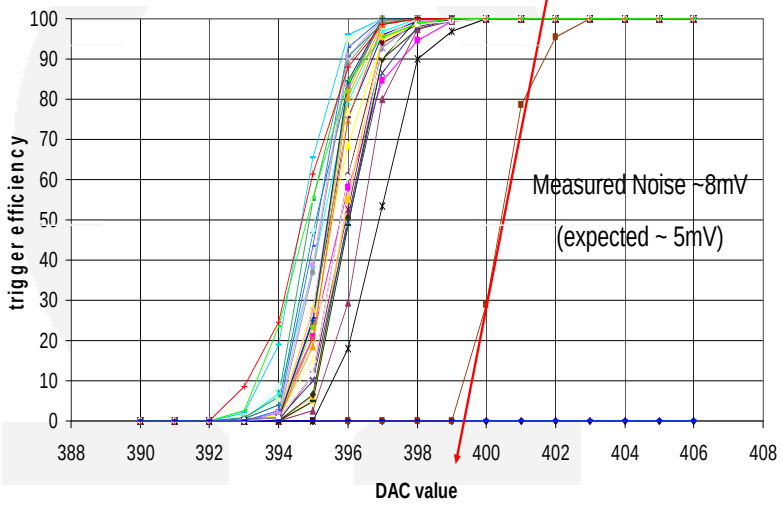
Fabricated in SiGe AMS 0.35 µm
Submitted in June 2007
Delivered in October 2007
Chip area: 30 mm² (4.2mm × 7.2mm)

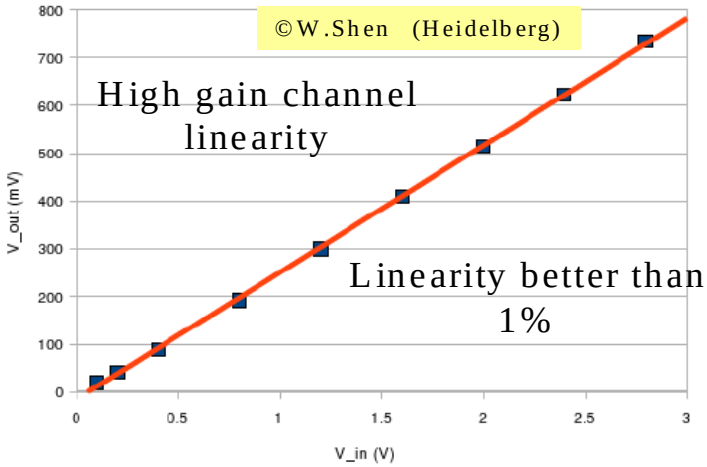

ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Channel 1
36
ValGain (low gain or
high Gain)
A/D
conversion
+
RAM
Writing
StartConvDAQb
Readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
36
EndRamp (Discri ADC
Wilkinson)
Wilkinson ADC
Discri output
Trigger discri Output
FlagTDC
Rstb
Clk40MHz
.....
...
ADC ramp
OR36
Startrampb
(wilkinson
ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

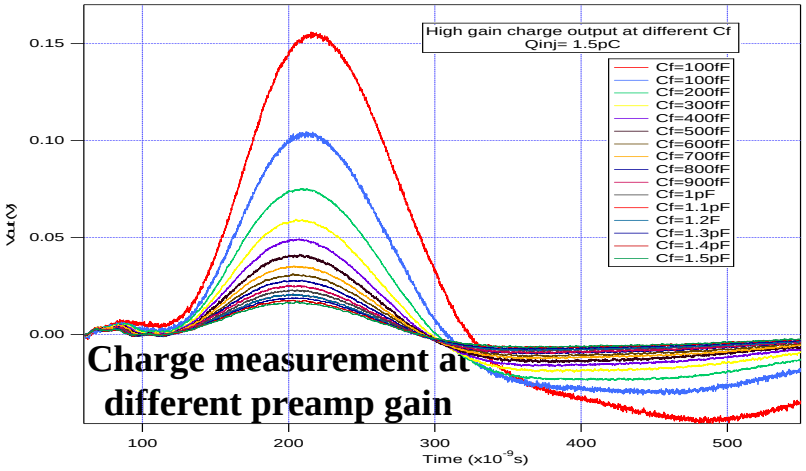
SPIROC 1 Status

- **Analog part OK, can be used to replace FLC_SiPM**
- **Autotrigger at ~50fC**
- **Could be tested with existing detector and DAQ**
- **Can be used to emulate SKIROC**
- **2 major bugs which need to be corrected : probe register to see intermediate signals and inverted ADC discriminator**
- **Probe register can be used now with a fix**



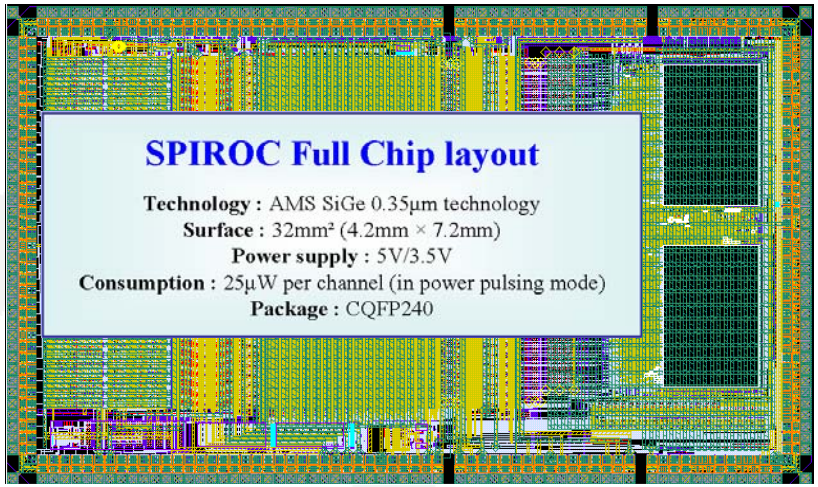






SPIROC 2 Status

- A second iteration was necessary
- SPIROC 2 prototyped in june 2008



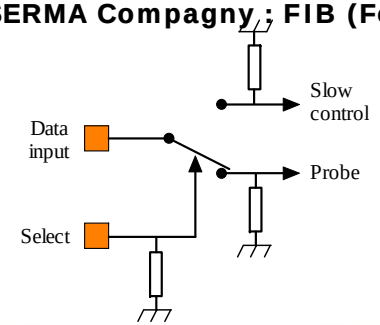
Submitted on 9th june 2008

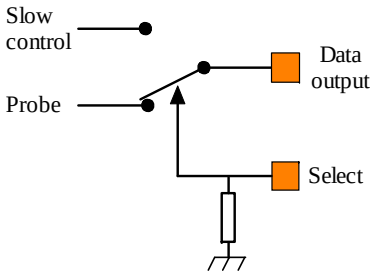
Delivery in October 2008

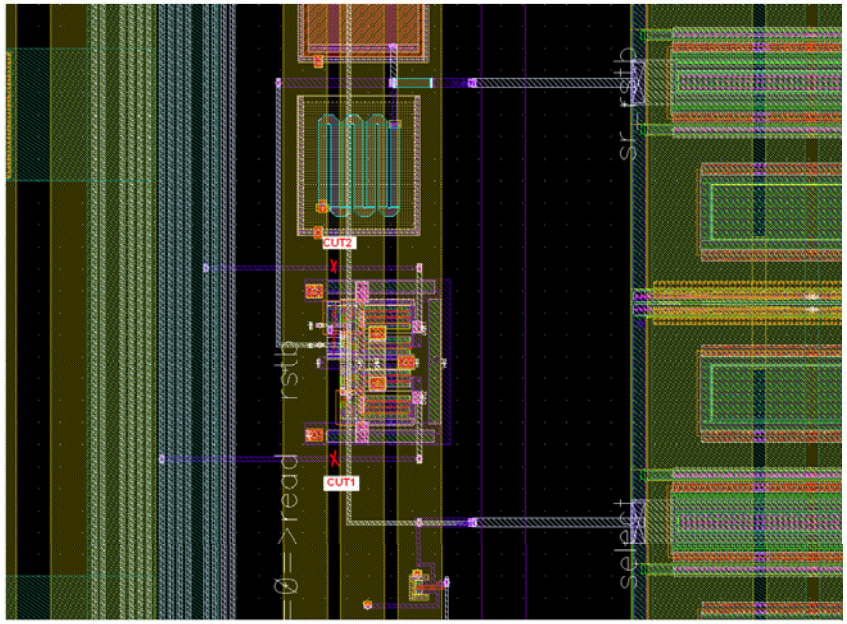
- Correction of the first version bugs (ADC discri, probe and slow control register)
- Add some light improvements (in digital part)

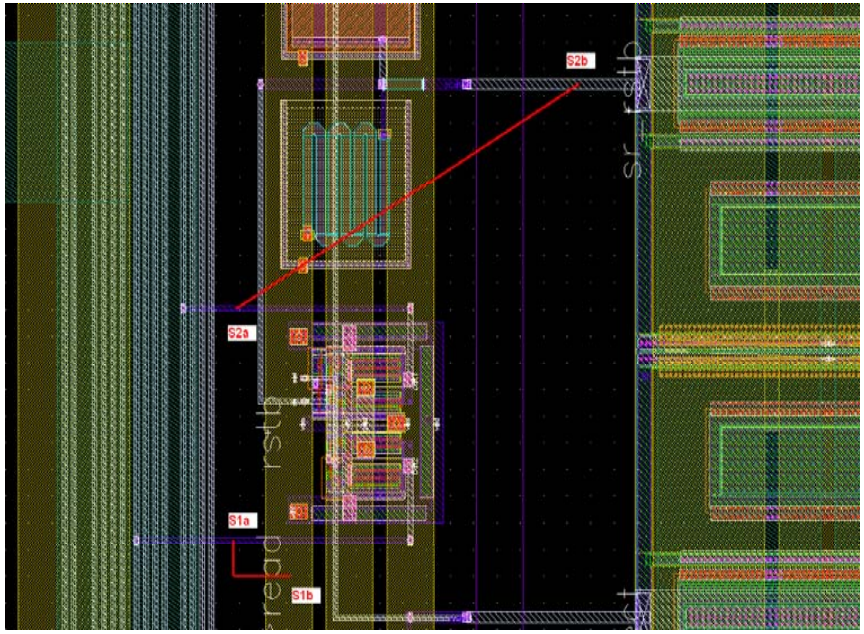
SPIROC 2 : slow control register

- **Bug on the reset signal of the new multiplexed probe and slow control register**
  - **Active low reset forced to 0 when not selected**
  - **Intempestive reset when register is unselected**
  - **Same problem on Hardroc 2**
- **Correction by SERMA Compagny : FIB (Focused Ion Beam)**







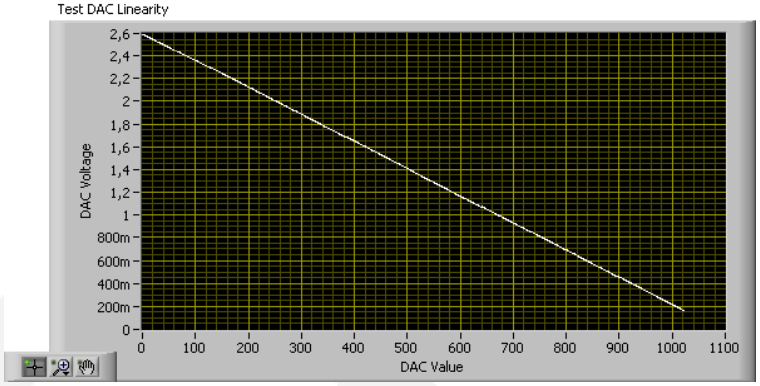


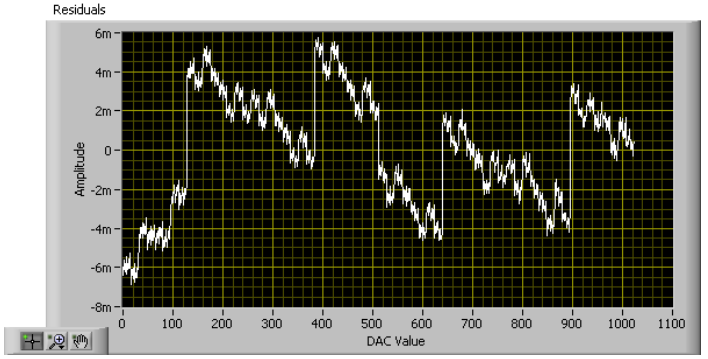
Spiroc 2: slow control and probe register problem

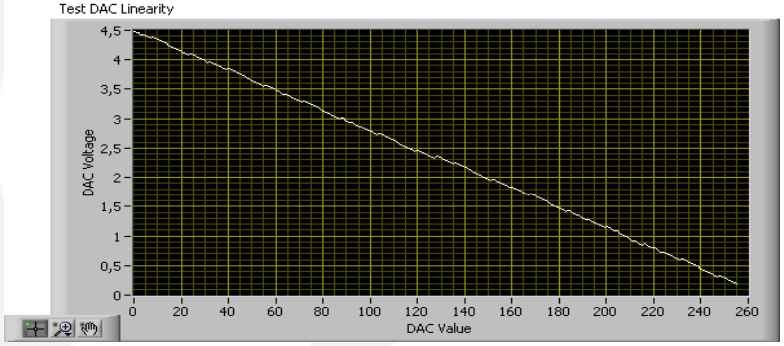
- Problem of synchronisation between DATA and Clock during the propagation in the register
- This problem already seen on SPIROC 1 probe register was supposed to be resolved in this second prototype with a new « backward » clock distribution in the ASIC layout
- Possibly due to parasitic resistance and capacitance on the clock, but still not really understood
- Problem partially resolved with an ad hoc fix for the slow control but not for the probe register by decreasing power supply to 1,5V during the loading phase

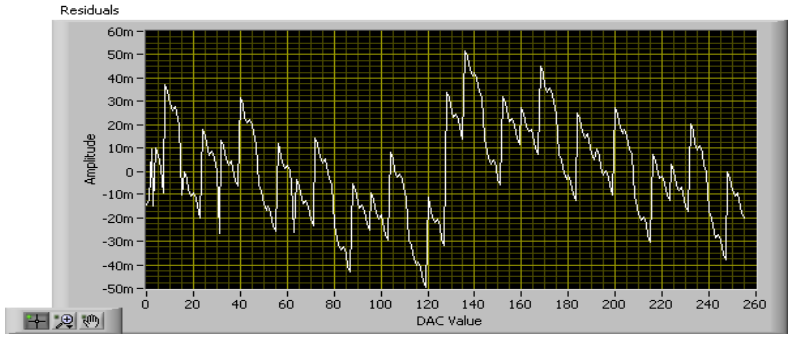
SPIROC 2: measurements

- As expected, similar analog performance as the first prototype :
  - Gain
  - noise
  - Ultra-low power input 8-bit DAC
  - Threshold 10-bit DAC









Extended measurements to be performed to validate features like ADC, autotrigger, TDC, power pulsing, etc.

SPIROC packaging

Production packaging:

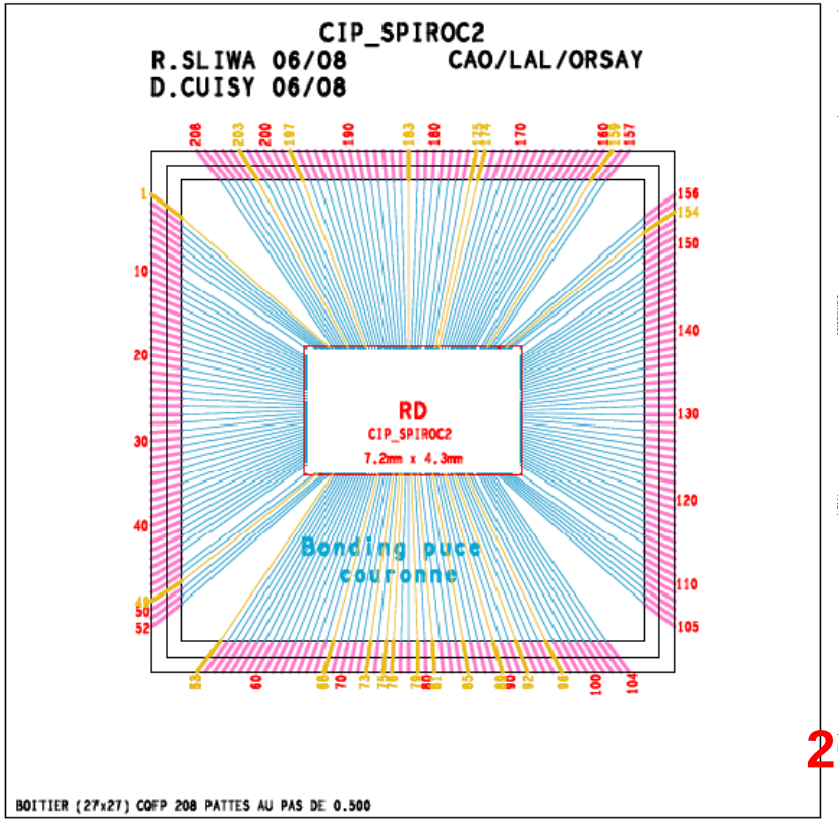
US compagny : I2A

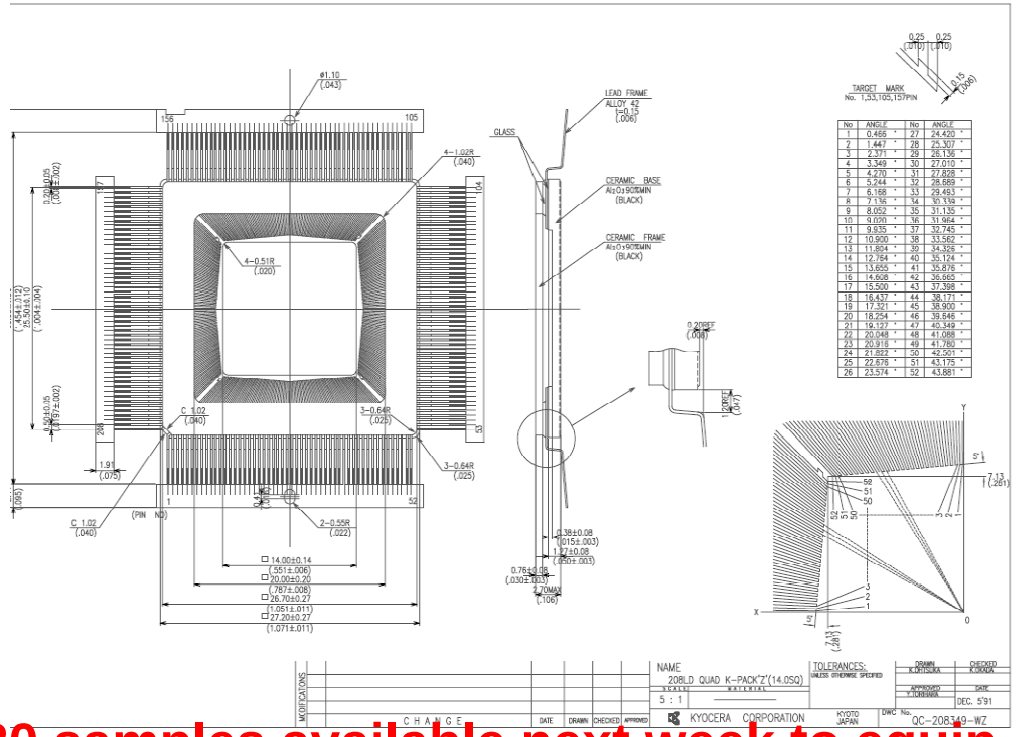
Cost : 3k euros

206 pads to connect

Best candidate for the production : TQFP208 (plastic packaging)

Dimensions:
27 x 27 x 1.4 mm



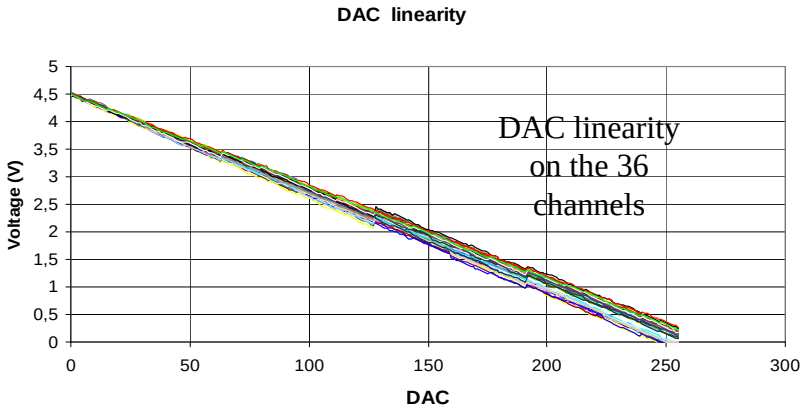


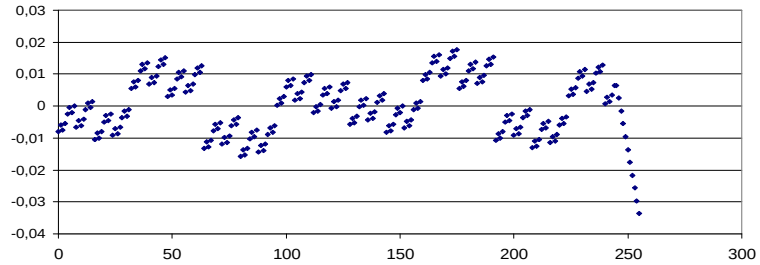
20 samples available next week to equip the first PCB prototype

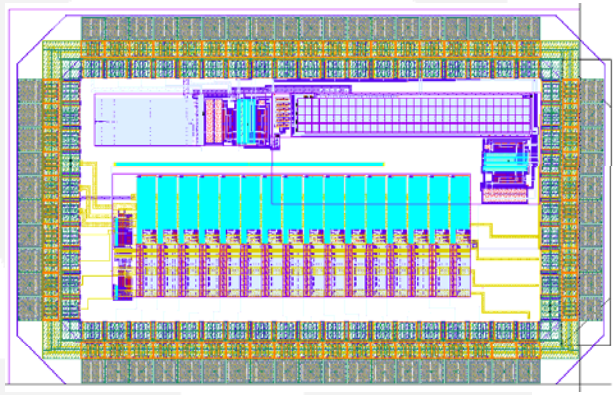
Future improvement on the SPIROC DACs

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range
- LSB=20mV
- 36 DAC : one per channel
- Ultra low power (1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 2%
- DAC uniformity between the 36 channels : ~3%

- « Building block » funded by IN2P3 submitted last month
  - Improved 12-bit DAC for the threshold trigger
  - 16 8-bit low power input DAC
- Improved performance (linearity, uniformity channel by channel) expected with a new layout rearrangment for a better matching
- Will be easily implemented in the next iteration if OK







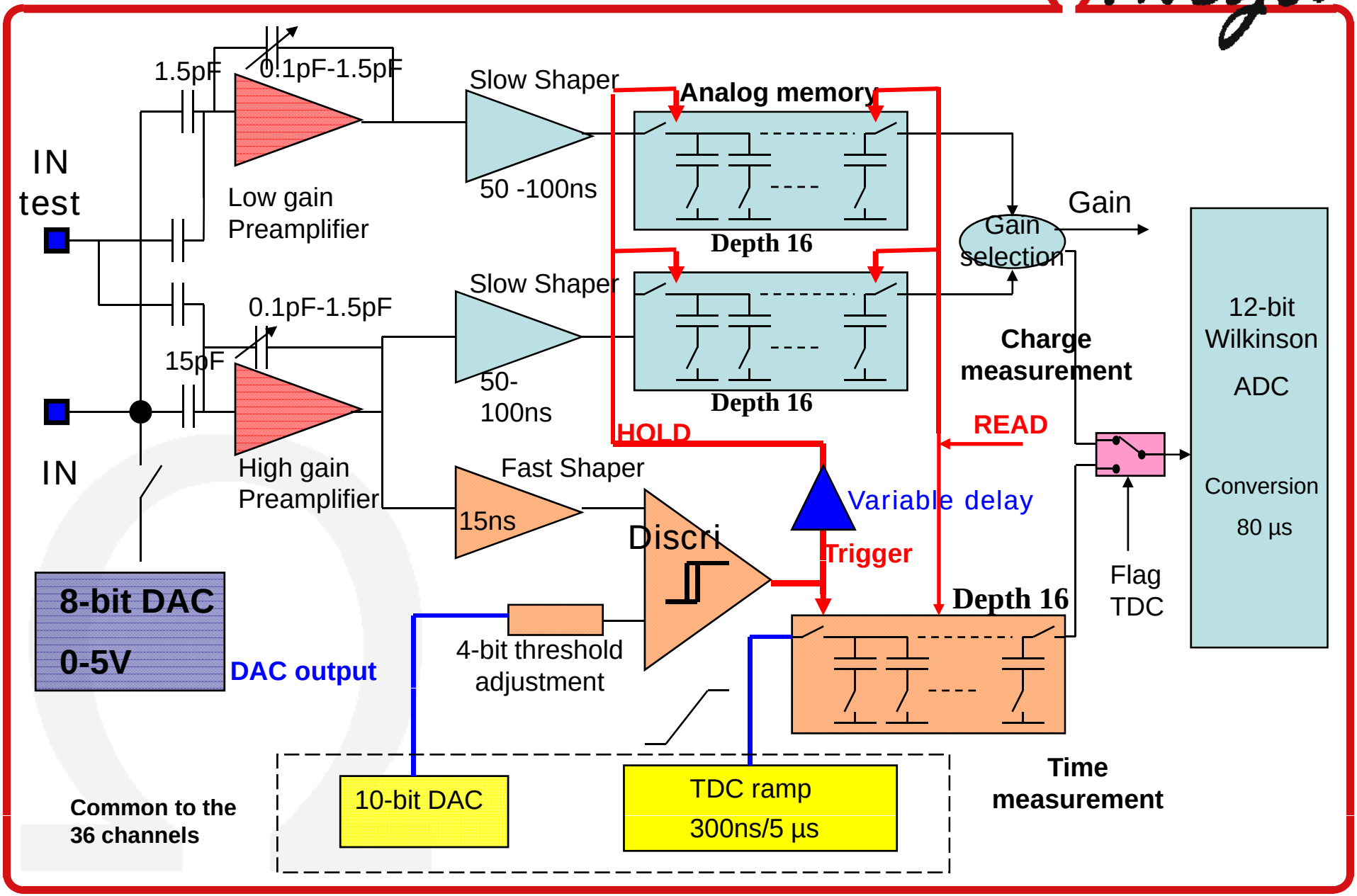
Submitted in November 2008

Delivery expected in February 2009

Conclusion

- SPIROC 2 chip
  - Very conservative prototype compared to the first one with corrections of the first version bugs (ADC discri, probe and slow control register) and adding some light improvements (in digital part)
  - New bug on the slow control and probe register has appeared. The bug on the slow control can be circumvented to operate the chip but not on the probe register
  - The first measurement results give similar results as the first prototype, but it is now essential to perform extended measurements to see if the chip can be used for the EUDET prototype (ADC performance, auto-trigger, power pulsing,etc.)
  - Chip in final package: TQFP 208 : 20 Samples available next week for the first PCB prototype
  - Next chip will go with the hardroc engineering run (Summer 2009?)

Reminder: SPIROC channel schematic



SPIROC 1 status : other measurement on Time

- Time walk: ~10ns (can be corrected off line)
- Jitter at 50ns delay ~ 45 ps
- Delay box to set Hold signal to peak : OK