Progress report on the LPSC-Grenoble contribution in micro-electronics (ADC + DAC)

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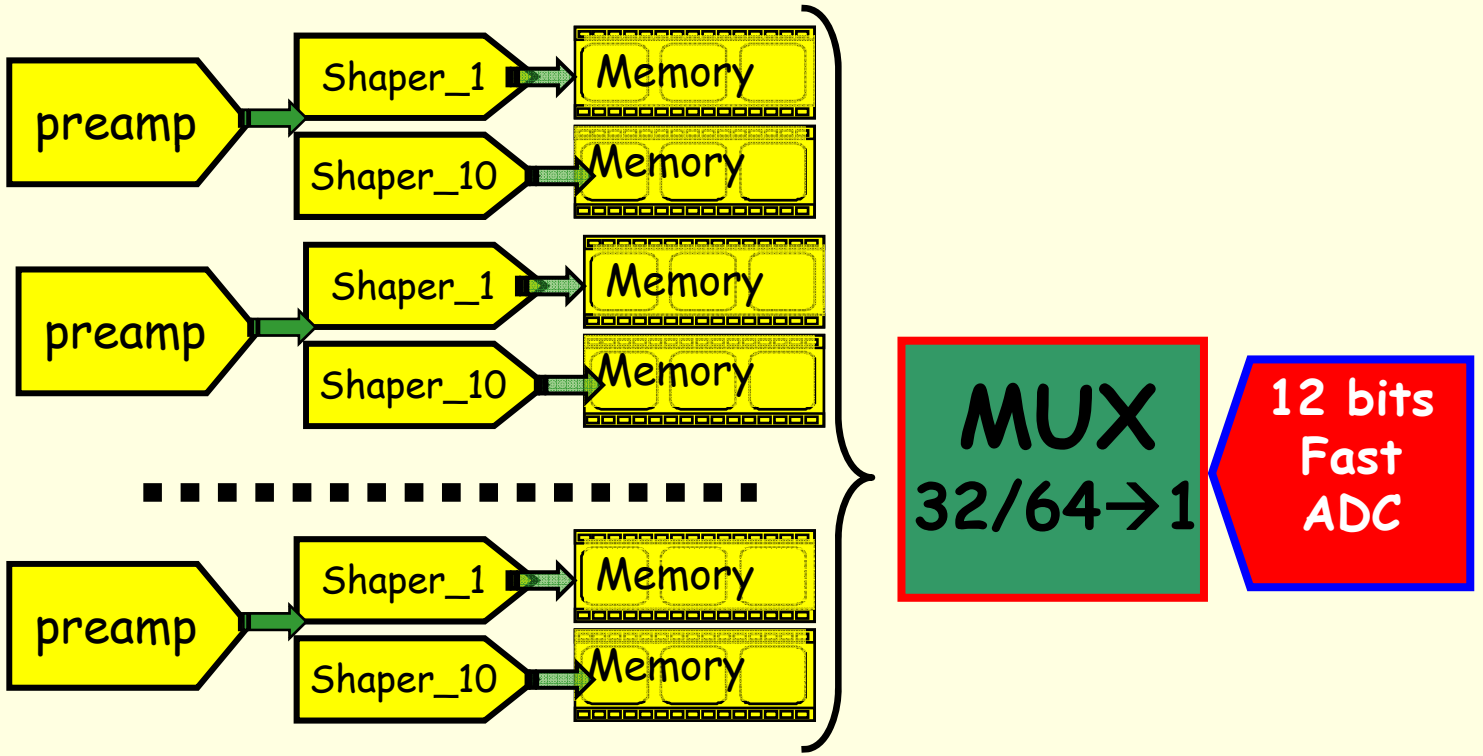
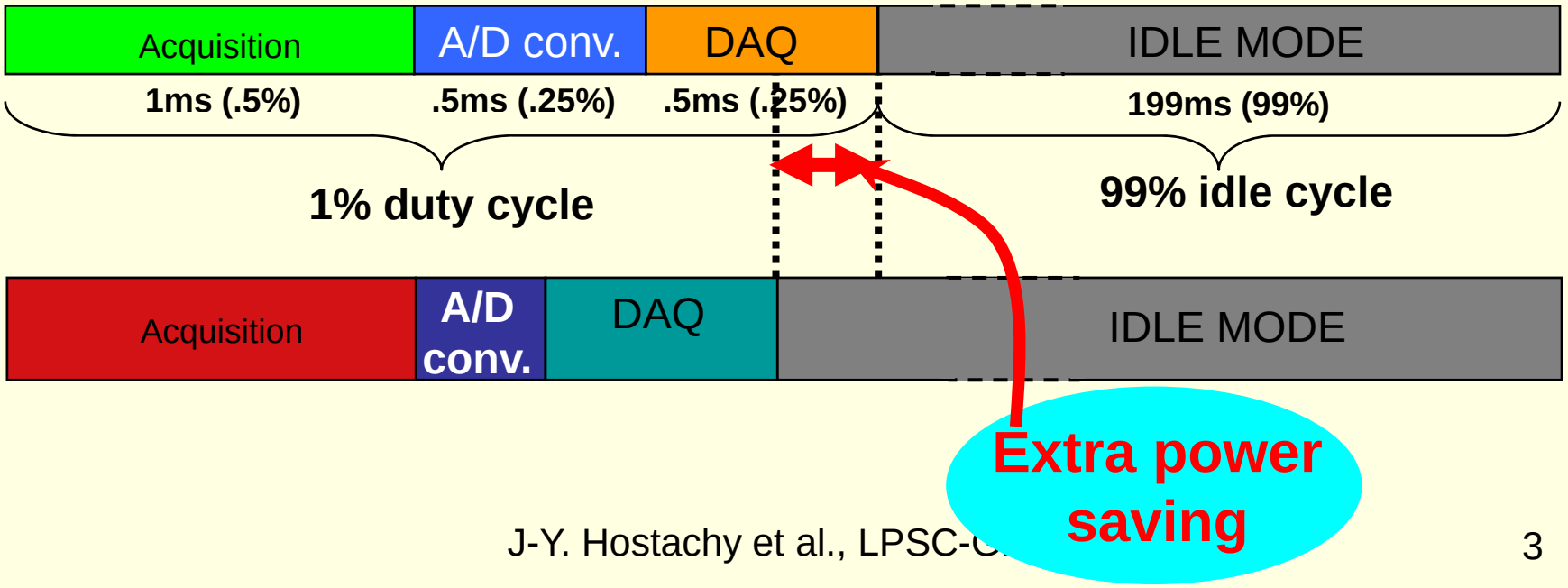
Fast Digitizer for CALICE

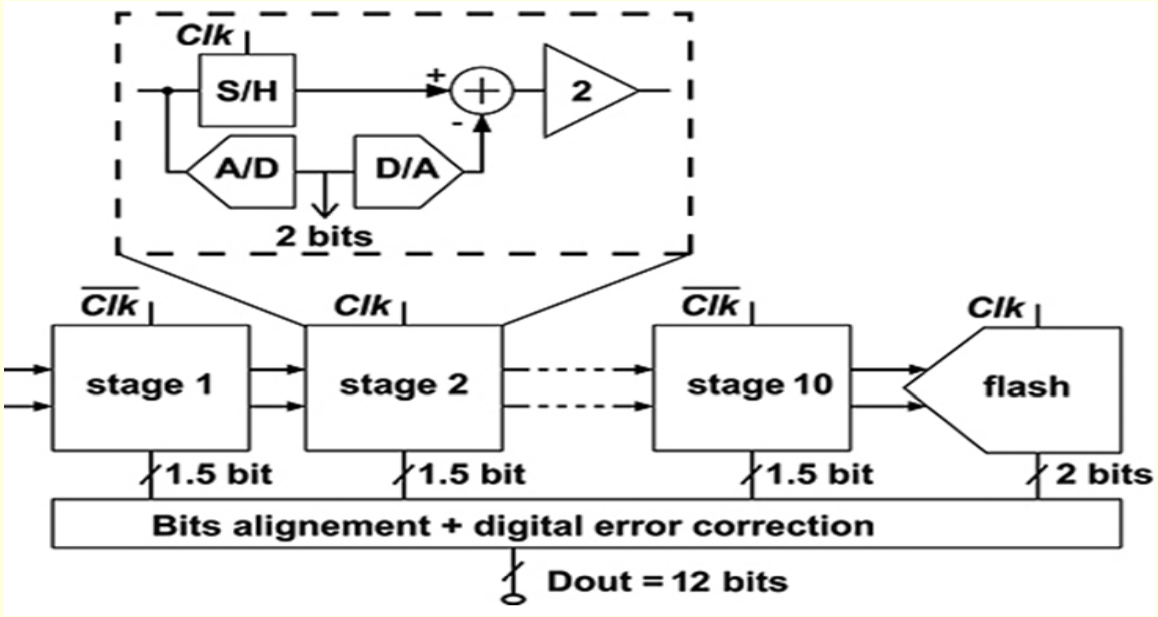


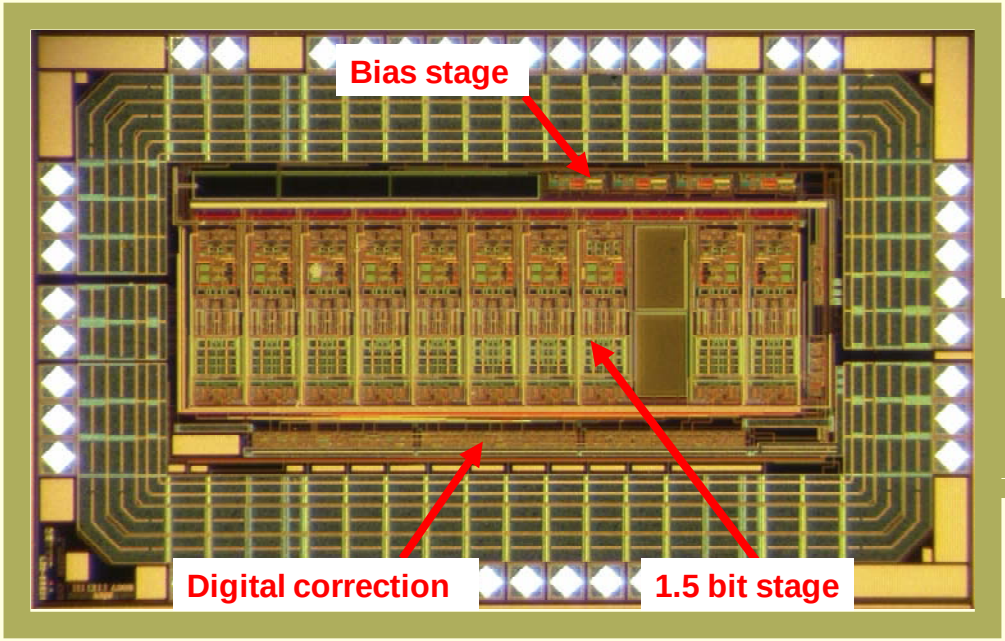
Why a high speed ADC ?

- Multiplex 32/64 to 1 ADC
- High speed converter:
  - Read all channels faster
  - More “IDLE mode” time => **Saving power**
  - digital noise source from one ADC



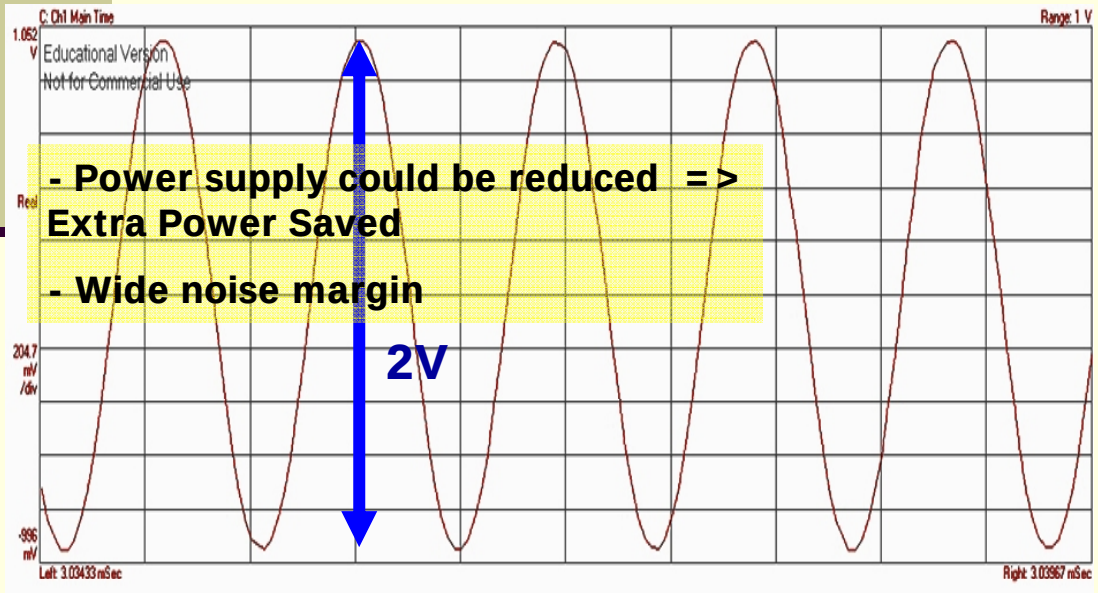
25 MHz, 12 bits, $2V_{pp}$ Pipeline ADC

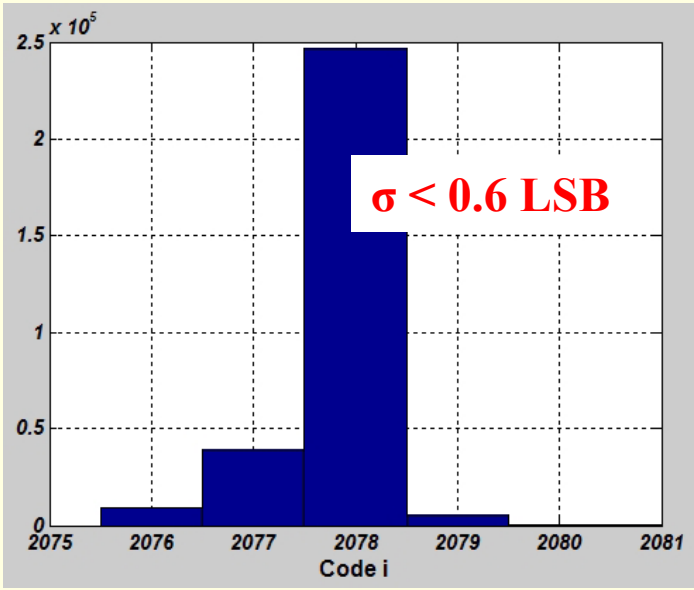


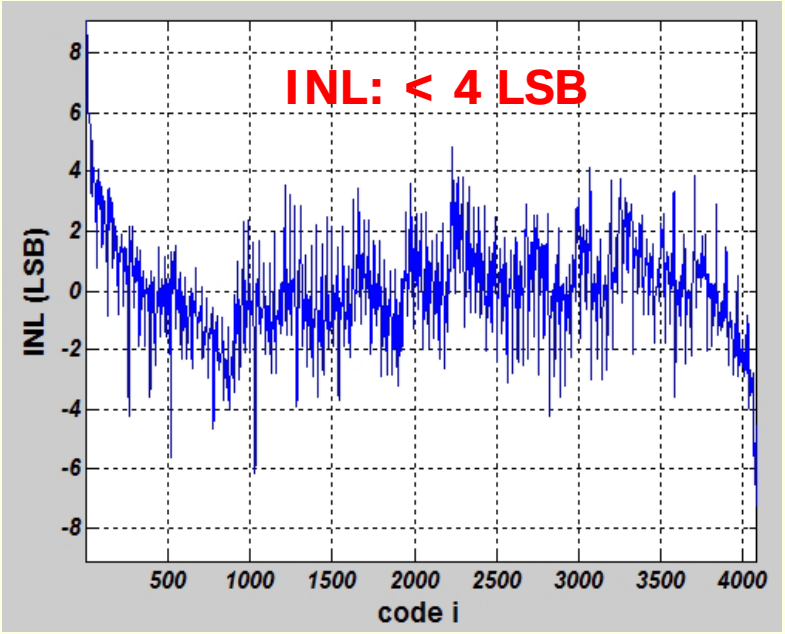


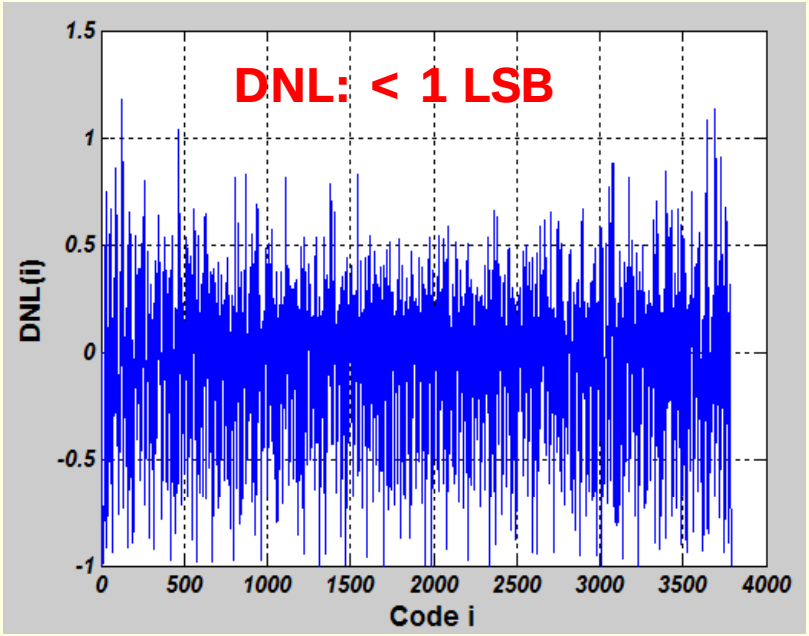
Full 1.5 bit per stage

Tests of the pipeline ADC

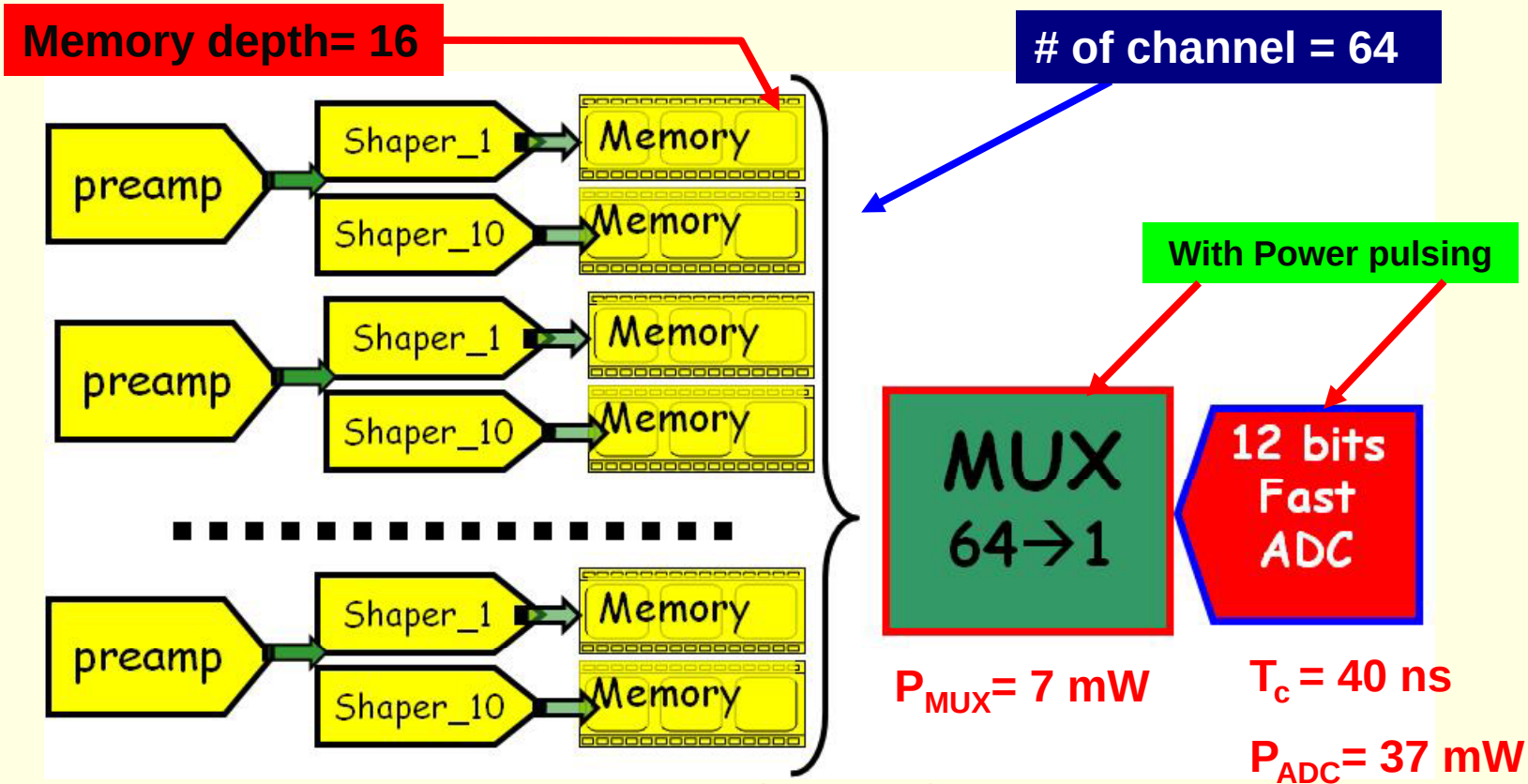








Average Power Pulsing Budget



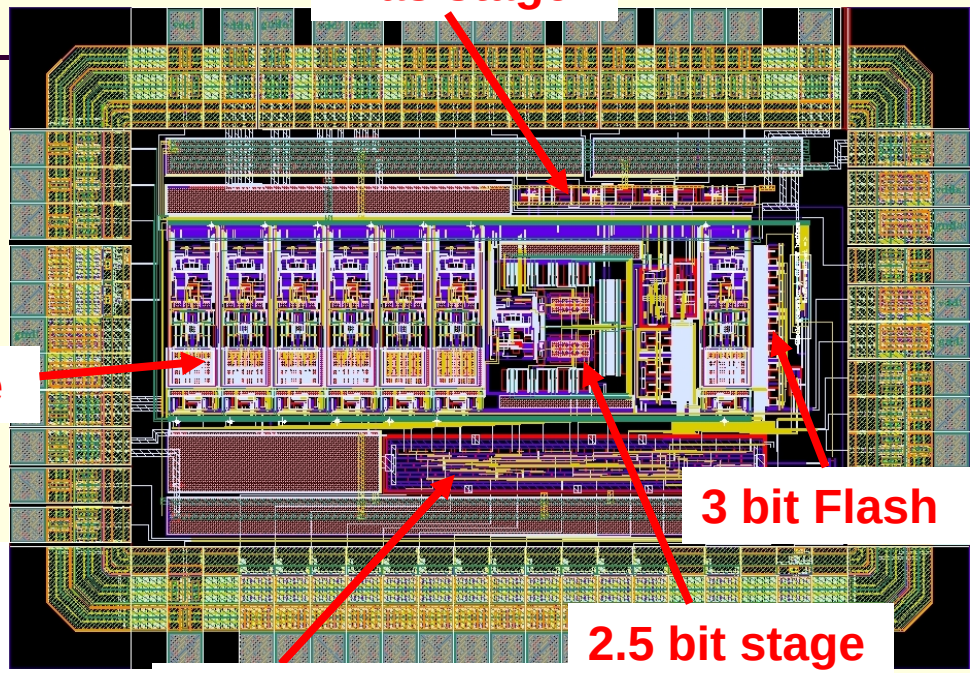
T_{TC} (Total Time conversion) = 40ns x **64 x 16**

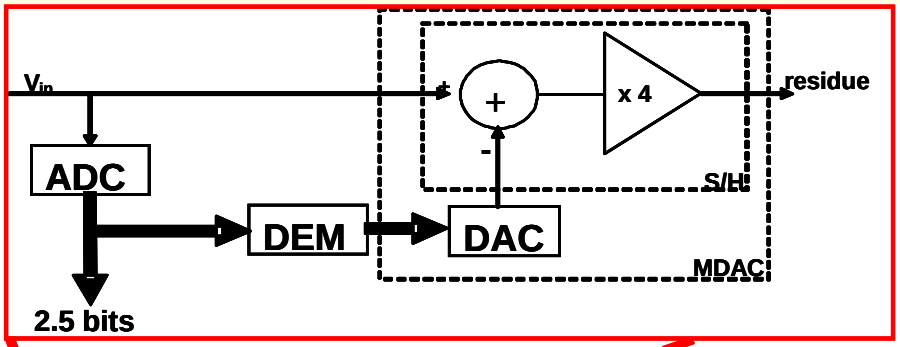
= 41µs

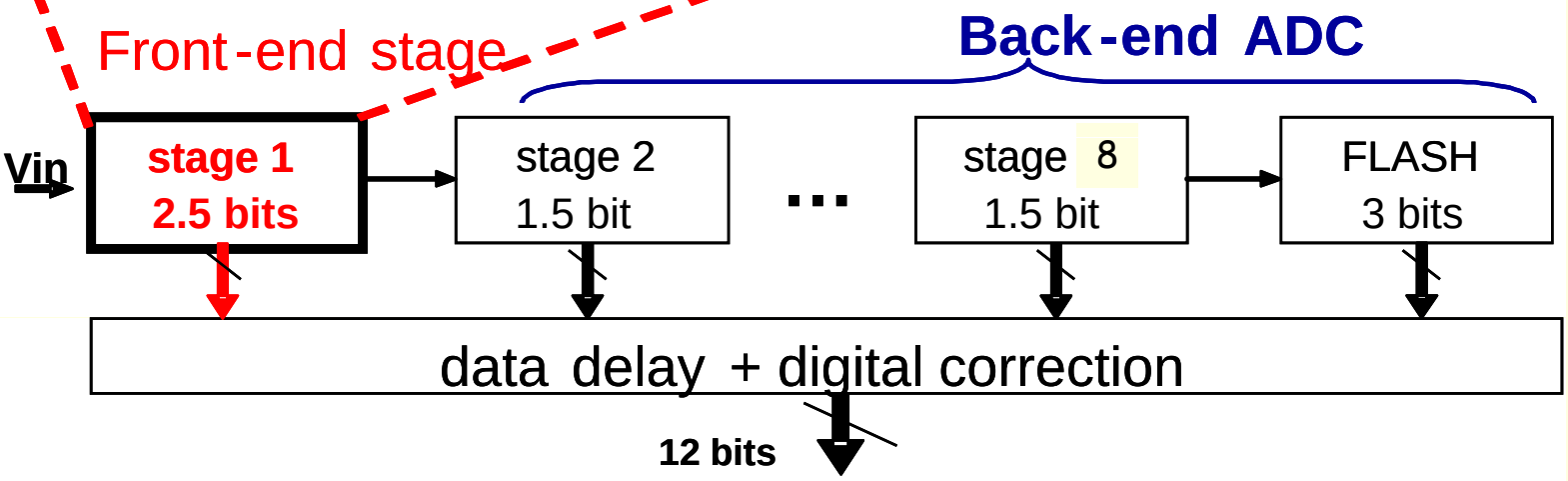
MUX + ADC Power Consumption per channel = ((P_{ADC}+P_{MUX}) x T_{TC})/200ms/64ch

→ **141nW/channel**

A multi bit 2.5 bits 1st stage ADC



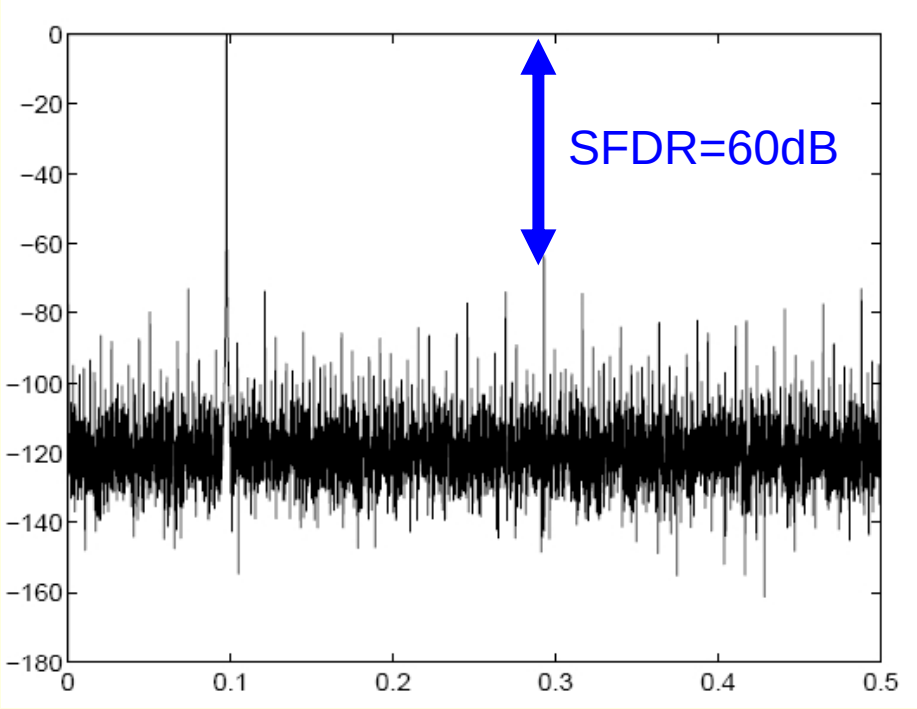




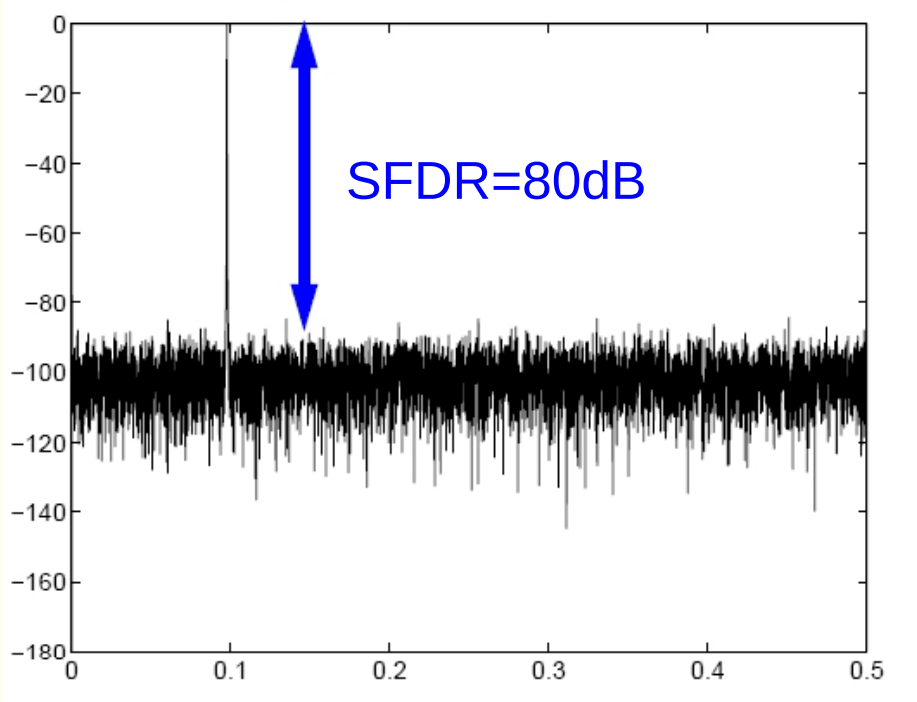
Dynamic Element Matching (DEM)

Dynamic Element Matching effect (simulation estimate)
Distortion reduced => Improvement of INL

Without DEM => INL = 4 LSB



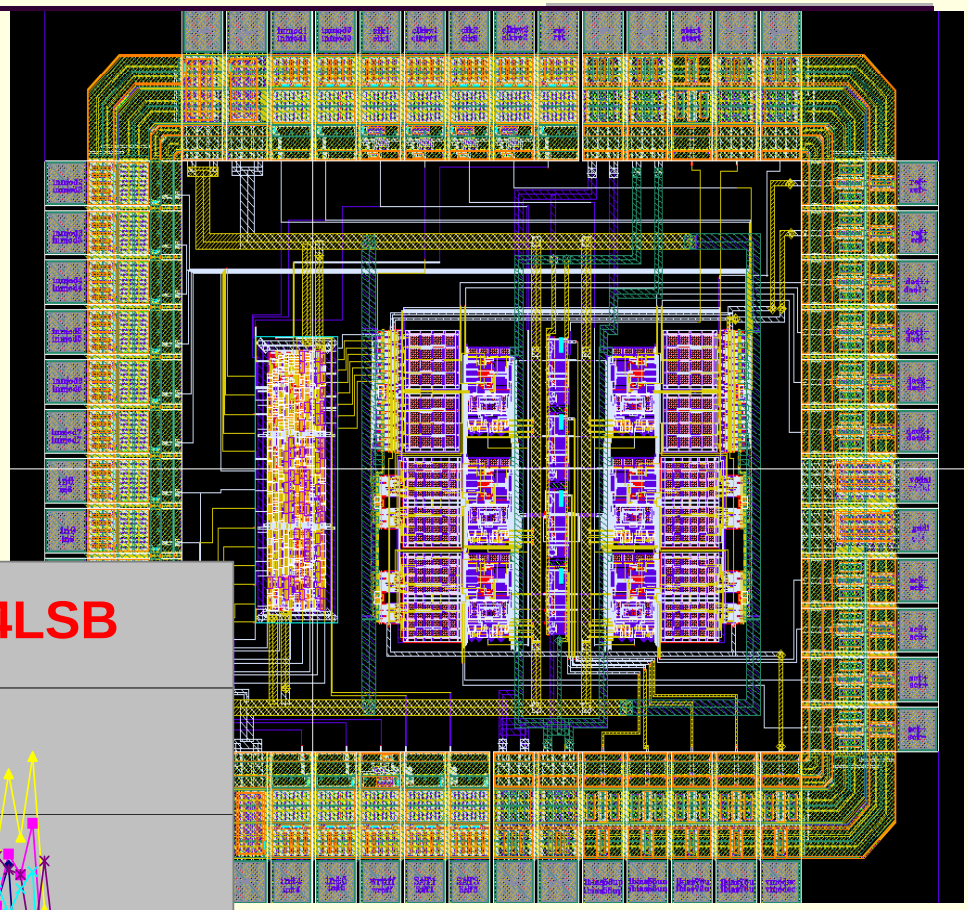
With DEM => INL = 0.4 LSB

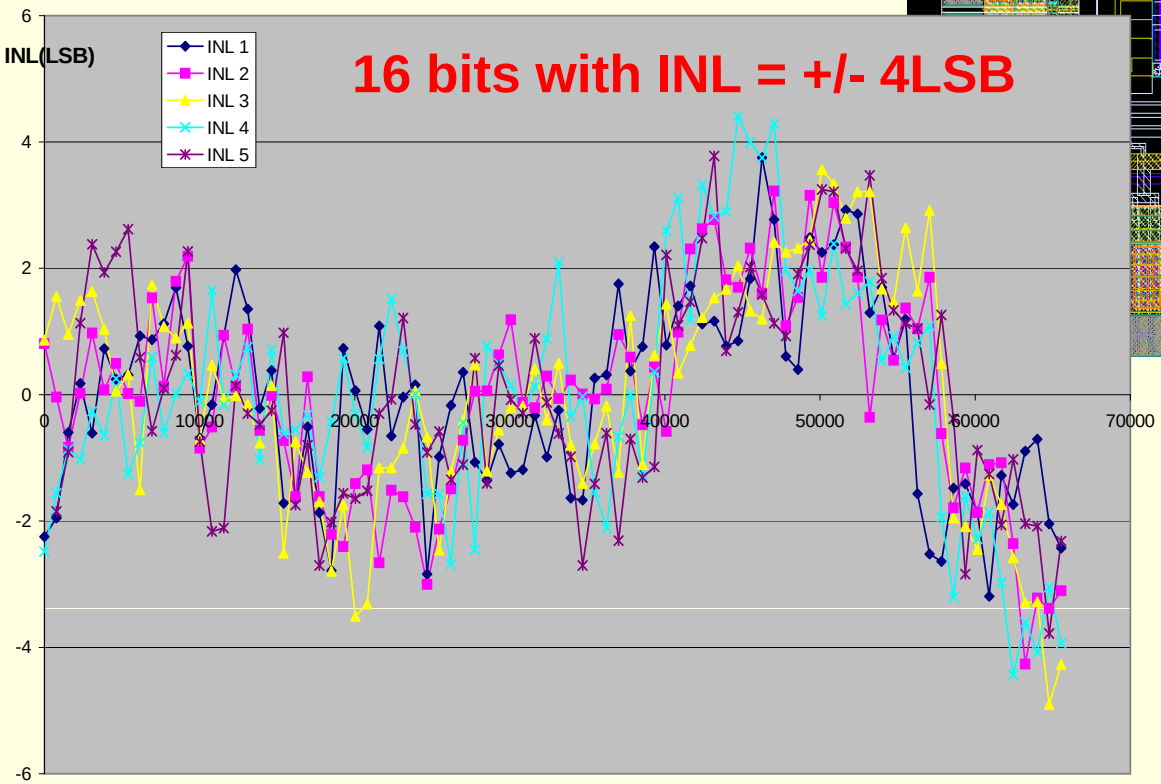


16 bit Sigma Delta DAC

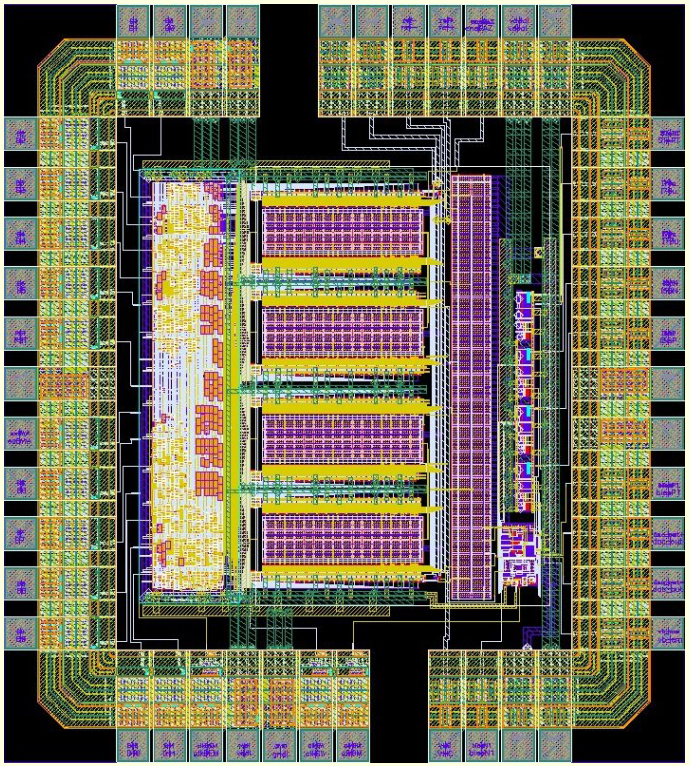
Fine results **but an integrated filter is needed** to generate a DC signal

This is not trivial, this is why we consider another architecture "C_2C"

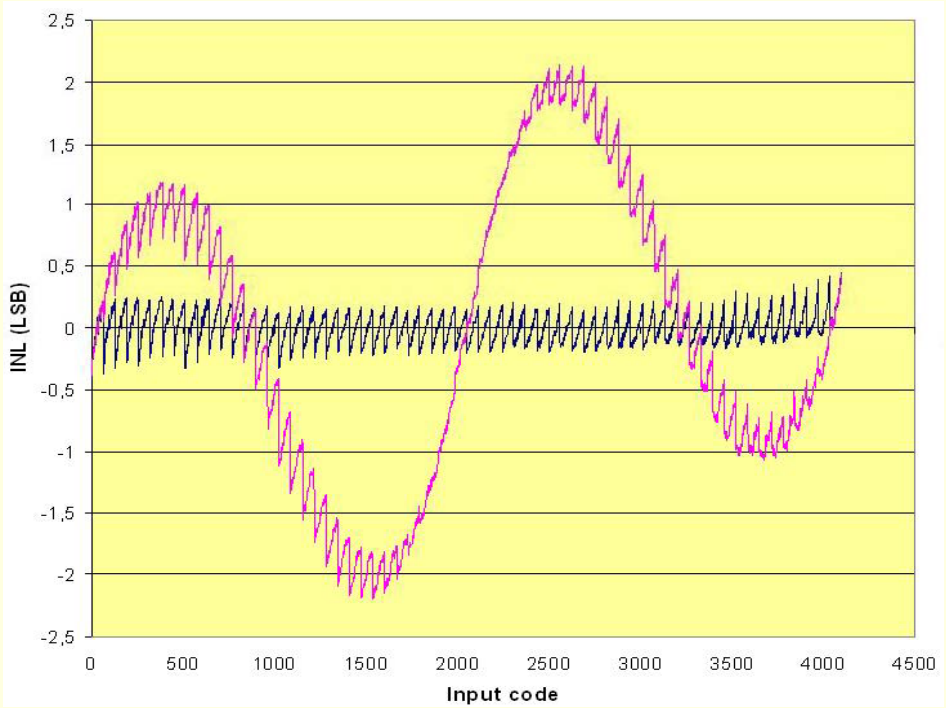




12 bit 4 MHz DAC for calibration (Segmented arrays of switched capacitors)



12 bits with INL = +/- 0.4 LSB



This 12 bits is the basis to go forward to a 14 and 16 bit version.