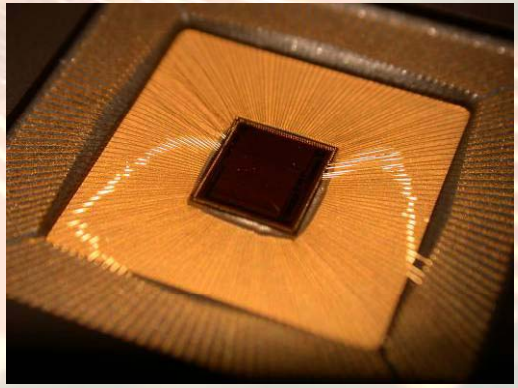
IN2P3

Omega

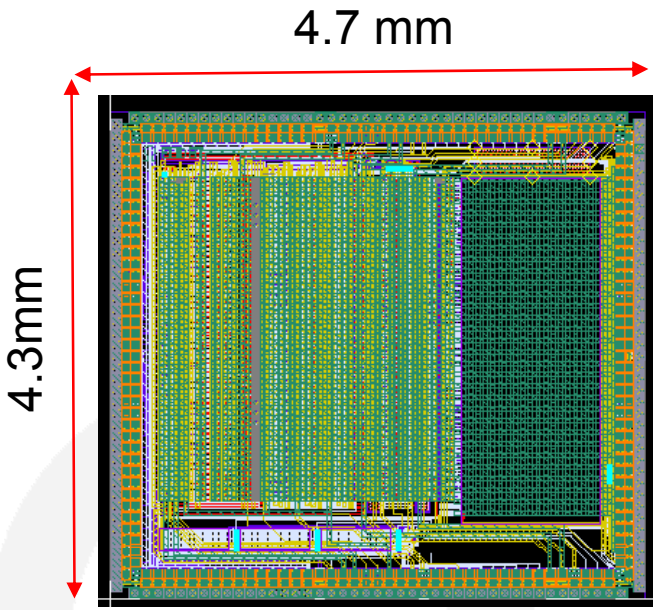
HARDROC2



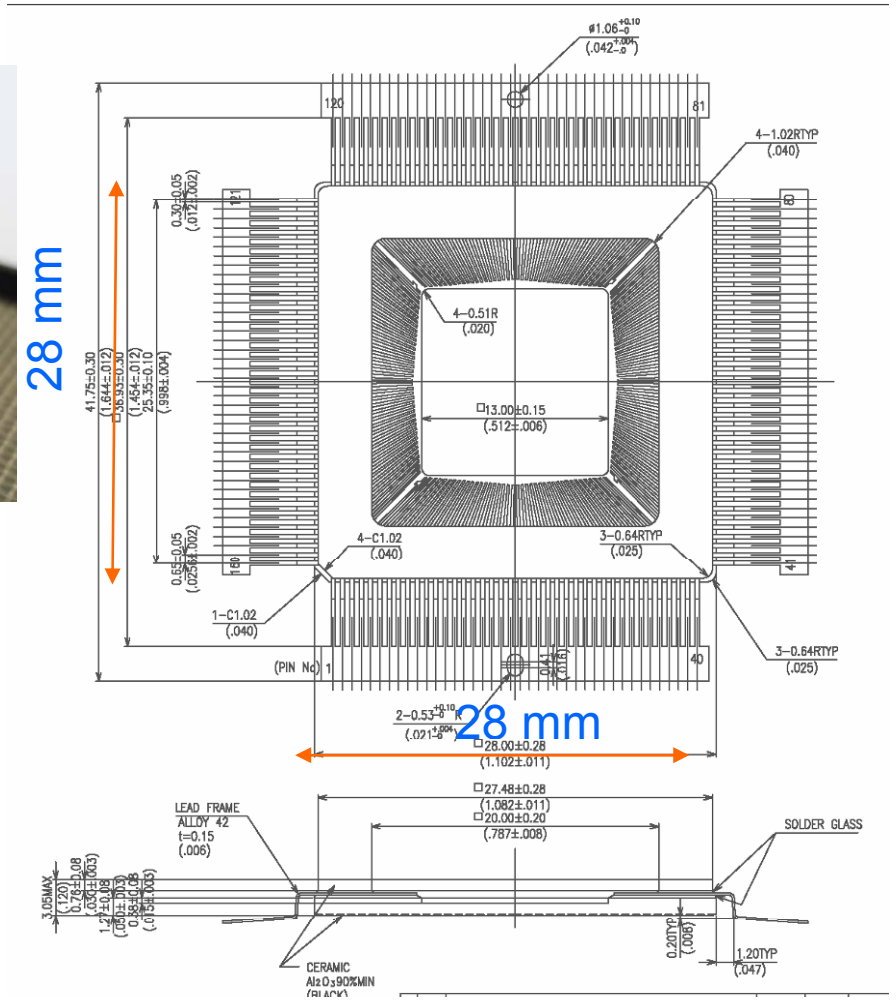
Orsay MicroElectronic Group Associated

HARDROC2

- Hardroc2 submission: mid june 08,
- Delivered end of october 08: 6 packaged chips, 440 naked dies
- Package: QFP160 1single row of pads

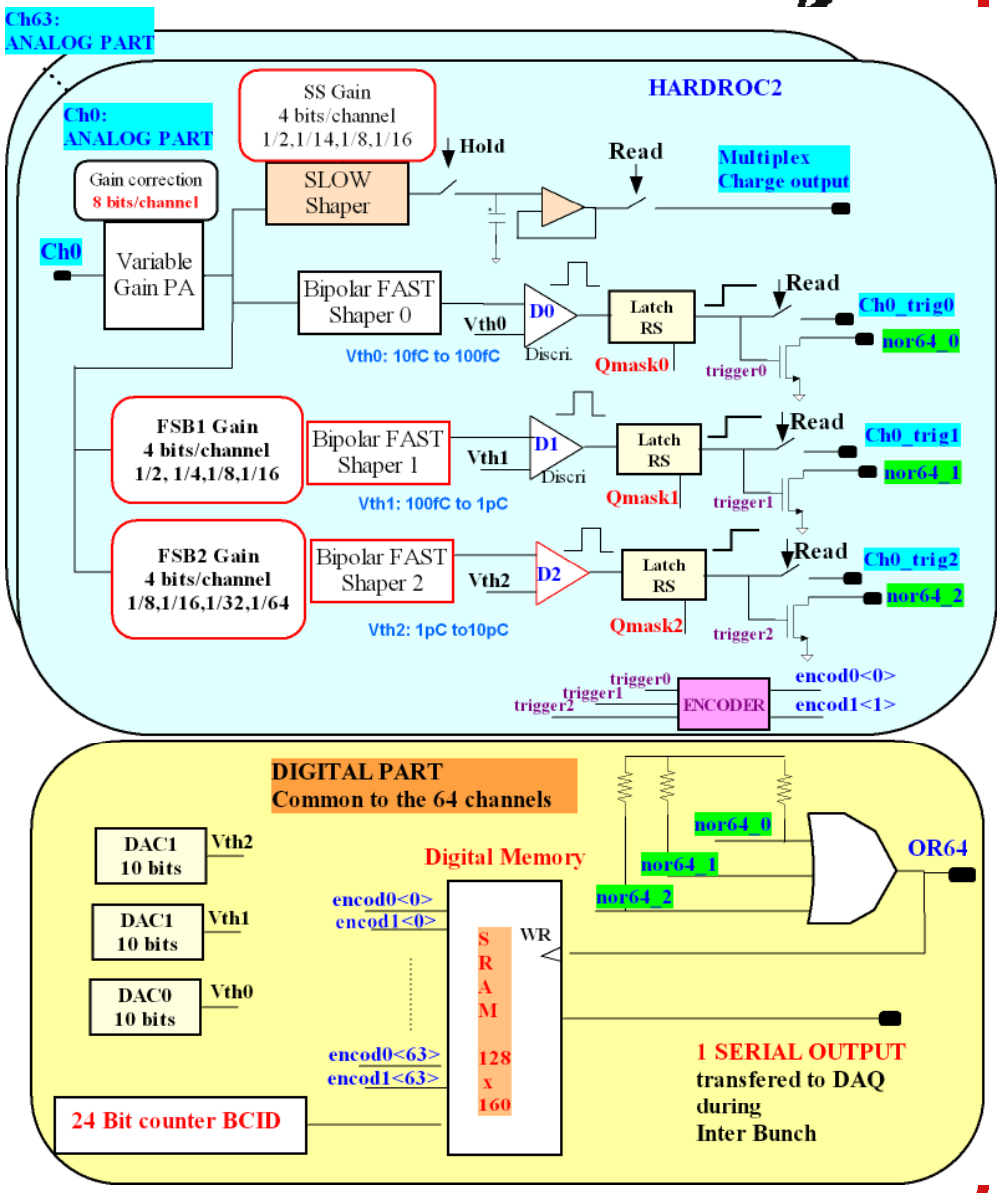


Plastic (Thin QFP): 1.4 mm
(Ceramic: 3.4 mm)



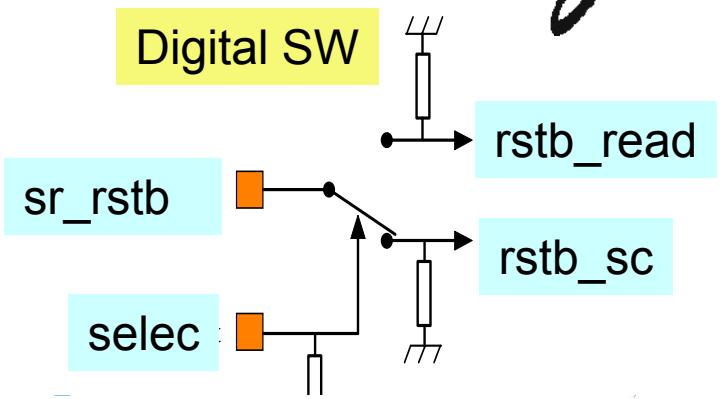
HARDROC2: HARDROC1 +modifs

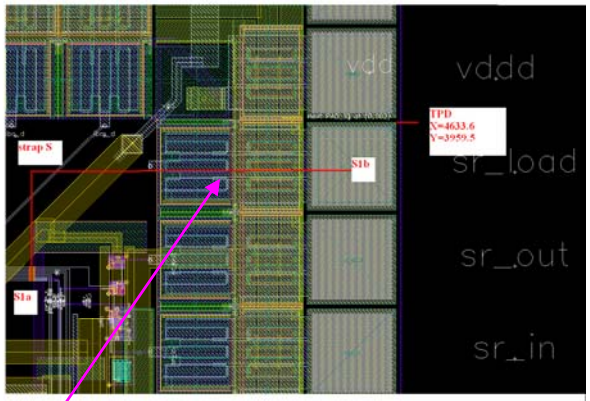
- **Dynamic range extension**
  - Gain correct.: **8 bits** instead of 6: G=0 to 255 (analog G=0 to 2)
  - **3 shapers, different Rf,Cf and gains**:
    - Fsb1, G= ½,**1/4**,1/8,1/16
    - Fsb2, G= 1/8,**1/16**,1/32,1/64
  - **3 thresholds** (=> 3 DACs):
    - 10 fC, 100fC, 1pC (megas)
    - 100fC, 1pC, 10pC (GRPC)
- **Correction** of the minor **bugs** of HR1: MASK, memory pointer (dummy frame)
- **872 SC registers**, default config
- **Power pulsing:**
  - Bandgap (redesigned)+ ref Voltages + master I: power pulsed
  - POD module (power budget)

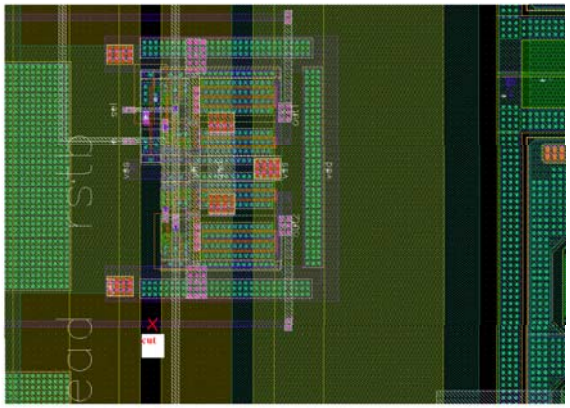


SC/Read pb

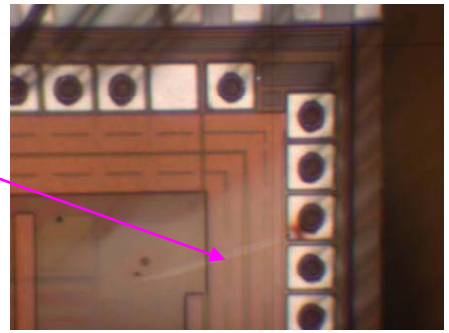
- To spare output PADS and to avoid parasitics on the SC registers, SELEC + switch to deliver:
  - sr_sc, clk_sc, rstb_sc
  - sr_read, clk_read, rstb_read
  - Pb=digital sw and reset active low => reset of the SC registers when SELEC switched on the read register
- Read register not essential but usefull for debug and characterisation => Focused Ion Beam on 2 packaged chips to be able to use the Read register
- SC loading:
  - 872 SC parameters
  - Vddd=4V necessary to load some SC config





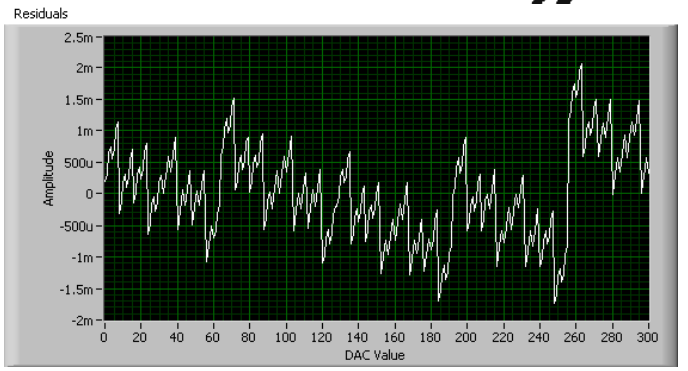


strap

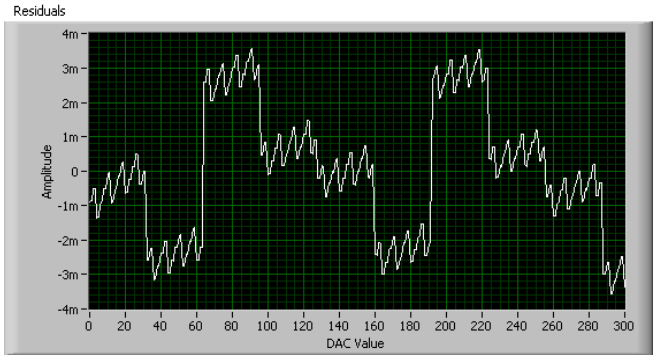


3 10bit-DACs

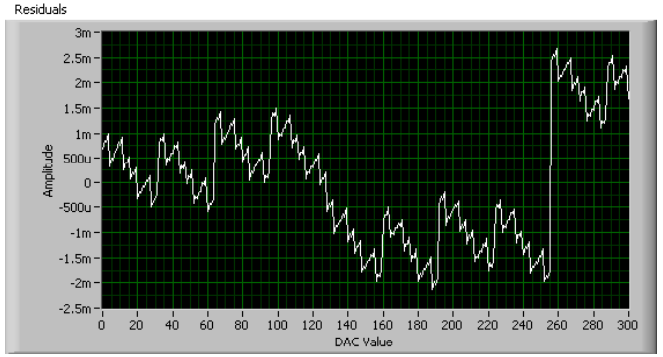
- **DAC0: fine=> -1.1mV/UDAC**
  - Vmax Vmin std
  - 2.3268 1.9966 0.09
- **DAC0: coarse => -2.21mV/UDAC**
  - Vmax Vmin std
  - 2.3271 1.66379 0.192



- **DAC1: coarse => -2.06mV/UDAC**



- **DAC2: coarse => -2.12mV/UDAC**



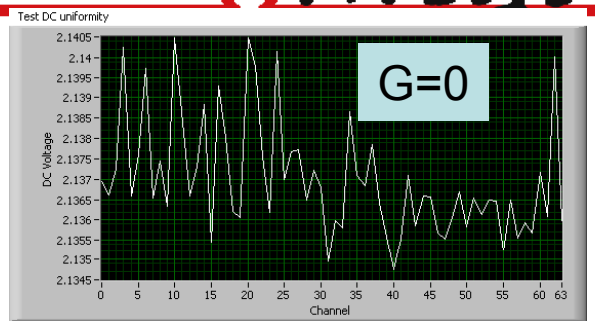
DC FSB0 vs G

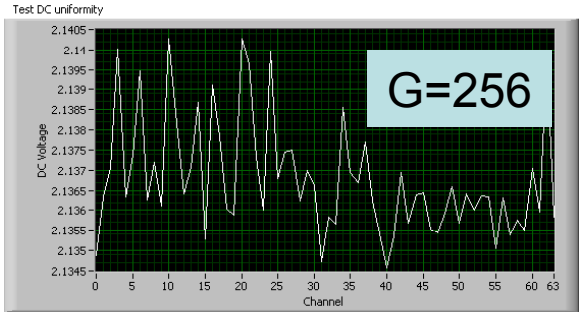
- **FSB0, 150fF, R∞,**
- **G=0**
  - **DC Max** **DC Min** **DC std** **DC Mean**
  - **2.140485** **2.134762** **0.001429** **2.137008**

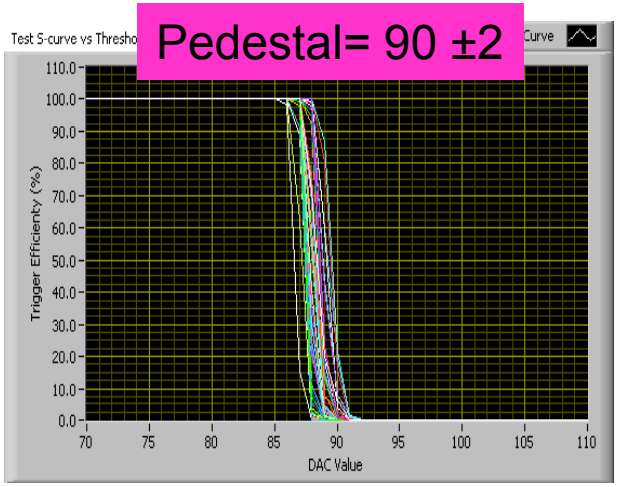
- **G=64:**
  - **DC Max** **DC Min** **DC std** **DC Mean**
  - **2.140636** **2.134892** **0.001437** **2.13714**

- **G=128**
  - **DC Max** **DC Min** **DC std** **DC Mean**
  - **2.140474** **2.134783** **0.001429** **2.136988**

- **G=256:**
  - **DC Max** **DC Min** **DC std** **DC Mean**
  - **2.140275** **2.134576** **0.001440** **2.136798**



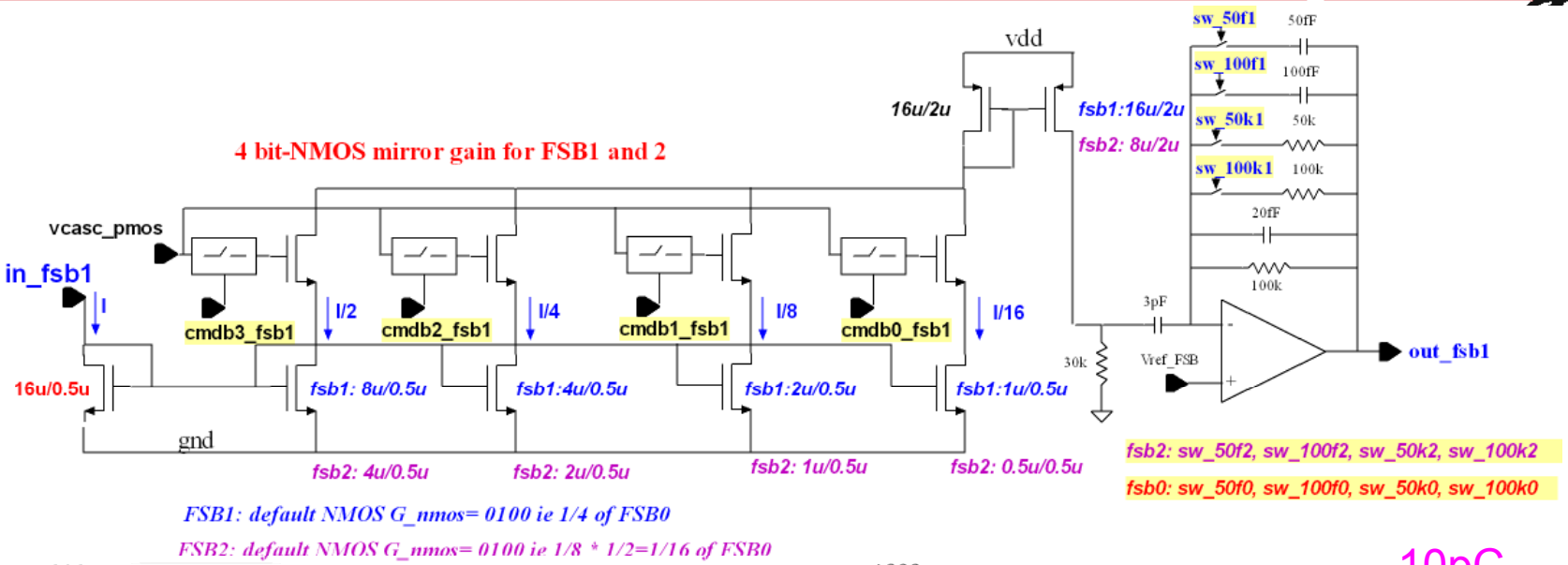




<>dc fsb: Independant of G
<>=2.14V = pedestal equiv. to DAC0 (coarse) ≈90

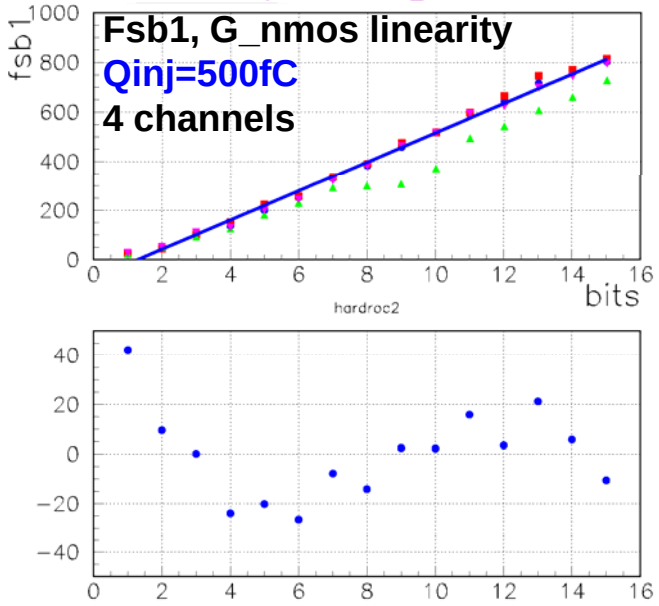
G=0 pedestal= 85 ±2 (peak to peak)
G=128 pedestal= 88±2 (noise envelop)
G=256 pedestal= 92±2

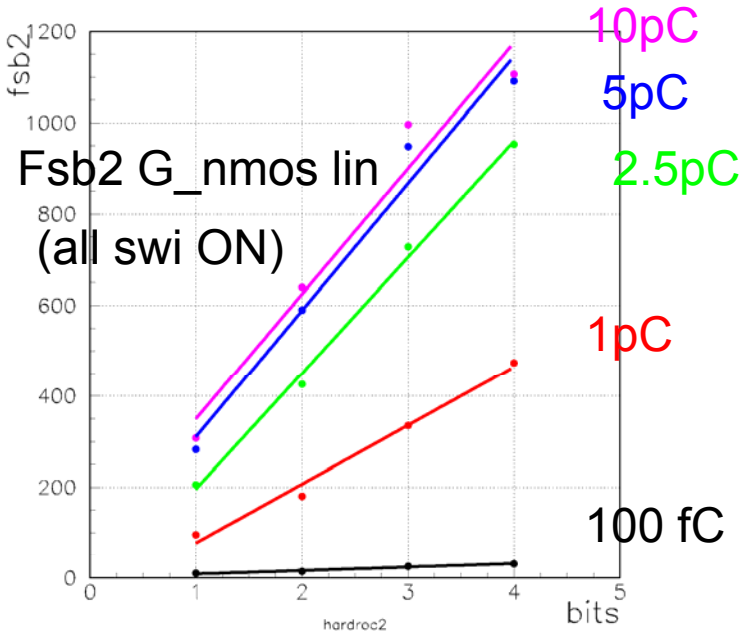
NMOS MIRRORS GAIN of FSB1 and FSB2



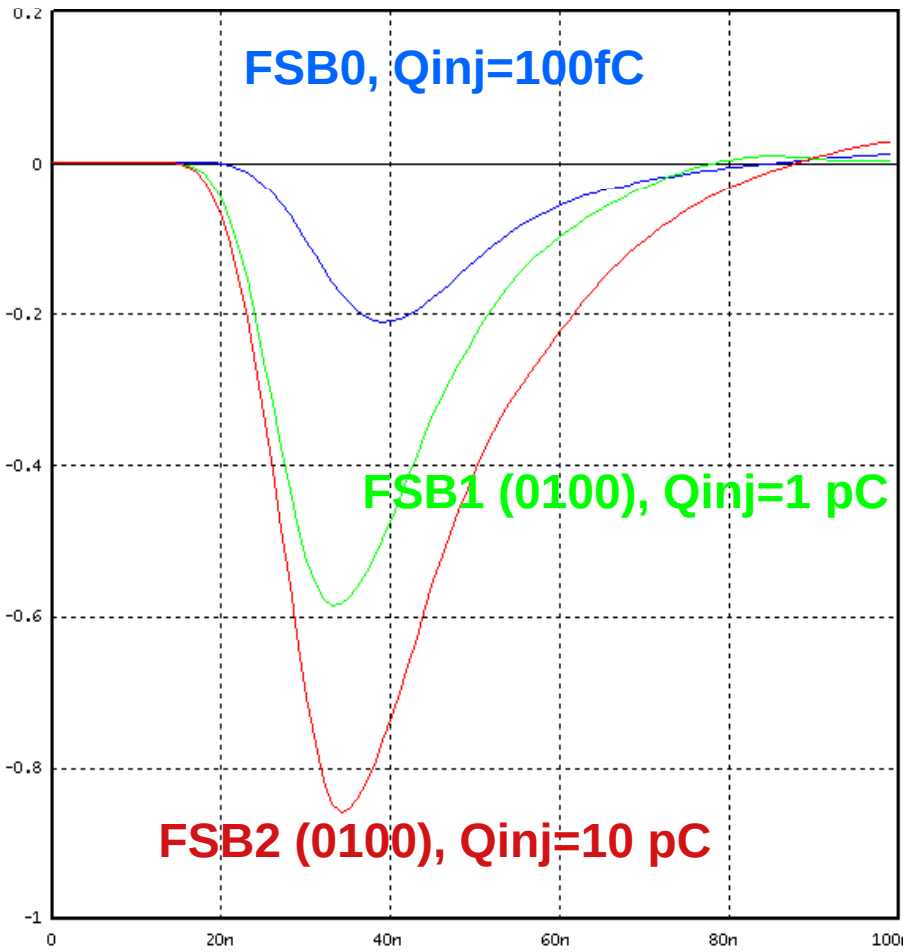
FSB1: default NMOS G_nmos= 0100 ie 1/4 of FSB0

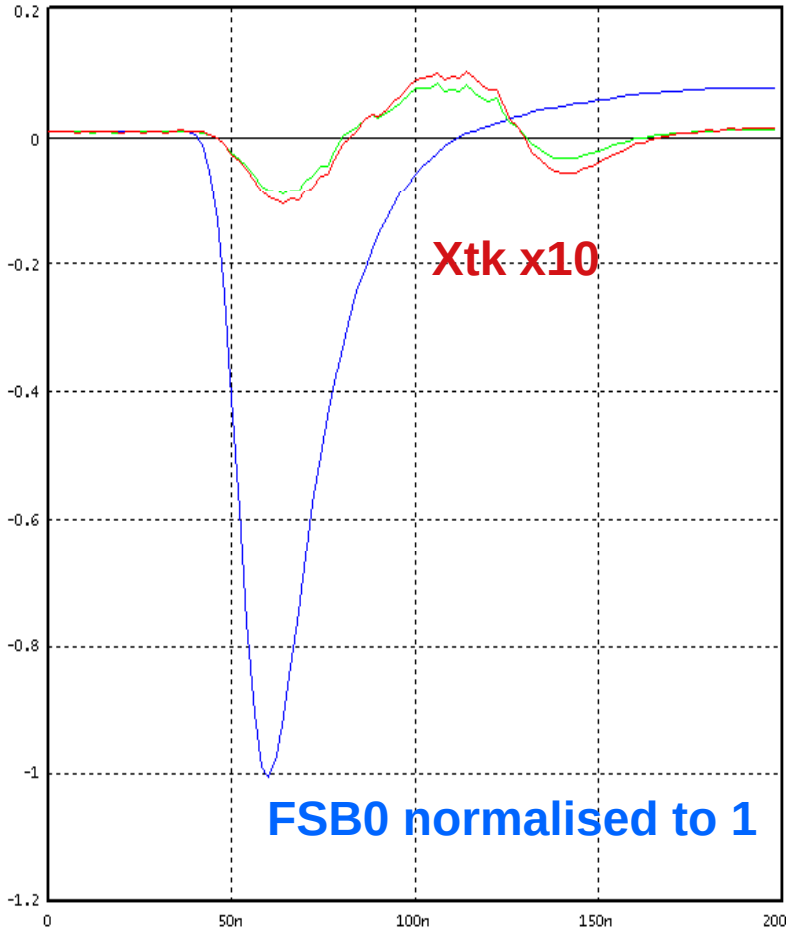
*FSB2: default NMOS G_nmos= 0100 ie 1/8 * 1/2=1/16 of FSB0*





Waveforms and Xtk: scope measurements



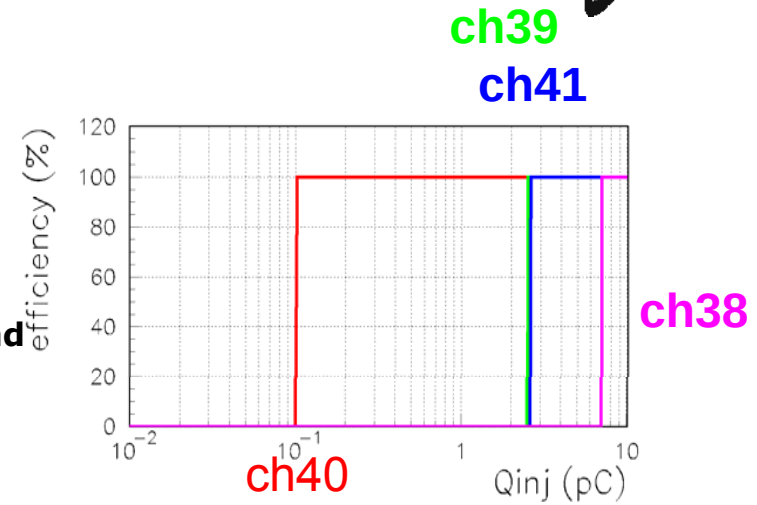


Analog Xtk < 1%

Testboard wo any decoupling cap.

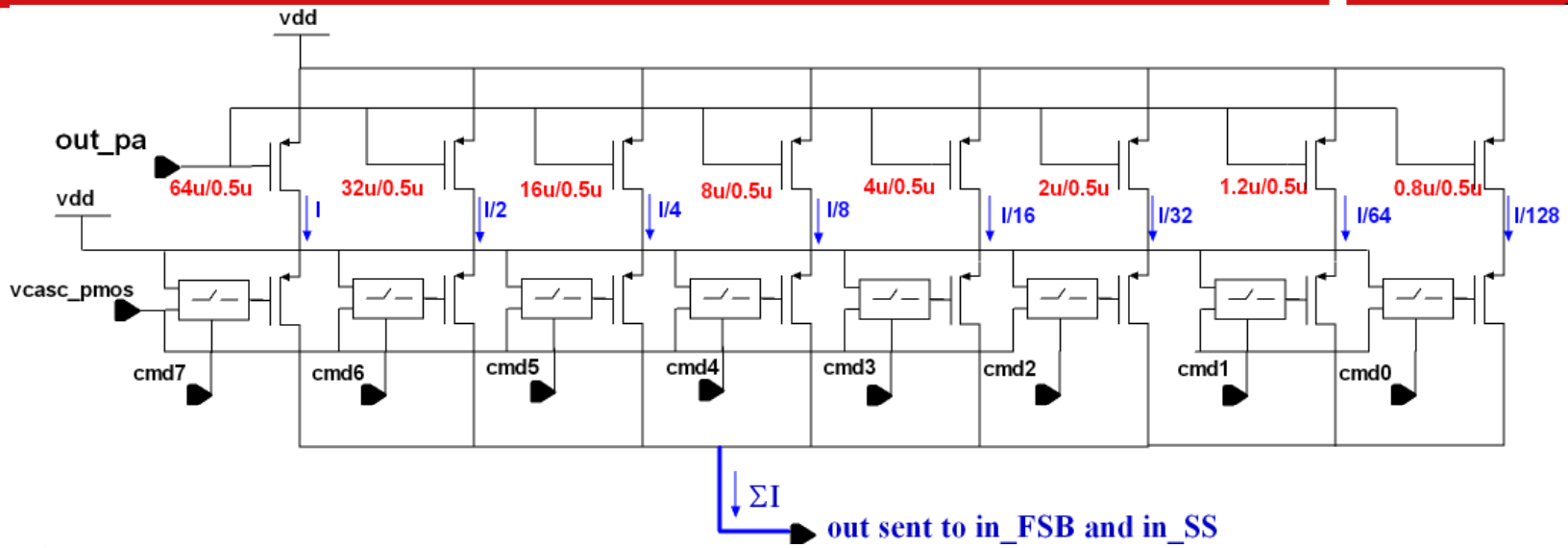
Digital Xtk measurements (board wo DECOUPLING CAP)

- **FSB0 (sw_Cf=100fF, sw_Rf=100k and G=144):**
- **100fC in ch40, Vth0=205=> 200mV, trigger for Vth0<205**
  - **Qinj=1pC (1V@20dB in 10pF), no trigger on direct neighbours**
  - **Qinj> 2.5pC (fsb0 sature), trigger on ch39 and ch41 ie 4%**
  - **Qinj>7pC (fsb0 sature), trigger on ch38,39 and 41,42**
  - **Qinj>56pC, triggers on 37,38,39 and 41,42**
  - **100pC, triggers on ch 34,35,36,37,38,39 and ch 41,42,43,44,45,46**

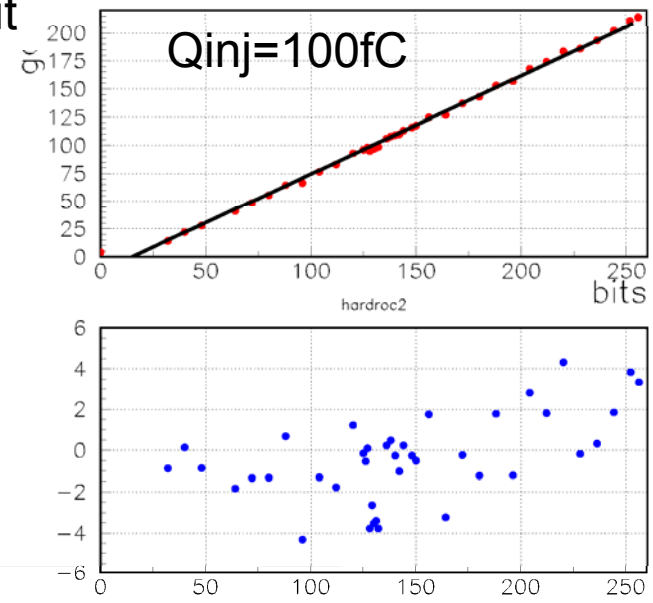


- **FSB1 (50f,100fF,100k,50k and G=144 and Gnmos=1000):**
- **1pC, Vth1=443=> 730mV, trigger for Vth1<445**
  - **Qinj=1pC (1V@20dB in 10pF), no trigger on direct neighbors**
  - **Qinj> 56p, trigger on ch39 and 41**
  - **100pC, triggers on ch39 and ch 41**
- **FSB2 (50f,100fF,100k,50k and G=144 and Gnmos=0010):**
- **10pC, Vth2=230=> 730mV, trigger for Vth2<233**
  - **Qinj=1pC (1V@20dB in 10pF), no trigger on direct neighbors**
  - **Qinj=100pC, no triggers on neighbours**

8bit PMOS MIRRORS: linearity measurement



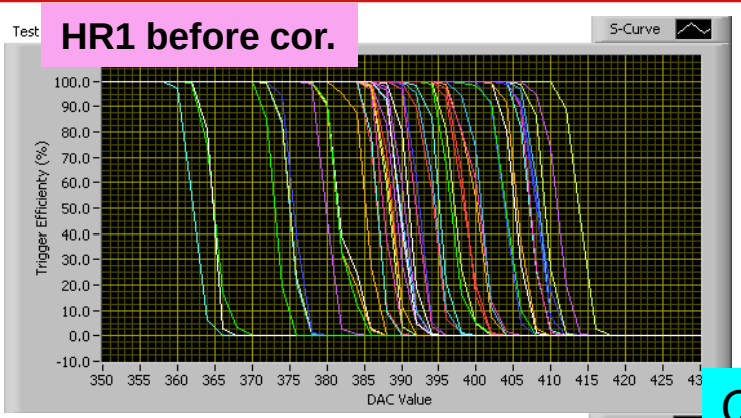
Vout



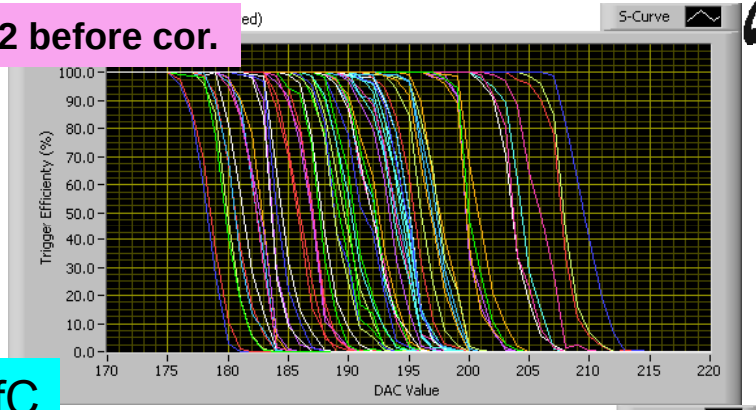
- Allows accomodating the gain according to the detector choice
- PMOS gain: 8 bits/channel
  - Binary G_b= 0 to 255
  - Analog G = 0 to 2
- Current mirrors mismatch between channels (small size transistors to optimise the speed): layout redone in HR2 to improve the uniformity

FSB0 scurves: HR1 /HR2 before and after gain correction

HR1 before cor.

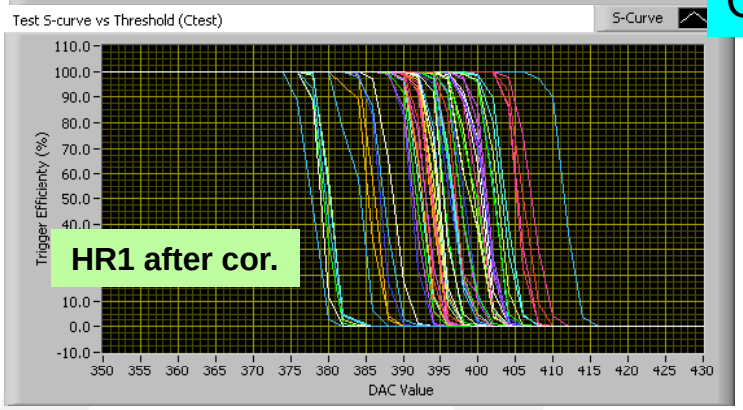


HR2 before cor.

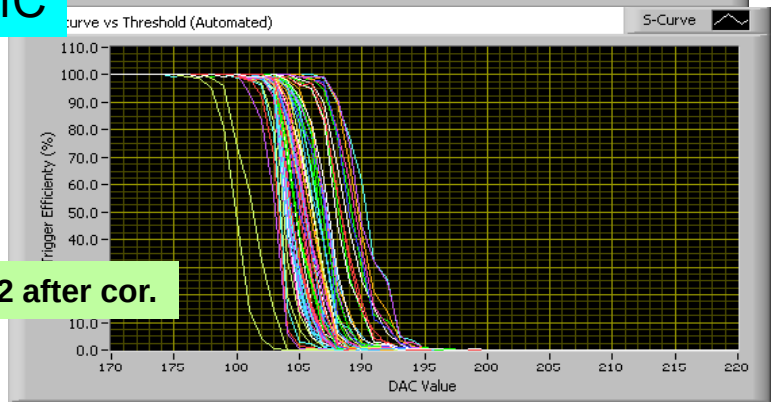


Qinj=100fC

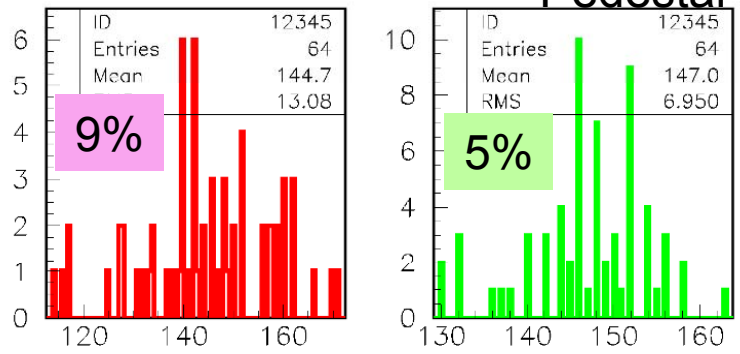
HR1 after cor.

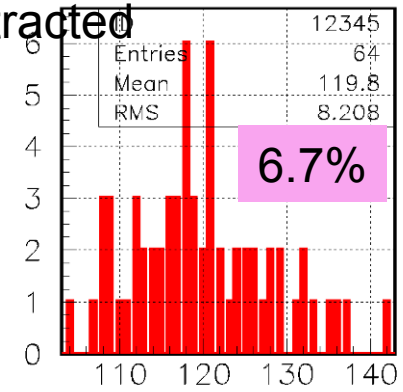


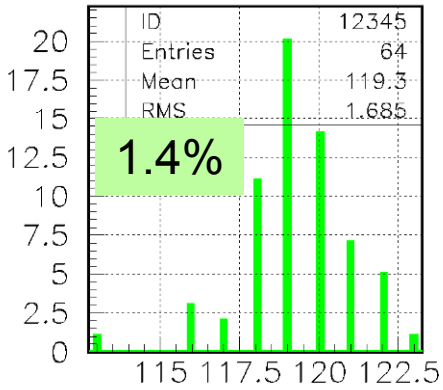
HR2 after cor.



Pedestal substracted

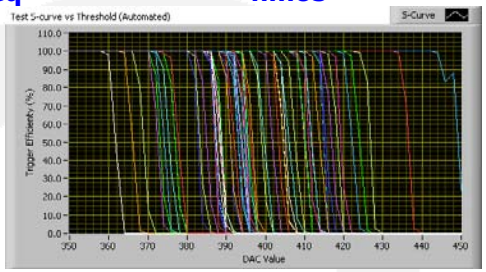




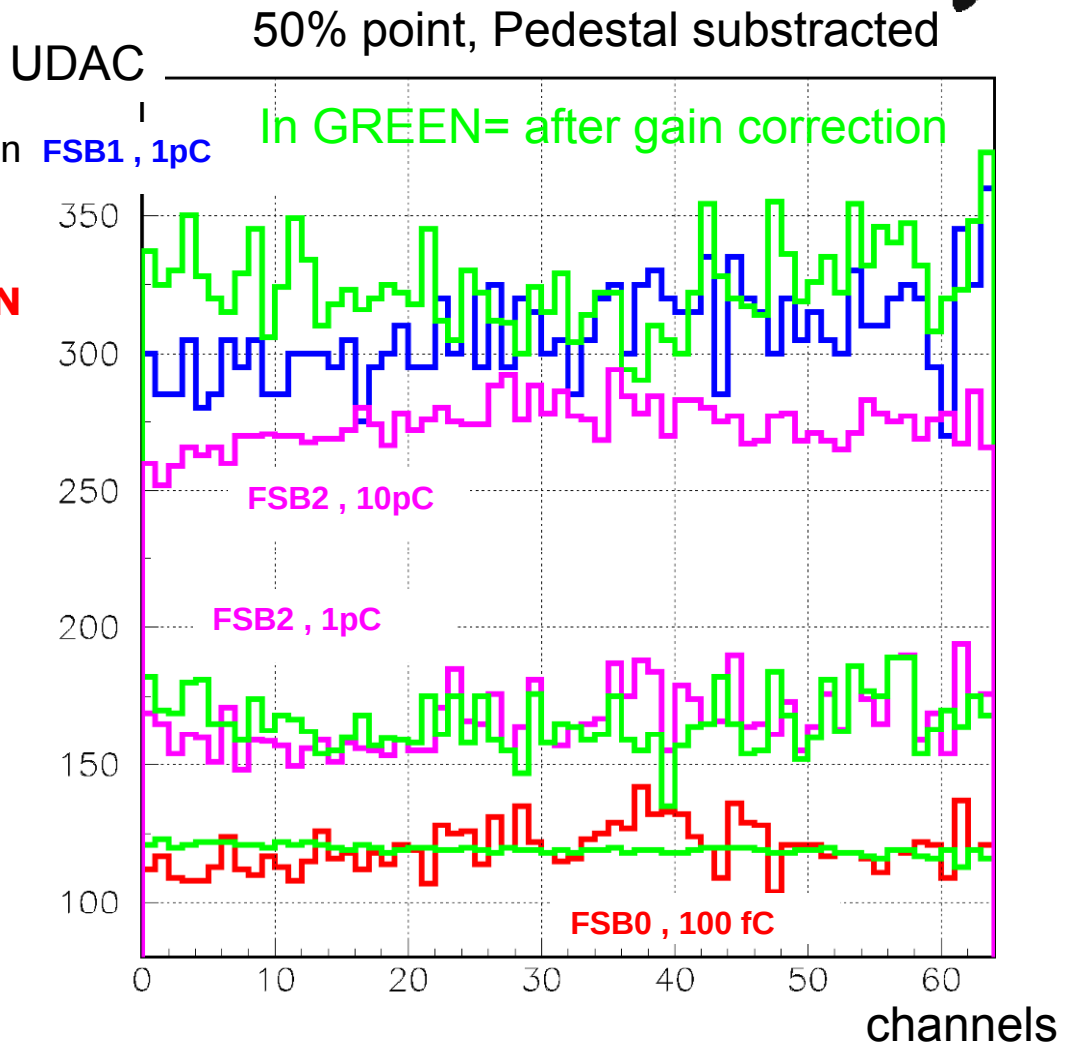


SCURVES: FSB0,1,2

- Gain=144 (Ga=1.125) for all channels before correction
- Gain correction for each channel on FSB0
- **FSB0, Cf=100f and Rf=100K ON (Cf_{eq}=120fF, Rf_{eq}=50K), Qinj=100fC**
- **FSB1, all Rf, Cf on (Rf_{eq}=25K, Cf_{eq}=170fF), G_{nmos}=1000, 1pC**



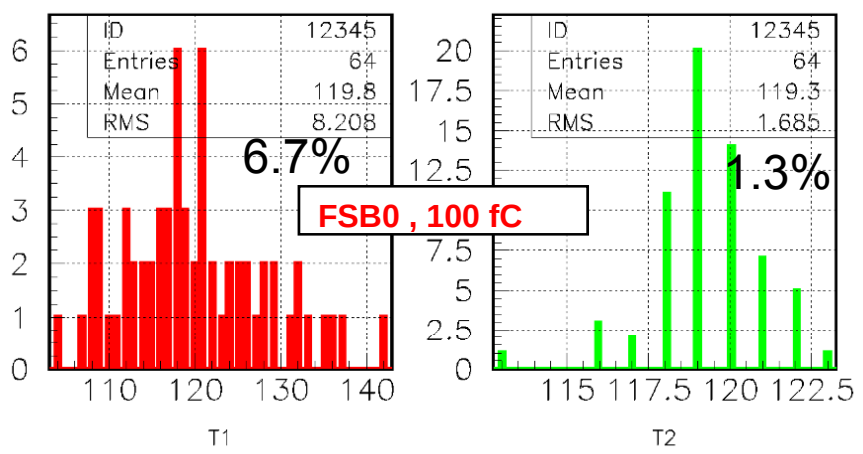
- **FSB2, Qinj=1pC, Cf=100f (Rf_{eq}=100K, Cf_{eq}=120fF), G_{nmos}=1000, G=144**
- **FSB2,Qinj=10pC (Cinj), all swi ON (Cf_{eq}=170fF, Rf_{eq}=25K, G_{nmos}=0010, G=144**

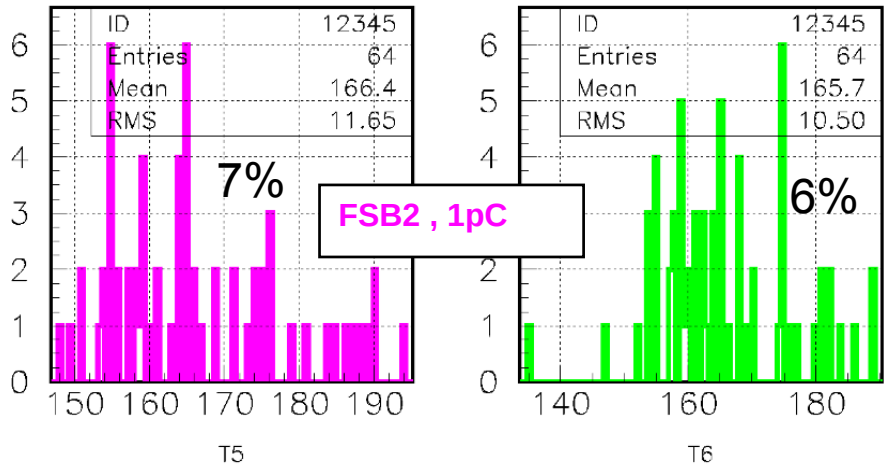


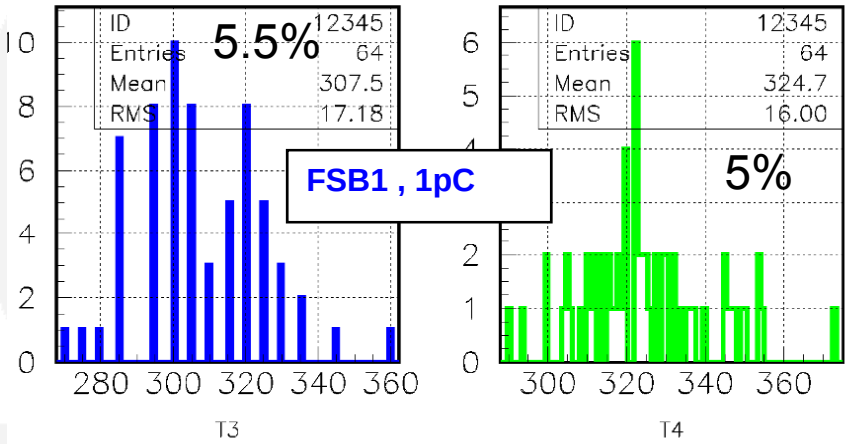
SCURVES: FSB0,1,2

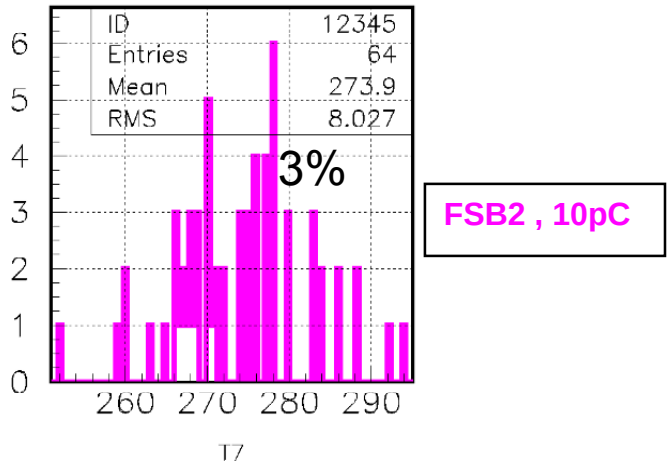
- Gain=144 for all channels before correction
- Gain correction performed for each channel on FSB0, not efficient on FSB1 and FSB2 as non uniformity is dominated by non uniformity of NMOS mirrors used to change Gnmos

In GREEN= after gain correction







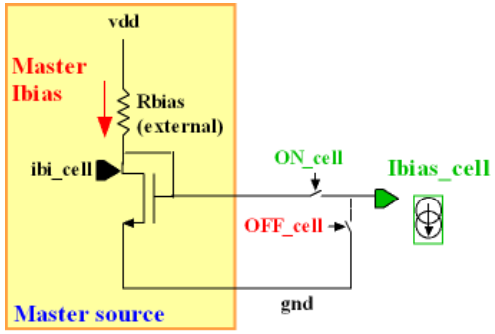


POWER CONSUMPTION

PA	5.46mA	DAC	0.84mA
3 FSB	12.3mA	BG	1.2mA
SS	*9.3mA*	vddd	0.67mA
3 Discris	7.3mA	vddd2	0.4mA (=0 if 40MHz OFF)
TOTAL	38mA		

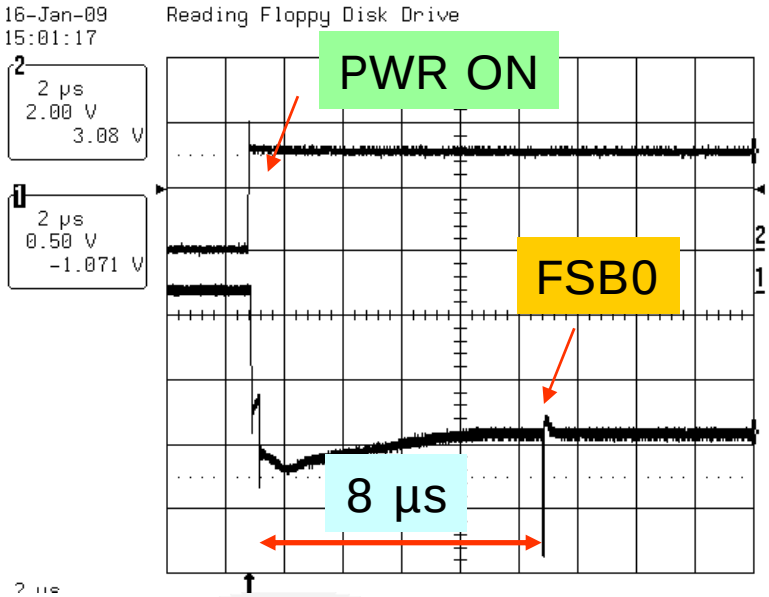
Pwr_on_a alone	14.9mA
Pwr_on_dac	1.025mA
Pwr_on_d	0.93mA
ALL ON	17 mA
ALL OFF	**<4µA**

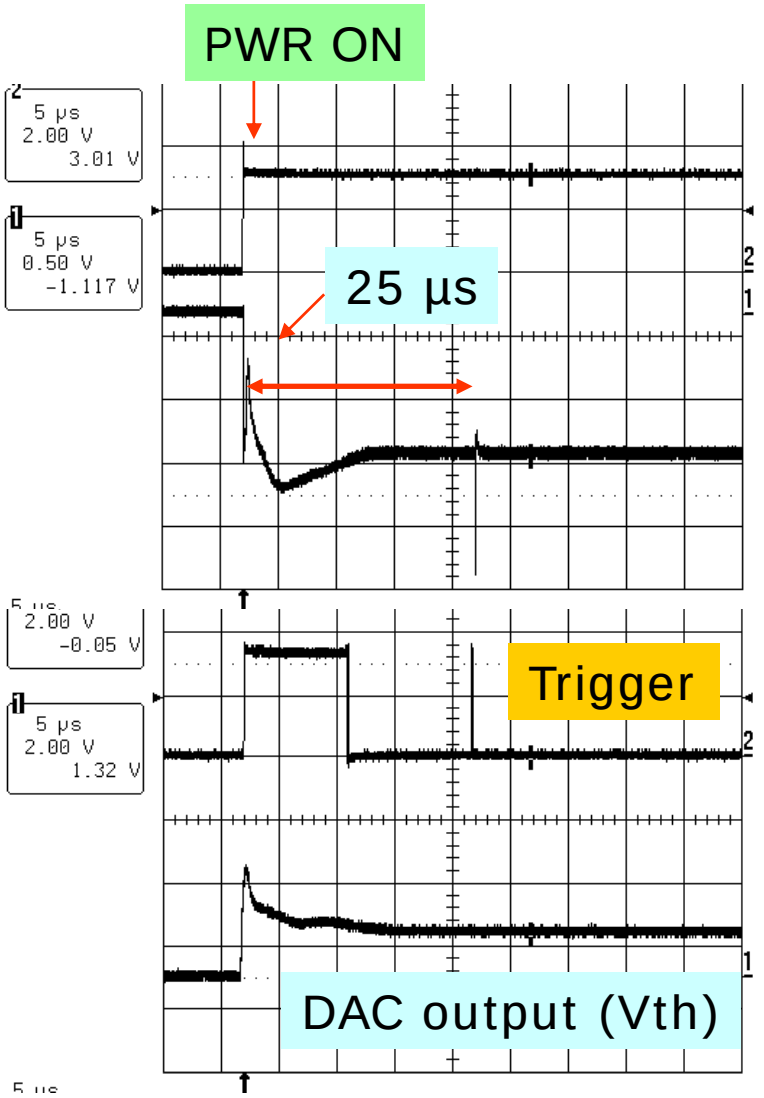
- **Maximum power available:**
  - **10 µW/ch with 0.5% duty cycle**
  - **=> 640µW/3.5V=180 µA for the entire chip**
  - **OFF= Ibias _cell switched off during interbunch**
  - **SW added in HR2 to switch off all the master Ibias, Vref, V_BG…**



- **Without SS:**
  - 38-9=29mAx3.3V≈100mW
  - **1.5mW/ch**
  - **7.5 µW/ch with 0.5% duty cycle**

Power pulsing of HR2: « Awake » time

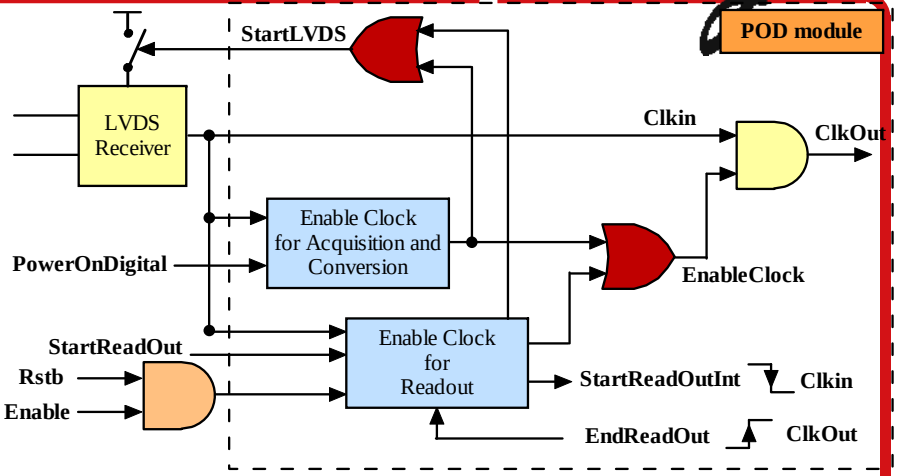


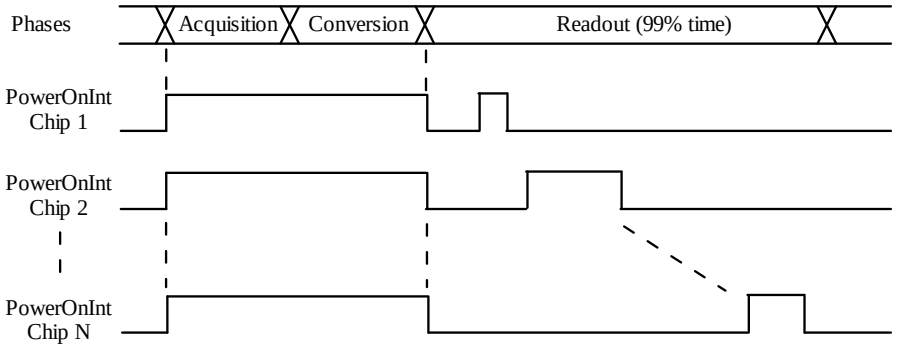


- **PWR ON: ILC like (1ms,199ms)**
- **All decoupling capacitors removed**
- **PP of the analog part:**
  - **Input signal synchronised on PWR ON**
  - **=> Awake time= 8 µs**
- **Power pulsing of the DAC:**
  - **25 µs (slew rate limited)**

Power On Digital:

- PowerON start/stop clocks and LVDS receiver bias current to meet power budget.
- LVDS receivers for RazChn/NoTrig and ValEvt ON during PowerOnAnalog (during bunch crossing)
- Clock is started asynchronously, enabled and stopped synchronously (at '0')
- 2 operation modes :
  - Acquisition, Conversion ➔ common to all managed by DAQ
  - Readout ➔ daisy chained managed by StartReadOut and EndReadOut





• POD successfully tested on testbench

CONCLUSION

- HR1 bugs corrected:
  - Mask, pointer
  - 0.5% duty cycle pwr pulsing: pwr <8µW per channel
  - Better uniformity between channels before correction: 7%, down to 1.5% (fsb0) after correction
  - Scurves@ 1pC and 10 pC OK, dispersion=5%

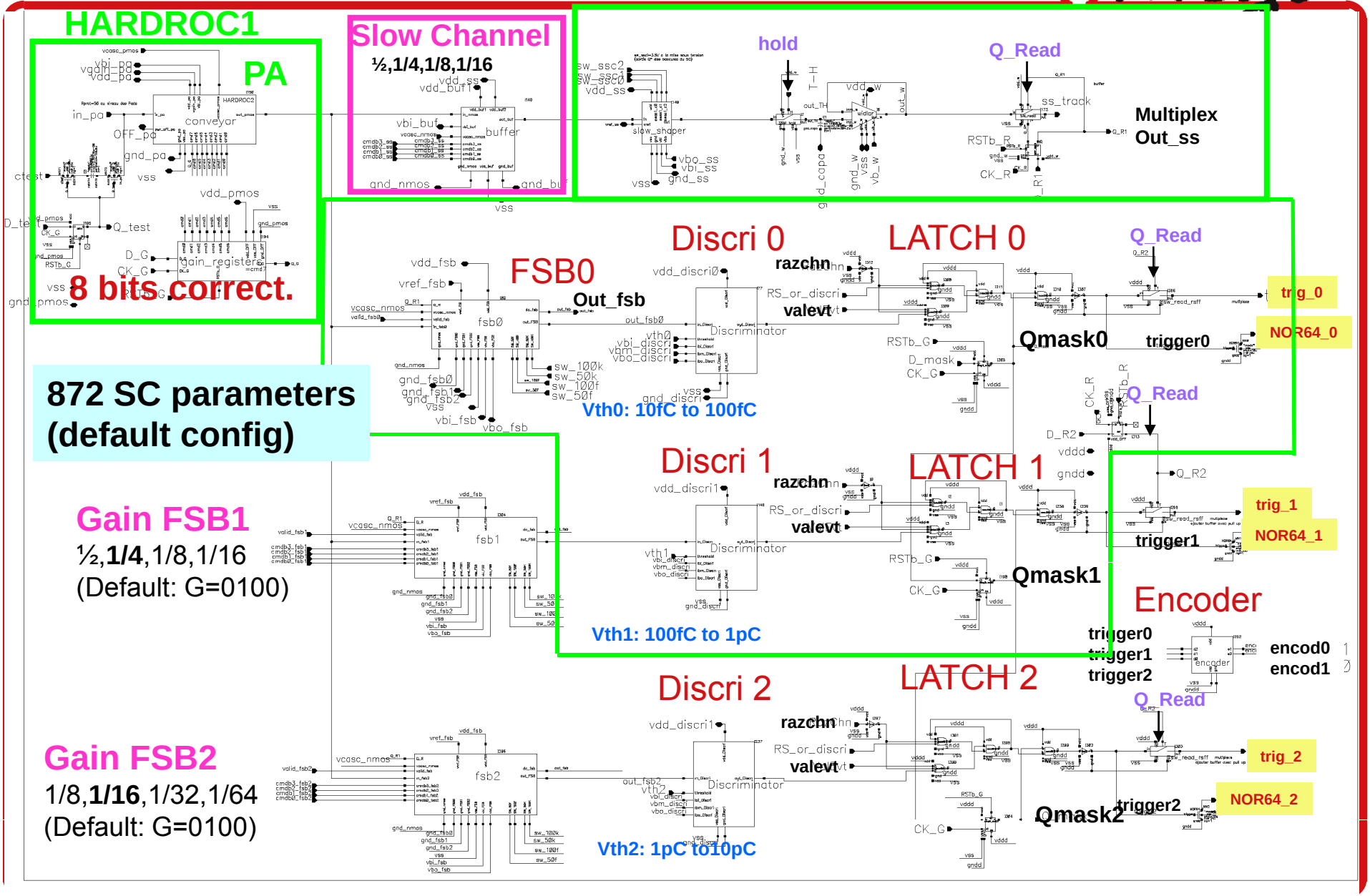
- HR2: suitable for m^2 (No analog output)

- 400 HR2 are in I2A packaging company (USA) to be packaged in plastic TQFP160.
- Must be TESTED (=characterisation=>30minutes/chip)

- Power pulsing tested on testbench. To be tested in test beam

ANNEX

HARDROC2: analog part



HR2 in TQFP160