Status of the DHCAL 1m2 GRPC Acquisition

C. Combaret

IPNL

Status on january 20th

- Setup with :
  - 1 IPNL PCB (24 hardrocs), GRPC
  - 1 IPNL slab made of 2 IPNL PCBs
  - 1 DAQ PC (Dell Poweredge 2950) running SL5
  - 1 laptop for user interface
  - XDAQ software running on the DAQ PC

Status on january, 20th: Breakdown problem

- Breakdown problem :

  During november beam test several Hardrocs died because of breakdowns linked to accumulated charges on the GRPC detector.

  All slabs have been investigated (electronic point of view). Procedure was :

  Does slow control work on this slab ?

  If not which asic(s) does (do) not propagate the SLC data?

  Short SLC of faulty asic(s)

  Then individual check of polarisation of every pad input of every hardroc of every slab (ie 9216 inputs…)

  Asics with dead slow control have been replaced.

  Asics with only few dead channels have been kept

Status on january, 20th: Breakdown problem

Card 1

149			135	106	103	
		146	147	111	116	
		126		129		DIF
148	123			117		

Card 2

217	235	239	236	230	247	
224	238	242	245	234	219	
228	241	229	240	237	225	DIF
231	152	233	227	243	220	

Card 3

162	169	163	137	153	177	
166	318	173	144	156	218	
172	317	164	154	161	263	DIF
175	159	170	315	174	314	

card 4

287	282	279	277	290	289	
291	278	295	280	296	303	
294	281	299	284	300	302	DIF
297	285	293	286	292	304	

Card 5

198	179	204	178	216	196	
191	180	184	182	211	215	
207	185	190	188	201	208	DIF
195	199	203	193	200	244	

Card 6

262	267	264	248	253	273	
266	252	272	251	257	276	
271	256	275	254	261	249	DIF
274	260	268	259	115	265	

Card 1 was connected to the readout

Other cards were left unconnected

NB: Blanks on card 1 are for hardrocs whose sticker is missing or unreadable

Status on january 20th : long slabs

2 PCBs with 24 hardrocs have been connected together.

→ Works OK (SLC and digital readout) after a few weeks of tests and adjustements

Most (not to say all) problems come from long transmission lines and their consequences

What is mandatory :

All foreseen buffers on the PCB shall be used

SLC : Additional buffers on slc_clk

All touchy lines must be correctly adaptated to avoid reflexions

Digital readout : Data line capacitance forces to reduce the readout speed (2,5MHz instead of 5MHz)

In next versions of the PCB, parasitic capacitance of open drain lines shall be kept as low as possible.

Status on january 20th : long slabs

DIF

Slab 1

Slab 2

PCBs conected with 0 ohms resistors

Status on january 20th : what next?

XDAQ Software with Hardroc asics is functional

DIF with one Hardroc PCB is functional

2 PCB can be connected together to make a 1m long functional slab with 48 hardroc

So, we need to put all this on one 1m2 RPC detector!