Laboratoire d'Annecy-le-Vieux
de Physique des Particules

LAPP electronic status for DHCAL

20 janvier 2009
DHCAL meeting at LLR

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CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

IN2P3
INSTITUT NATIONAL DE PHYSIQUE NUCLÉAIRE ET DE PHYSIQUE DES PARTICULES

UNIVERSITE CHAMBERY ANNECY SAVOIE

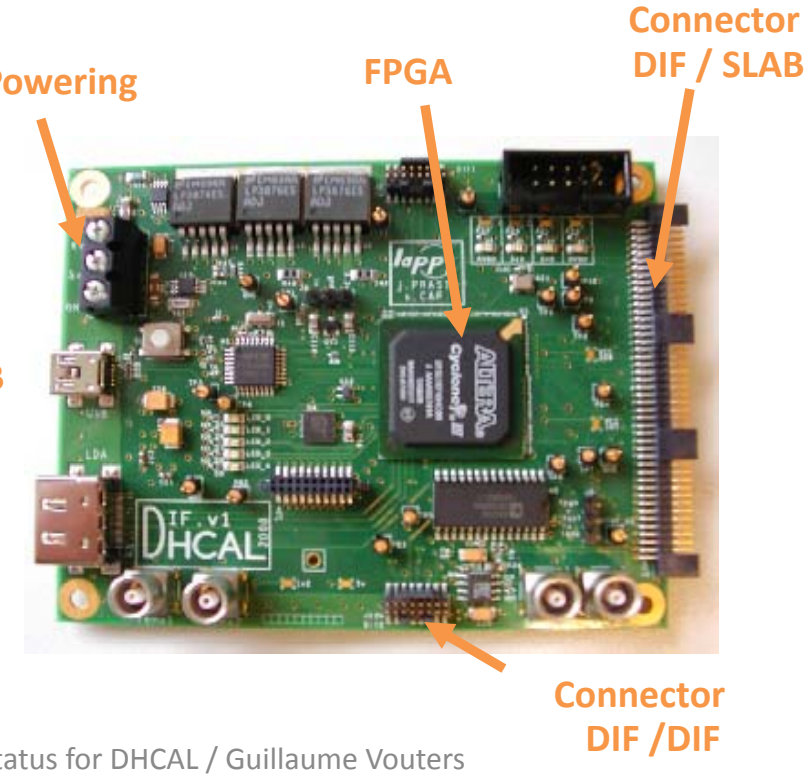
Summary

- **DIF (Digital InterFace)**
  - Cap Sébastien, Prast Julie, Vouters Guillaume.
- **MicroMEGAS ASU (Active Sensor Unit) with HARDROC 1/2 or DIRAC**
  - Dalmaz Alexandre, Drancourt Cyril.
- **Beam Test**
  - LAPP MicroMEGAS team
- **On Going works**

DIF (Digital InterFace)

DIF board :

- Independent board to have more flexibility
- It provides the communication with HARDROCs or DIRACs
- It allows ASICs configuration and performs analog and digital readout
- Also compatible with SPIROC and SKYROC (ECAL and AHCAL)
- Two DAQs :
  - Through USB : Cross DAQ
  - Through HDMI : Calice DAQ

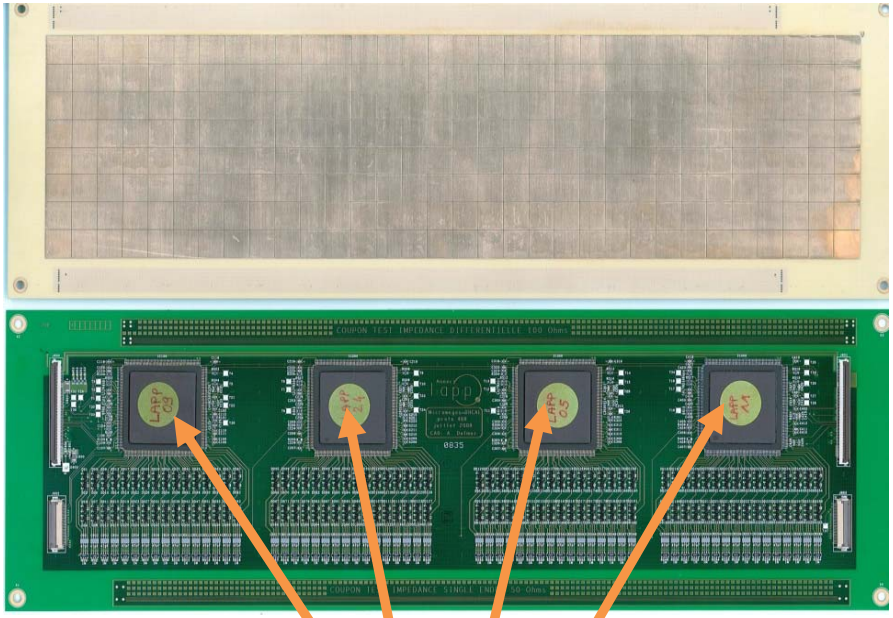


ASU for MicroMEGAS

ASU board with HARDROC 1 (8x32cm², 1cm² pad)

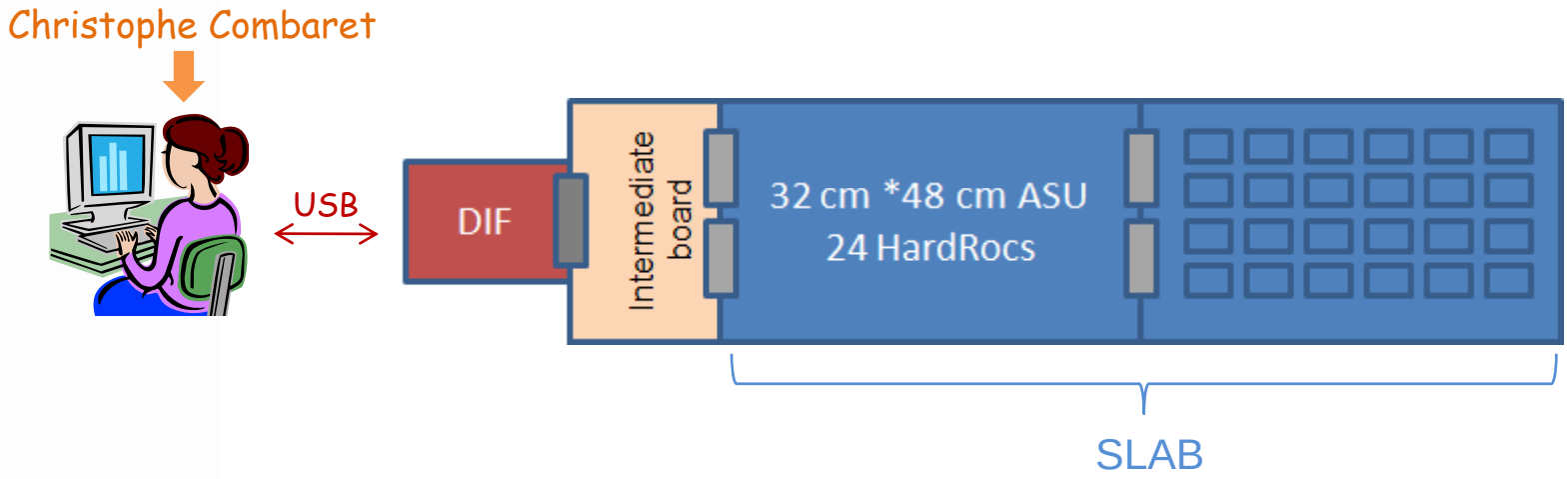
- 8 layers with careful routing to avoid crosstalk
- Sparks protections included

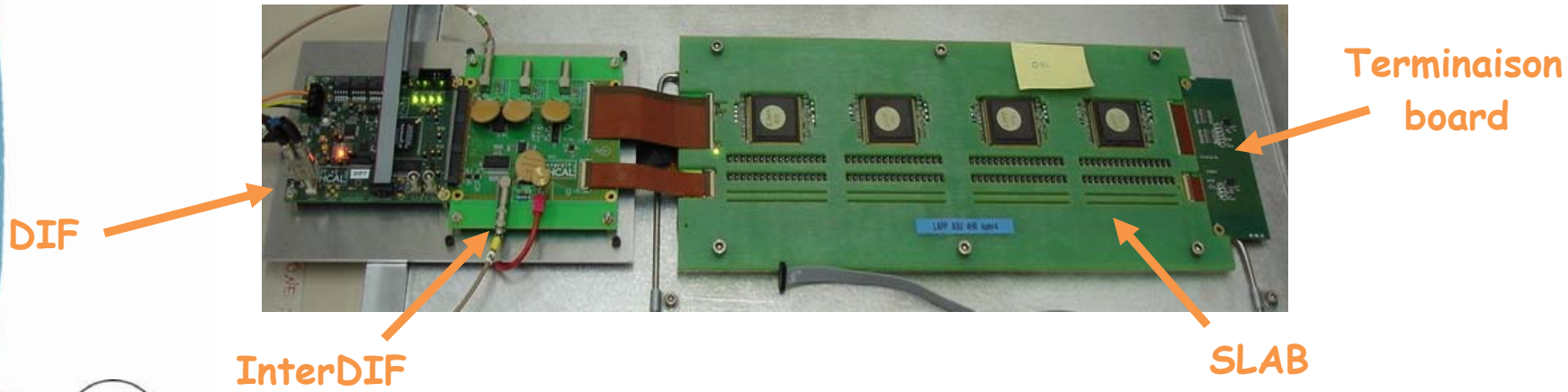
- HARDROC 1 (16 mm²)
  - Analog and digital readout
  - 64 channels
  - 2 thresholds in 10 bit precision
  - Digital memory for 128 events
  - Dynamic Range – 10 fC to 1 pC
  - Low consumption < 10µW/channel



4 HARDROC for 8x32 pads

The DHCAL Architecture For MicroMEGAS





Preliminary Tests at LAPP

First tests with DIF

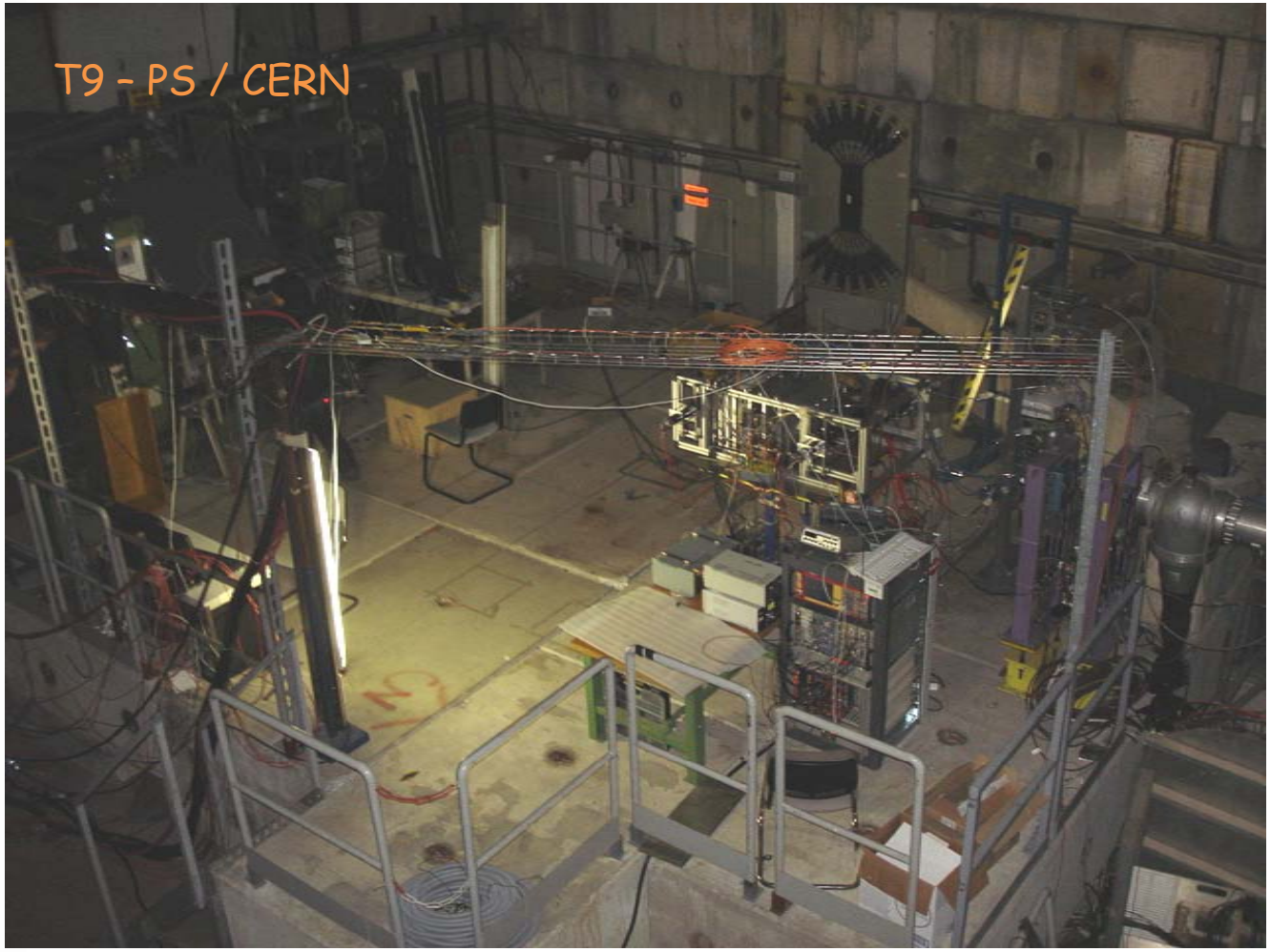
- All DIF are fully operationnal
- Command and register acces : ok
- Monitoring : ok
- Calibration of HARDROCs and Power Pulsing : not develop yet

First tests with ASU

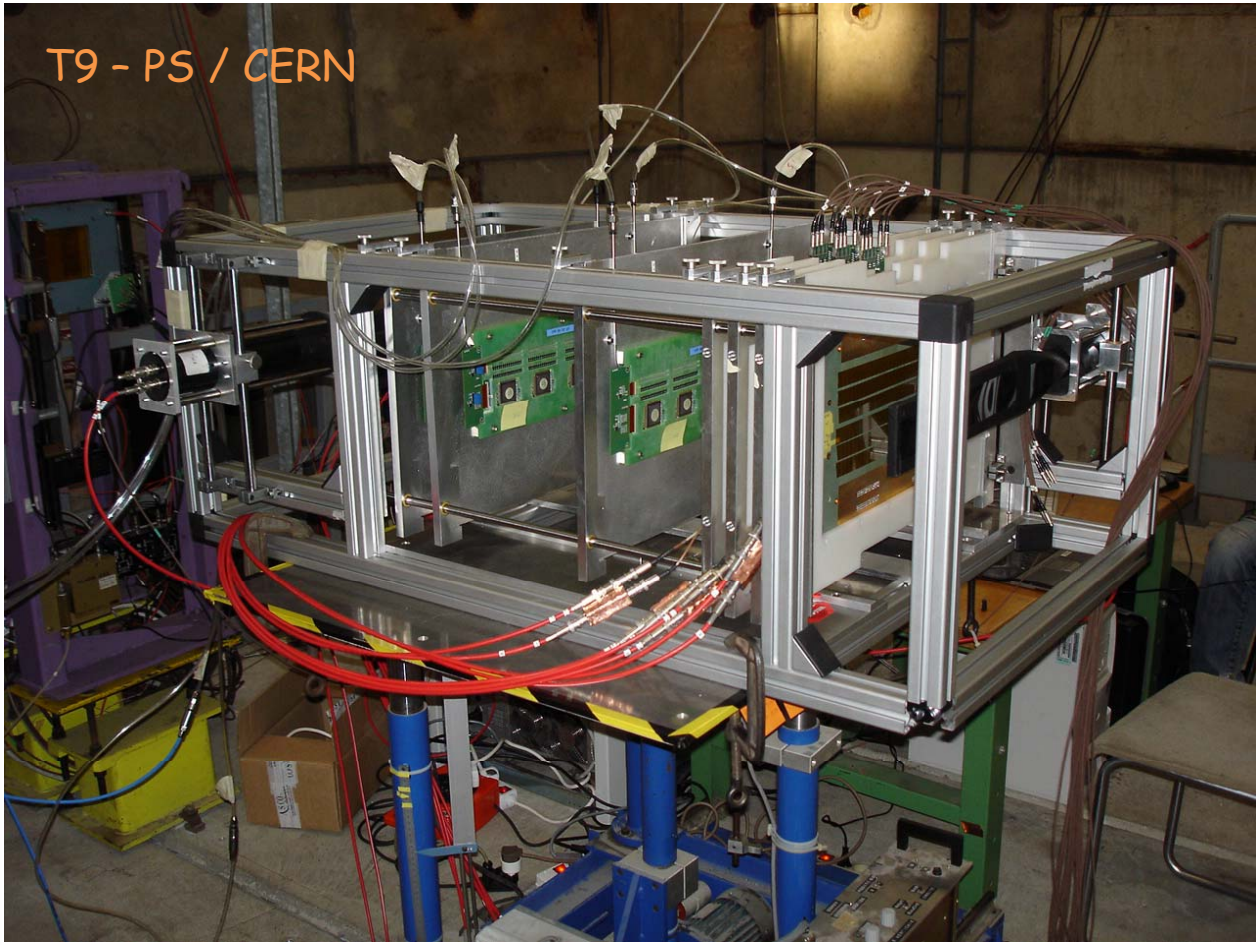
- 2 ASUs are fully fonctionnal
- 1 ASU : ASIC configuration doesn't work
- 1 ASU had a dysfunctionnal HARDROC
- 3 ASUs brought for the beam test

ASU was ready to test less than one month before the start of the Beam Test. We had less than one month to make electronics ready for the Beam test.

2008 November Beam Test



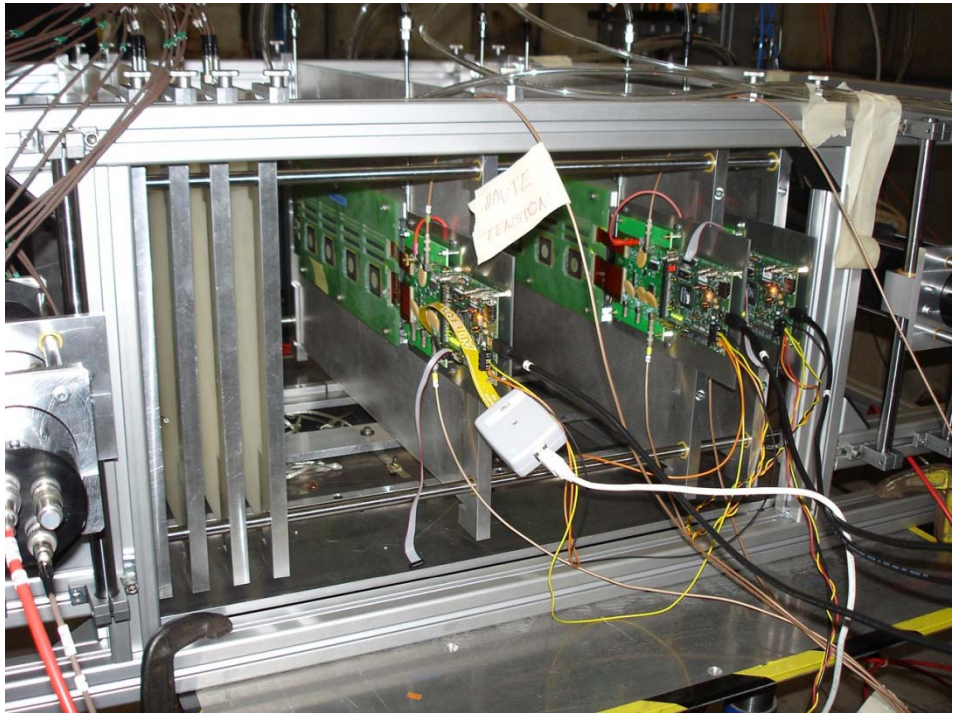
2008 November Beam Test



Installation

Setup with

- 3 (ASU+DIF) connected to the DAQ through a USB hub



Results

Configuration of ASICs (Slow Control)

- Tested with all HARDROC
- Checked by controling dac values and the DIF firmware

→ Stable and reliable

(tested also with 24 HARDROCs from the IPNL ASU)

Synchronisation of the 3 DIFs

- Synchronization of 5MHz clock and reset BCID
- Synchronization of the start of digital readout for several DIF

→ Stable and reliable

→ First time that several (DIF+ASU) were synchronized !!

Results

Digital Readout

- Tested with the manual and trig_ext/trig_int mode
- Tested with the automatic and trig_ext /trig_int mode
- Tested with the Beam Test mode

→ Stable and reliable

(tested also with 24 HARDROCs from the IPNL ASU)

Beam test mode

- Start Acquisition
- HARDROC data memorisation
- Erasing memory if there is a full HARDROC memory
- Read out if there is a particle(trigger)

Analog Readout

- Not tested

Data taken

The DIF developed features worked with all ASU but mesh high voltage was only stable on one ASU…

… so beam data were taken only with one ASU.

Data analysis is on going (LAPP/LLR) !

Observed noise :

→ 200 DAC value = 145fC

→ 150 DAC value = 100fC

Data format

<Format version = 2>
<Timestamp>
<Header global numérique>
<ID DIF>
<Counter trigger>
<Counter particule>
<Header data HARDROC1> <data HARDROC1> <Trailer data HARDROC1>
<Header data HARDROC2> <data HARDROC2> <Trailer data HARDROC2>
…
<Header data HARDROCn> <data HARDROCn> <Trailer data HARDROCn>
<Trailer global numérique>
<CRC>

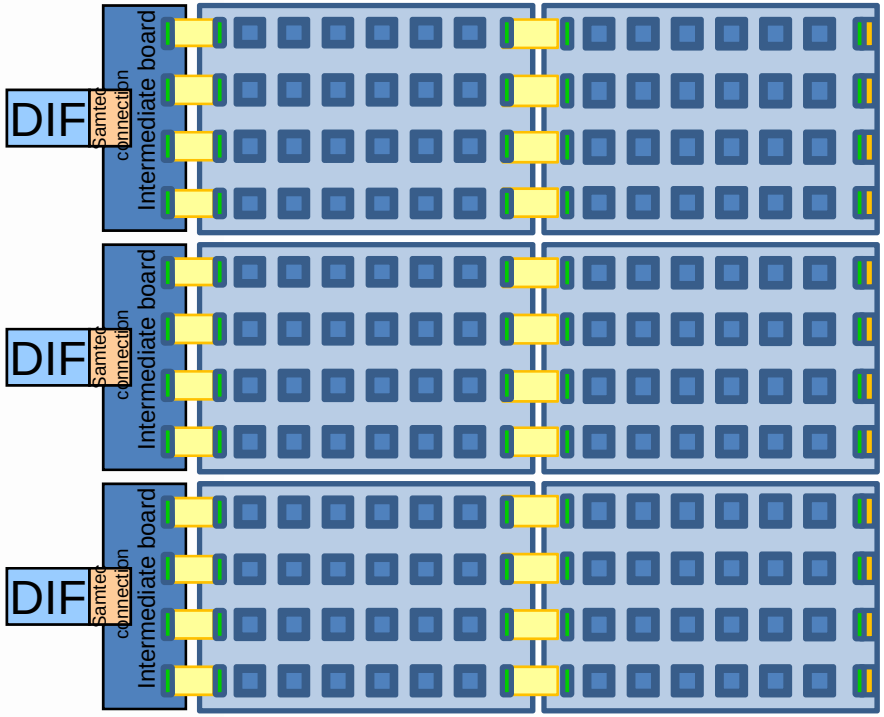
Ideas for 3rd format version, addition of :

- number of read frames
- number of read ASICs
- run number
- …

On going works

- **MicroMEGAS Square meter and DIF VHDL code with Hardroc 2**
  - Cap Sébastien, Dalmaz Alexandre, Drancourt Cyril, Prast Julie, Vouters Guillaume.
- **DIF VHDL code for DIRAC 2**
  - Gaglione Renaud, Prast Julie, Vouters Guillaume
- **DIF VHDL code for Calice DAQ**
  - Marc Kelly (Manchester), Prast Julie, Vouters Guillaume

MicroMEGAS Square meter



m² status:

- New DIFs are in production
- New Inter-DIF : design on going
- New ASUs with HARDROC 2 : design and routing finished

DIF status:

- The VHDL code has to be updated to HARDROC 2
  (Datasheet still not available)

: Flat Printed Circuit

: ASIC chip (64 channels)

: Hirose connector

: Terminaison board

DIRAC 2

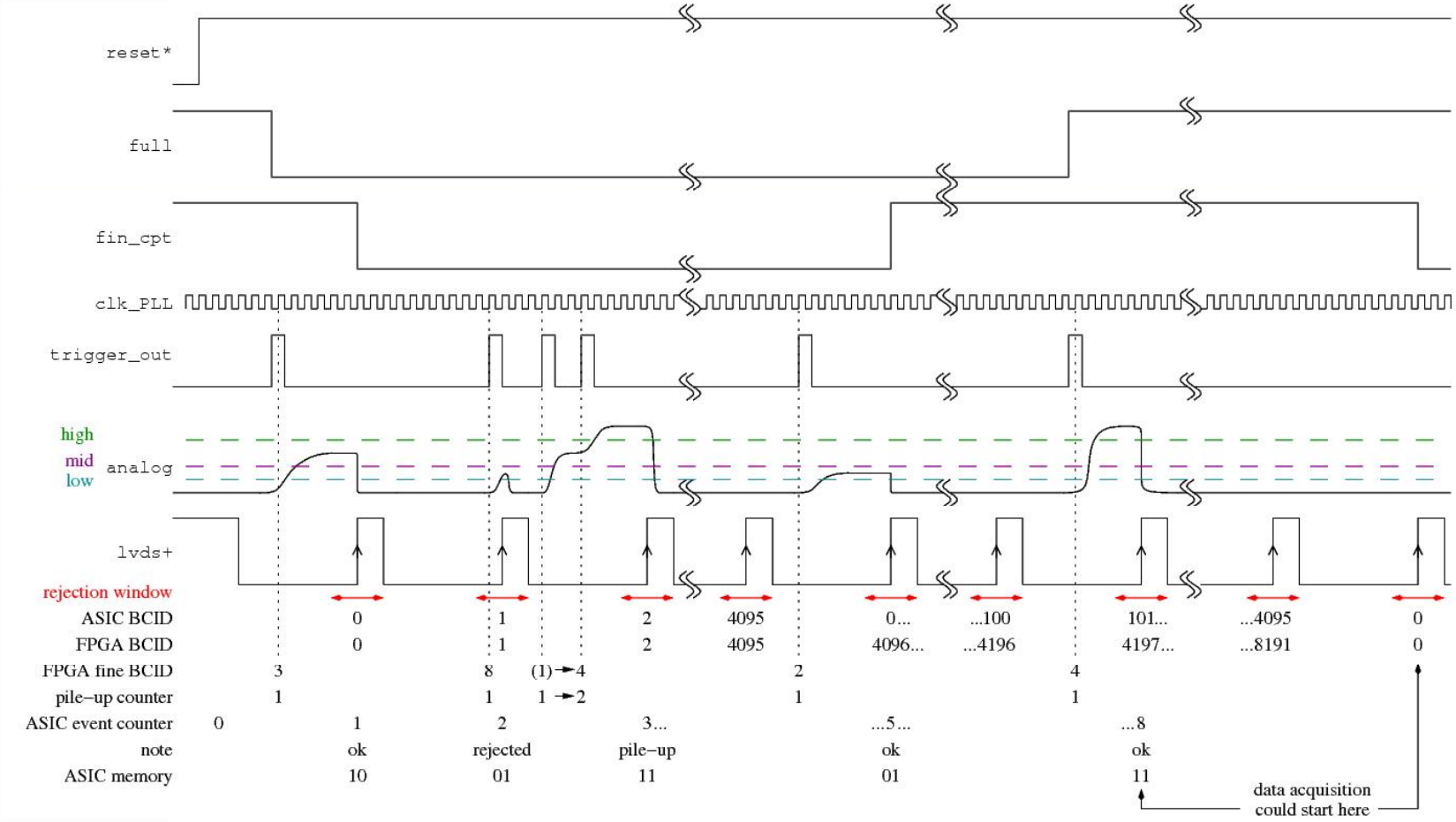
DIRAC 2 status

- DIRAC 2 ASICs and IPNL test board will arrive on the end of january.
- Tests will begin at the beginning of February
  - → test of Firmware and Software
  - → test of Dirac 2 features
  - → Characterization of ASICs
  - → …
- 24 Dirac 2 ASU for MicroMEGAS
- LAPP/IPNL DIRAC 3 collaboration
  - → i2c like configuration
  - → 0 suppression
  - → …

DIF Status

- The VHDL code is developed and we will test it soon.

DIRAC 2 / DIF features



CALICE DAQ

A protocol between the LDA and the DIF has been done by the DIF Task Force (Remi Cornat, Bart Hommel, Marc Kelly, Julie Prast, Mathias Reinecke)

- The Calice DAQ use the HDMI connector
- The document take into account AHCAL, ECAL and DHCAL project.

DIF Status

- The VHDL code development just started !

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Thank You

For Your Attention !

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