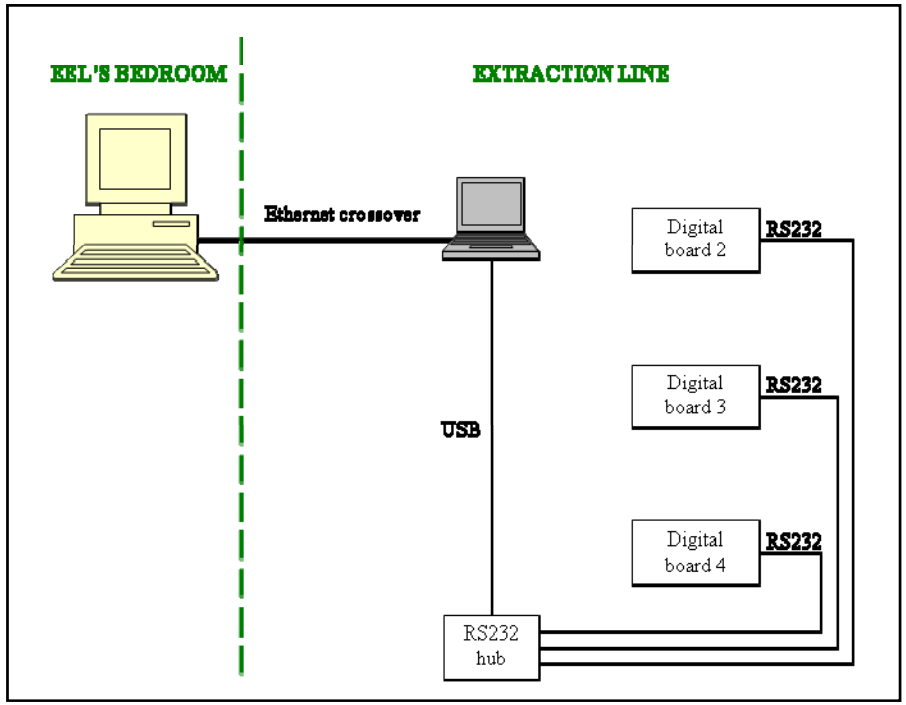
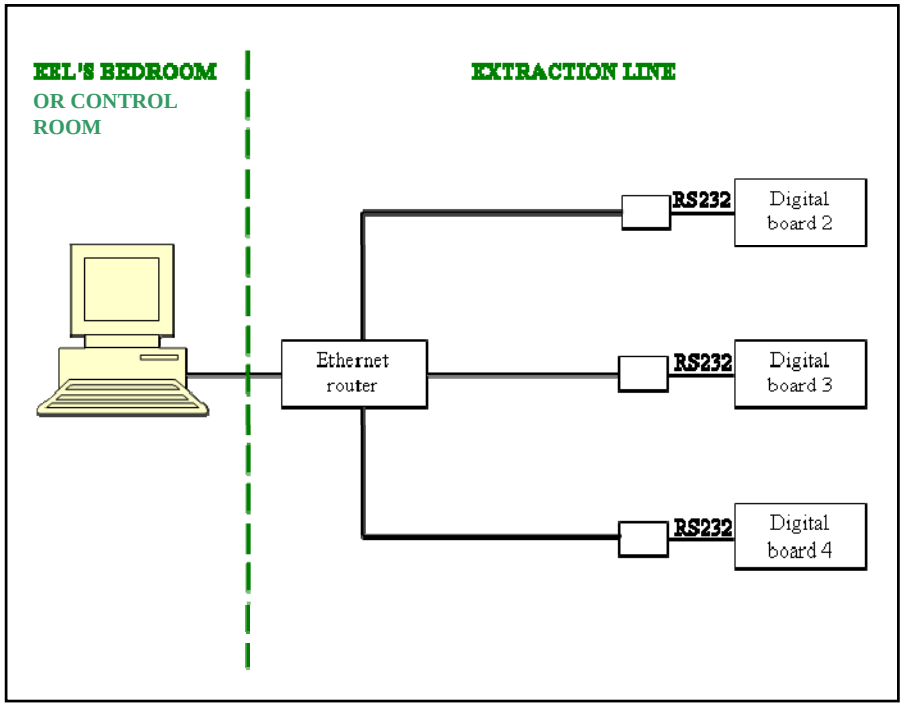
# Planned DAQ configuration for February

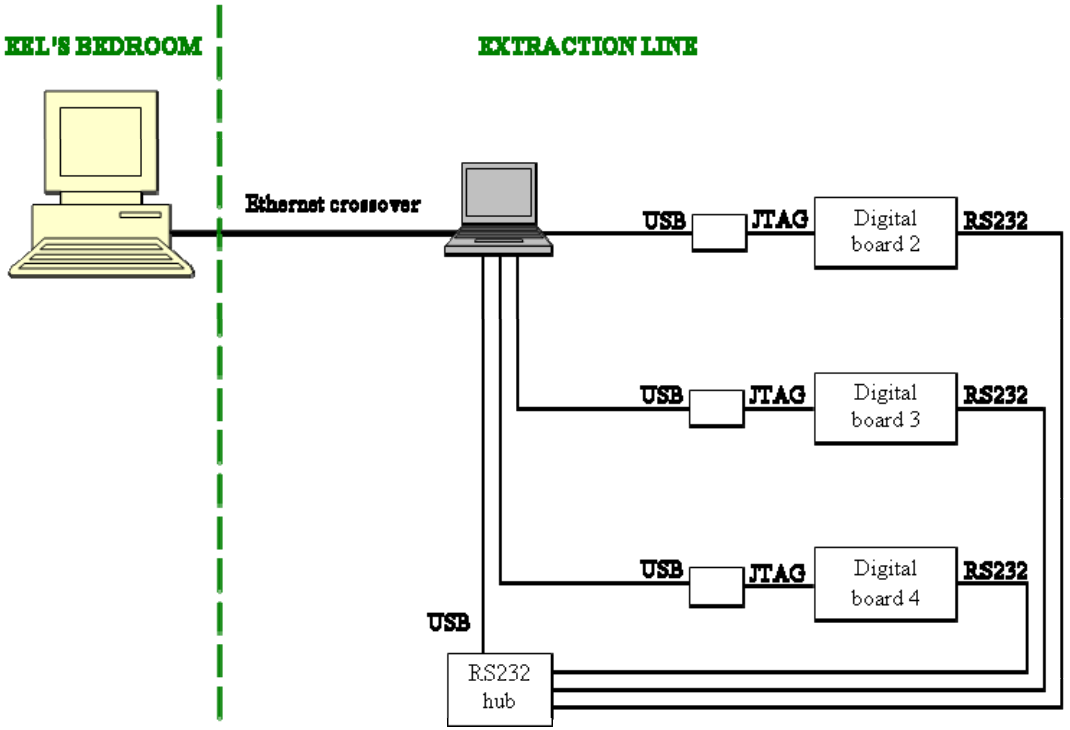
- Still plan to control FB boards over RS232
- Either use in-tunnel laptop
  - Simple solution.  No extra work required
- Or use RS232-to-ethernet converters & router
  - More elegant and similar to eventual solution.  Need 3x converters c. £100 each



# Contingency configuration

- Xilinx say we can also still use CS/JTAG control with 3 boards
  - Backup plan
  - Need a laptop with 4 USB ports (USB hub?)
  - Not yet tested in lab.  To be done shortly



# PC status

- The ATF PC is now working under Windows
- It even has a monitor!
- Intend to run DAQ software from PC in February
- Once we're using RS232-to-ethernet though:
  - Should be able to access FB board via ATF local network
  - Run DAQ from e.g. control room
  - Role of PC then less clear.  Some sort of server role perhaps?

# Firmware status

- Produced ‘DAQ’ FONT4 firmware with RS232 control
  - Place and route has passed timing with 72ps slack
  - Most modules have been tested, but full firmware hasn’t yet been
  - DAO software is needed for tests.  Currently writing this
- 357MHz domain control registers for selecting:
  - Trigger type (NIM/TTL)
  - Ring clock type (NIM/TTL)
  - Bunch spacing
  - Ring clock cycle wrt trigger
  - 357MHz cycle wrt ring clock
  - ADC clock phases
- 40MHz domain control registers for storing clock input delays

# Firmware status cont.

- Special instructions for:
  - Full reset (Includes DCM and takes ~200ms)
  - IDELAY reset (Resets only IDELAY and IDELAYCTRL elements taking 100ns)
  - Increment IDELAY to control register value
- Chipscope readout retained for bench tests

# RS232 control protocol

| Binary | Decimal | Purpose |
|---|---|---|
| 000x xxxx | 0 - 31 | Specify special instructions. Currently:<br>0 - Full reset (includes DCM and takes ~200ms)<br>1 - IDELAY reset (idelay and idelayctrl elements only. Takes ~100ns)<br>2 - Increment IDELAY1 to specified value<br>3 - Increment IDELAY2 to specified value<br>17 - Reserved for XON character<br>19 - Reserved for XOFF character |
| 001x xxxx | 32 - 63 | Used to address one of up to 32 RAM LUTs. Subsequent data are written to specified LUT. Not used for DAQ |
| 010x xxxx | 64 - 95 | Used to address one of up to 32 7-bit control registers on the **357MHz** domain. Registers may be concatenated to store larger parameters. Subsequent data are written to the specified register |
| 011x xxxx | 96 - 127 | Used to address one of up to 32 7-bit control registers on the **40MHz** domain. Registers may be concatenated to store larger parameters. Subsequent data are written to the specified register |
| 1xxx xxxx | 128 - 255 | 7-bits of data |

# Software and bench test plans

- Currently writing DAQ software
- Multithread old code to read and write RS232 simultaneously
- Control software required for firmware bench tests
- Expect test version next week with partial GUI
- Tests of firmware and of contingency config. will be done then
- Once firmware successfully tested, GUI will be completed

- Note: if ethernet is used then modifying DAQ should be simple

# Hardware required list

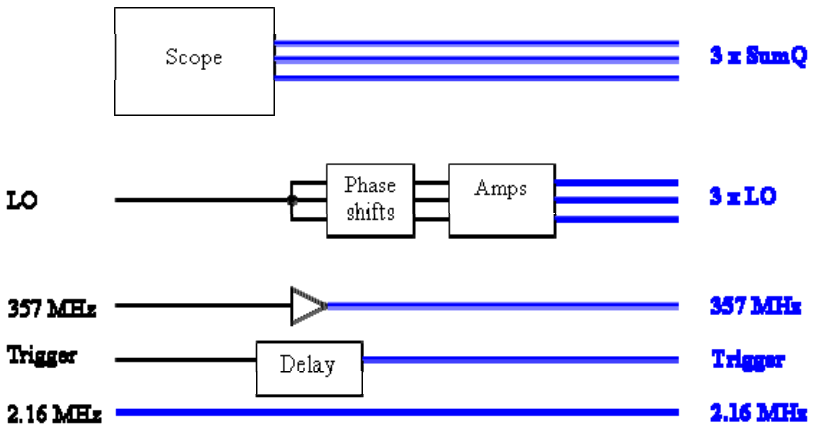
- 2x USB to RS232 hubs
- 3x RS232 cables (crossed ones)
- 3x RS232 to ethernet converters
- Ethernet router?
- We already have 3xUSB JTAG programmers (?)

- Should lay single ethernet with heliax to avoid reliance on ATF networking

- I guess we have 3 pairs of short matched cables for BPMs?

# Additional: heliax layout

**EEL'S BEDROOM**

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