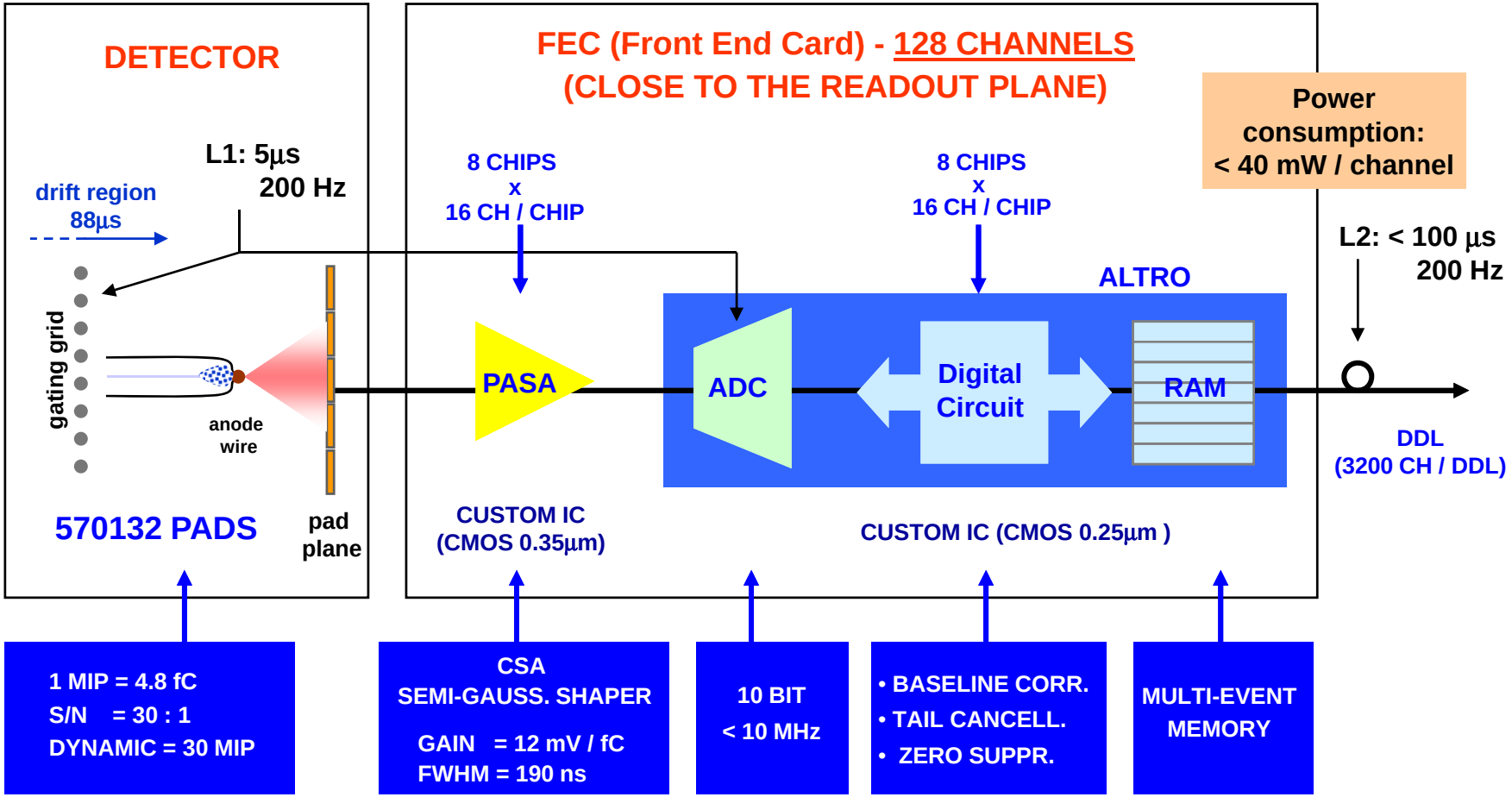
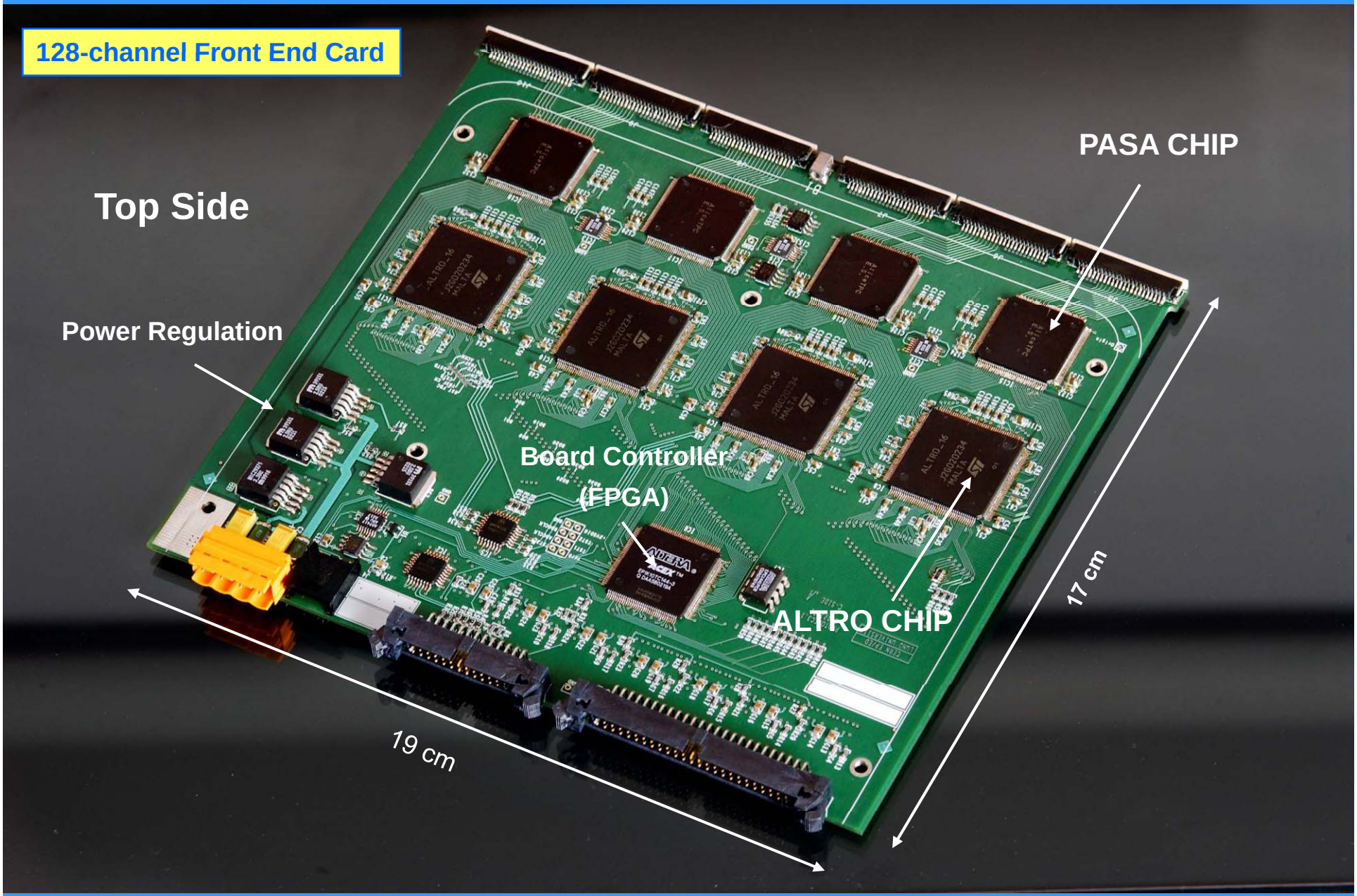
Charge Readout Chip Development
&
System Level Considerations

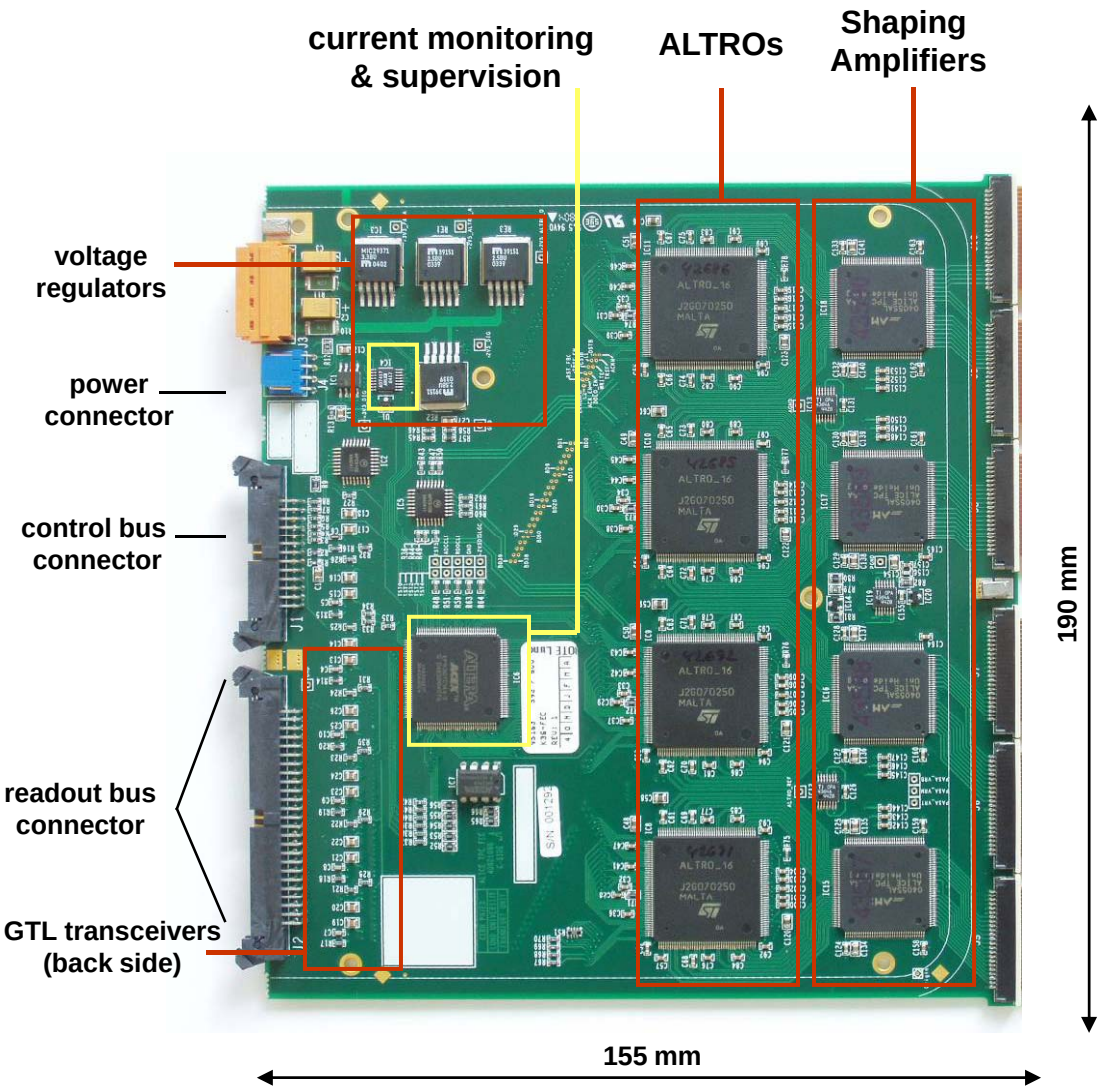
Front End Electronics Architecture

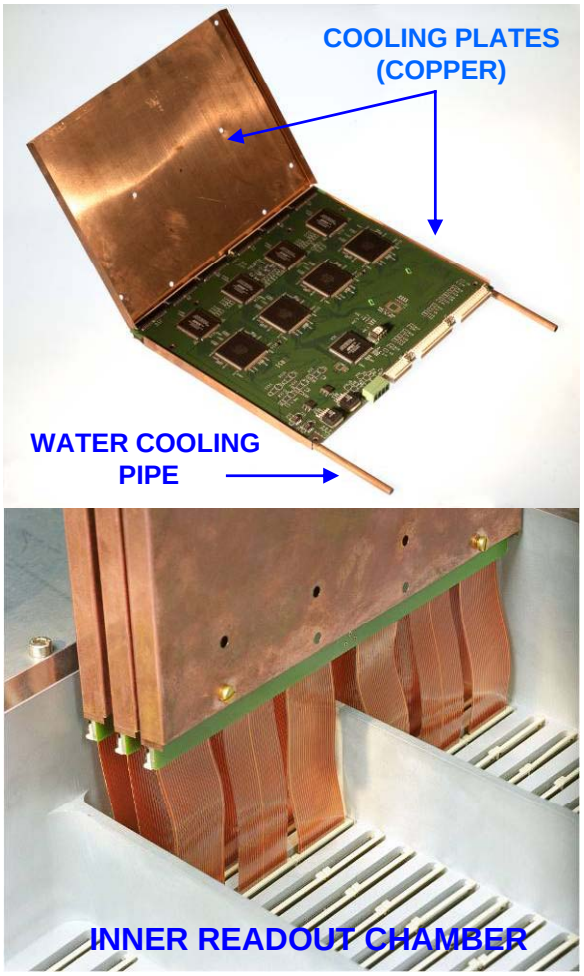


Alice TPC FEE – MWPC Readout



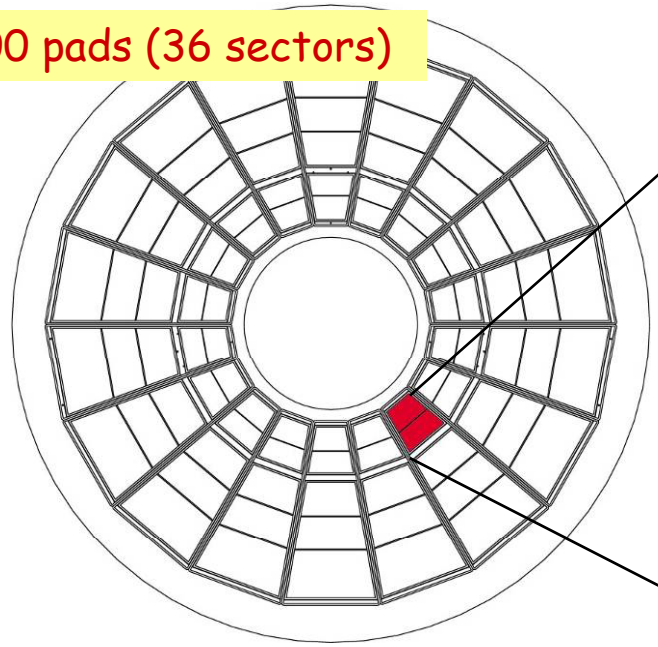
ALICE TPC Front End Card: Layout, Cooling and Mounting





ALICE TPC - Readout Chambers

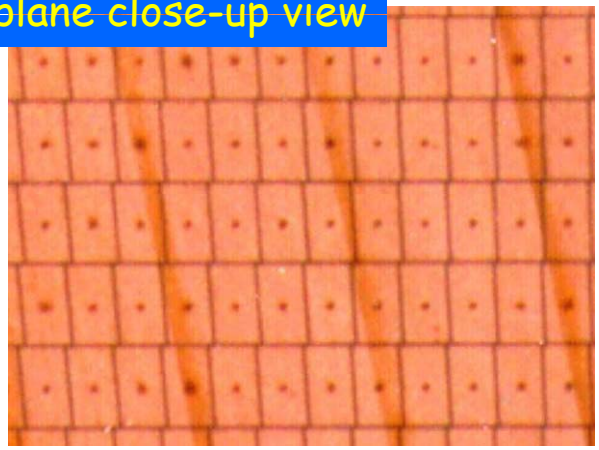
≈ 570 000 pads (36 sectors)

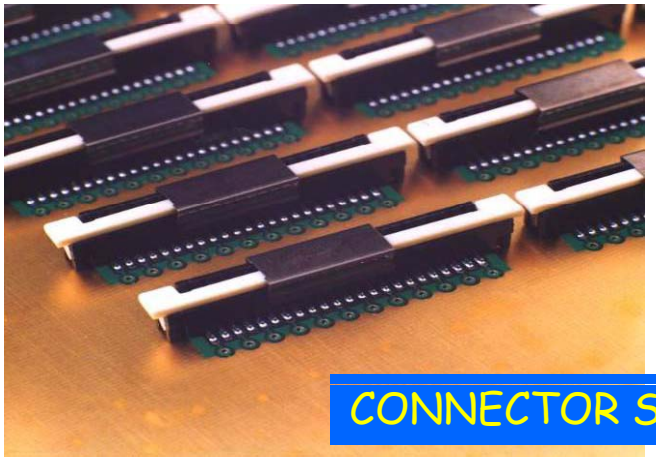


PAD SIDE

5504 pad (4x7.5 mm²)

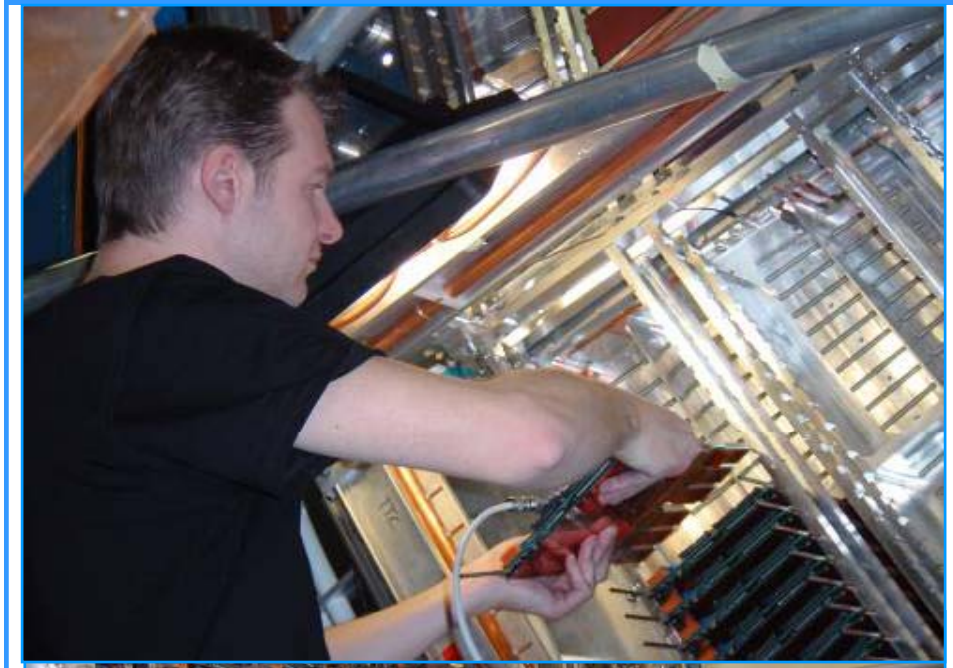
Pad plane close-up view

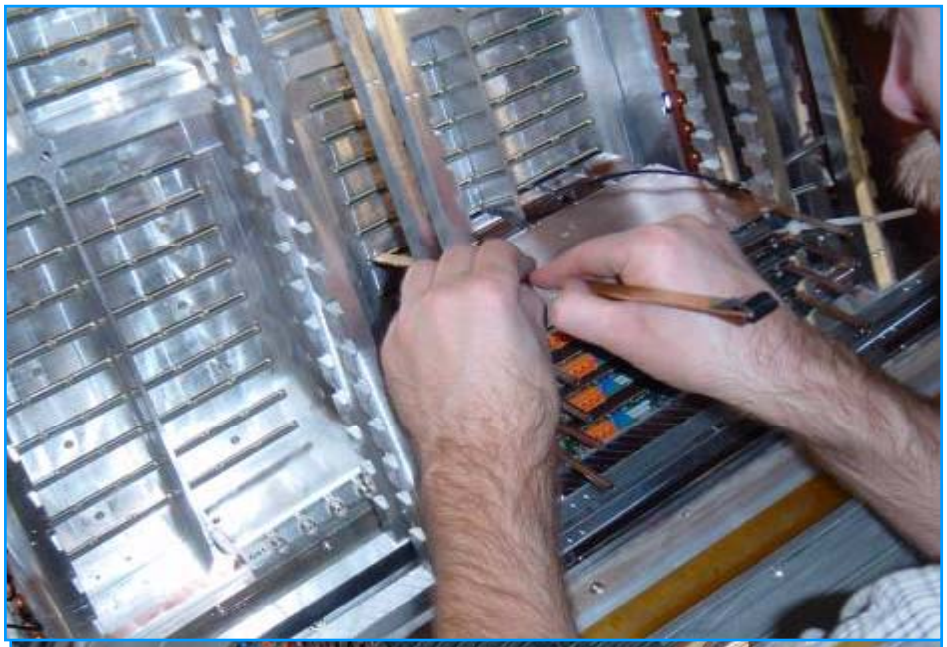




CONNECTOR SIDE

Installation of ALICE Front End Electronics (Feb-May '06)





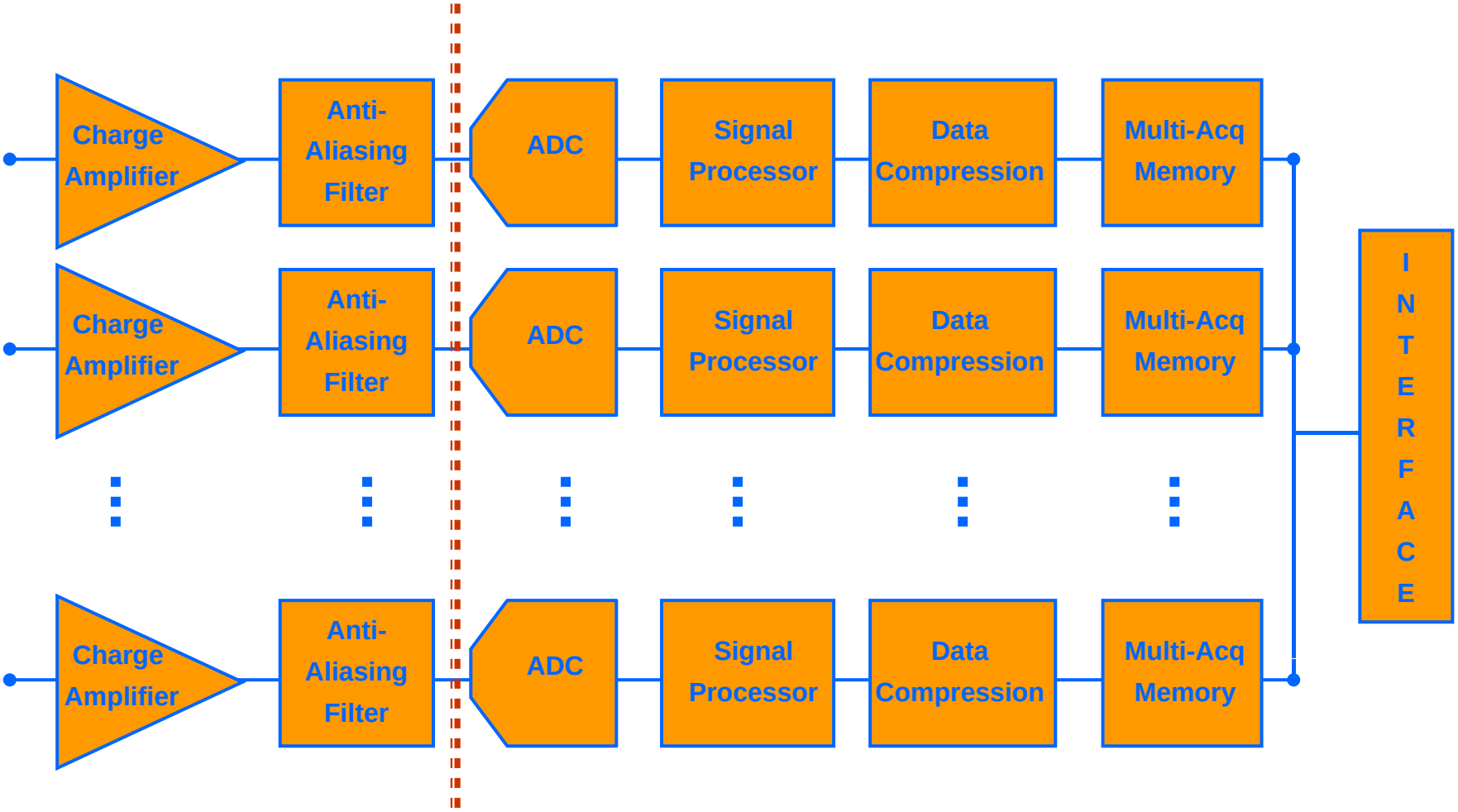

ALICE TPC in June '06

A general purpose charge readout chip for MPGDs

- ✓ number of channels: 32 or 64
- ✓ programmable charge amplifier
  - sensitive to a charge in the range: ~10^2 - ~10^6 electrons
  - Peaking time: 30ns – 120ns
- ✓ high-speed high-resolution A/D converter
  - sampling rate: 40MHz
- ✓ programmable digital filter for noise reduction and signal interpolation;
- ✓ a signal processor for the extraction and compression of the signal information (charge and time of occurrence).
- ✓ Two readout modes: external trigger or self-triggered
- ✓ Trigger can have any position wrt the acquisition window
- ✓ Standby mode

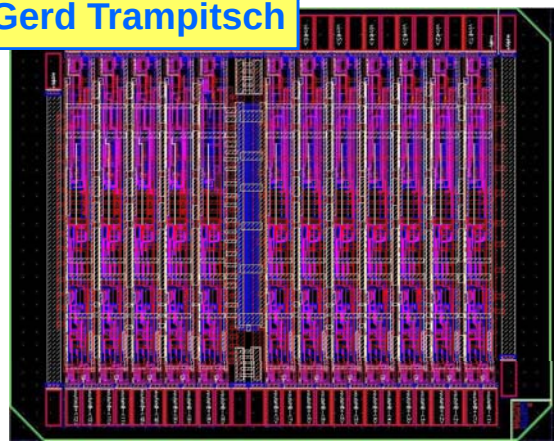
Charge Readout Chip Block Diagram

32 / 64 Channel



Charge Readout Chip – Amplifier and ADC

Gerd Trampitsch

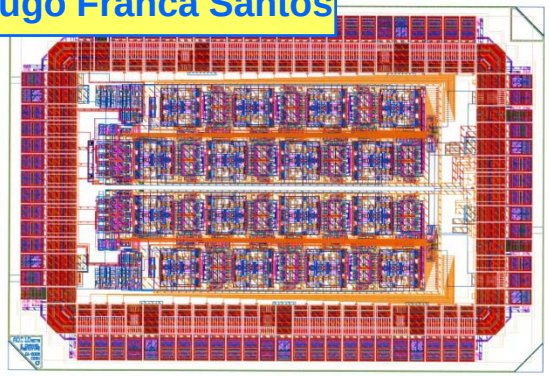


Layout of 12-channel PASA prototype

16-channel Shaping amplifier prototype

- 16-channel 4th order CSA
- programmable polarity
- programmable gain: 12-27 mV/fC
- Programmable peaking time: 30-120ns
- Process: IBM CMOS 0.13 µm
- area: 3 mm^2
- 1.5 V single supply, power: <8mW/channel
- **MPR samples (1000): May 07**

Hugo Franca Santos



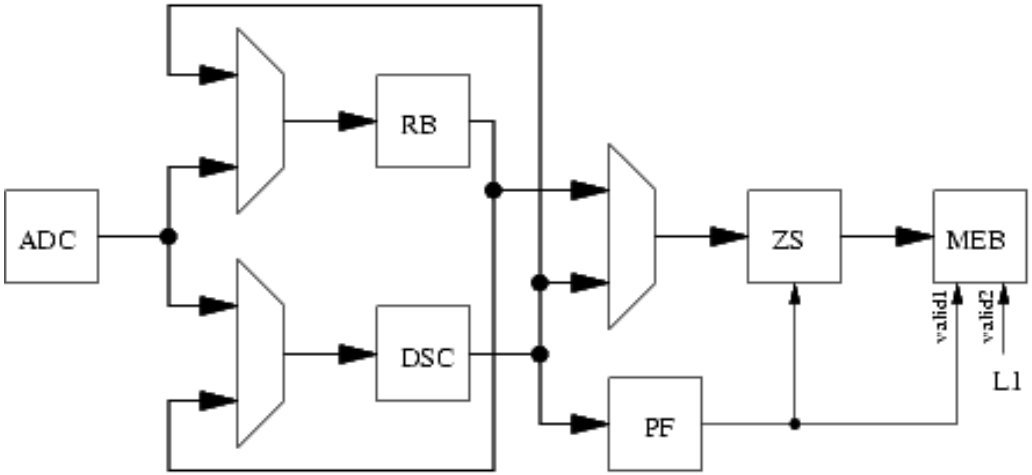
Layout of 2-channel ADC prototype

2-channel ADC prototype

- 10-bit ADC, 40MHz sampling frequency
- Pipelined differential architecture
- Process: IBM CMOS 0.13 µm
- area: 0.7 mm^2
- 1.5 V single supply
- Power/channel: 33mW @ 40MHz, 18mW @ 20MHz
- **MPR samples (40): Jan 09**

Charge Readout Chip – Digital Data Processor

Global Architecture

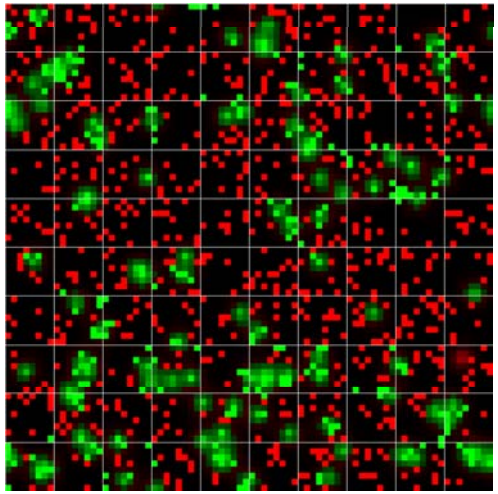


RB: ring buffer, DSC: digital signal conditioner, PF: pulse finder
ZS: zero suppression, MEB: multi event buffer

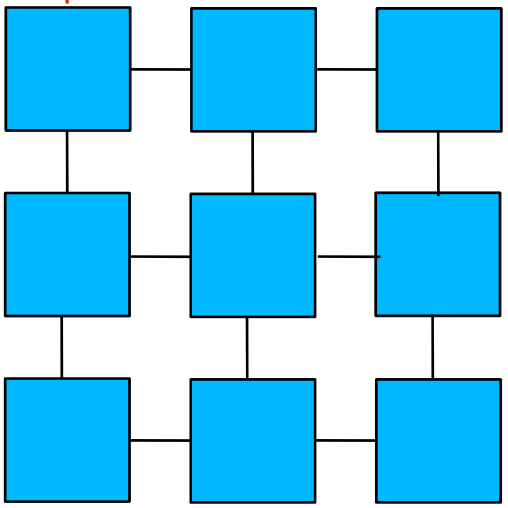
Main Features

- Programmable architecture
  - trigger related acquisition
  - trigger-less acquisition
  - free pos. of acq. window
- Flexible use of memory
- Full digital signal conditioning
- 3D zero suppression
- Integrated readout network

(3D) pulse/peak finder



Chip interconnection scheme



Considerations on readout plane

IC Area (die size)

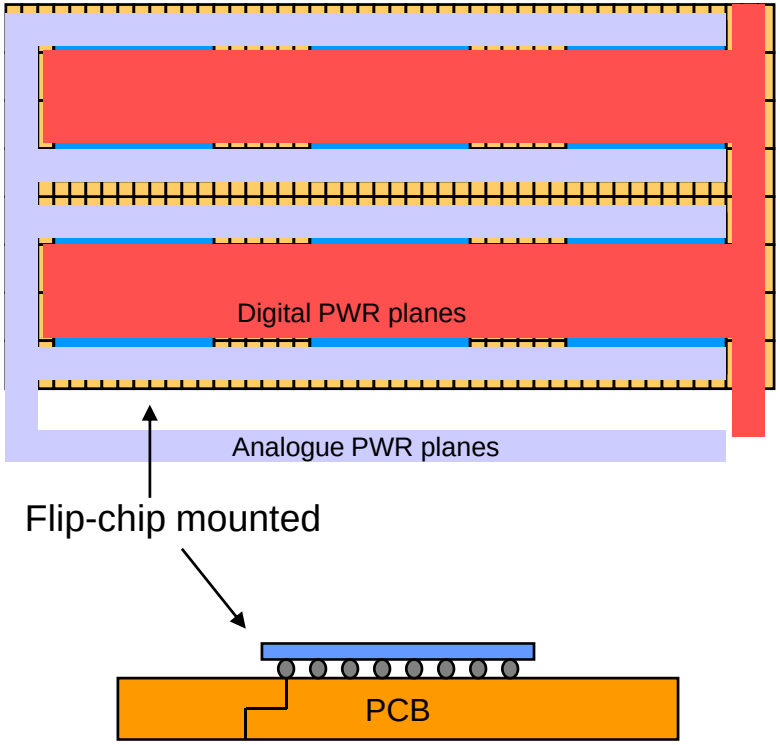
- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.7 mm^2 (prototype ➡room for improvement)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

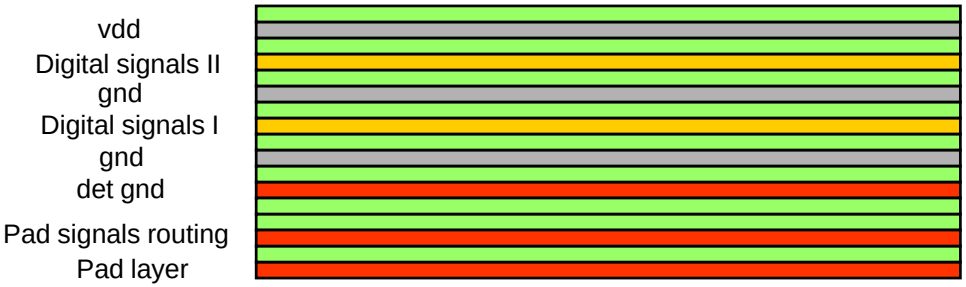
PCB dimensions < 40 x 40 cm^2 ⇨ 20000 pads (8mm^2/pad), ~300 FE chips / board

Considerations on readout plane

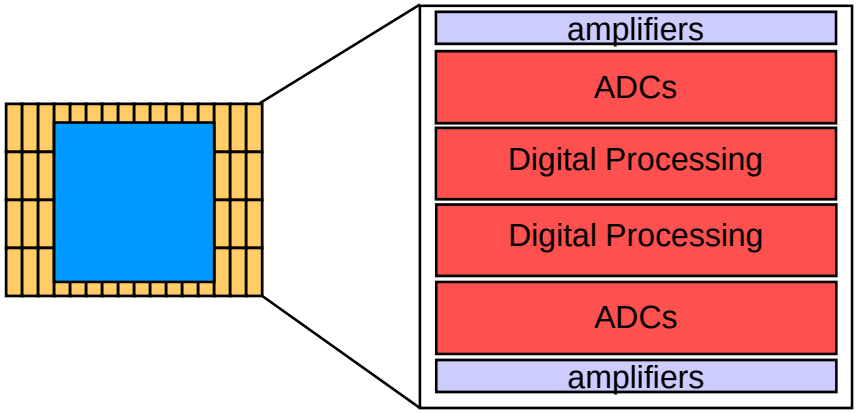
PCB topology and layer stack-up



8-layer PCB



Chip floorplan



Considerations on power consumption & cooling

Power consumption (for 30ns peaking time, 40Mhz sampling, 3mm^2 pad)

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- average power / m^2 167 W