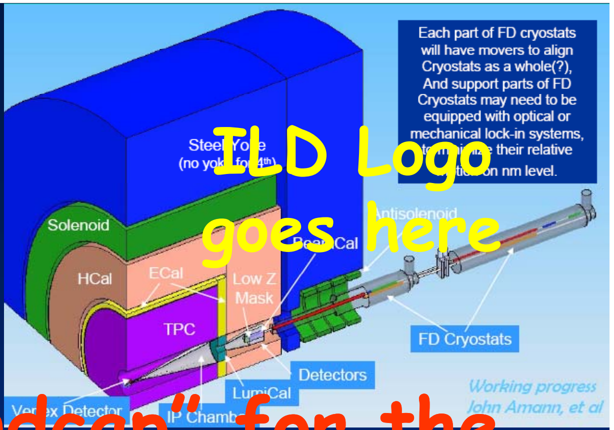
Worldwide Study of
the Physics and Detectors
for Future Linear
e+ e- Colliders



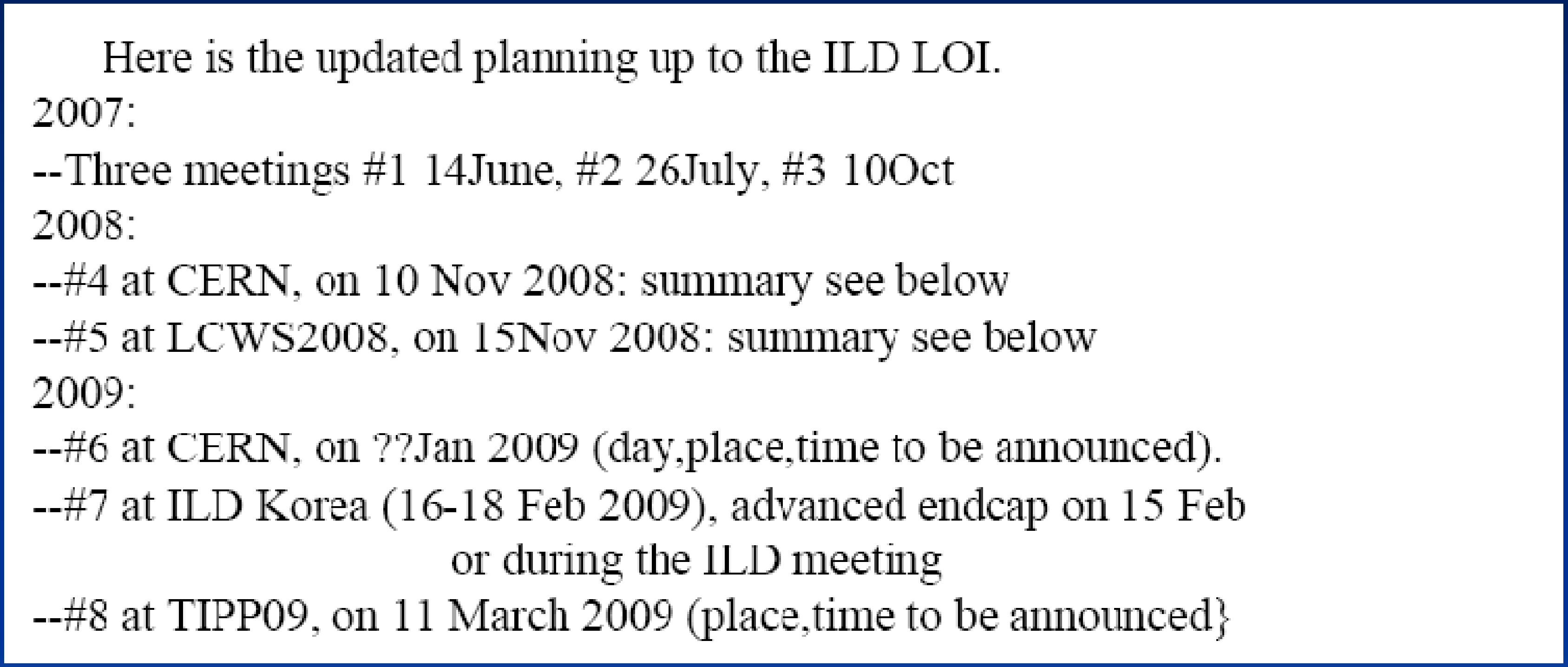
Iteration on LCTPC "advanced-endcap" for the ILD LOI…

19.01.2009

Ron Settles MPI-Munich

LCTPC engineering model for LOI

- "Advanced endcap" meetings now continuing.
- Next steps (updated):



Here is the updated planning up to the ILD LOI.

2007:

--Three meetings #1 14June, #2 26July, #3 10Oct

2008:

--#4 at CERN, on 10 Nov 2008: summary see below

--#5 at LCWS2008, on 15Nov 2008: summary see below

2009:

--#6 at CERN, on ??Jan 2009 (day,place,time to be announced).

--#7 at ILD Korea (16-18 Feb 2009), advanced endcap on 15 Feb
or during the ILD meeting

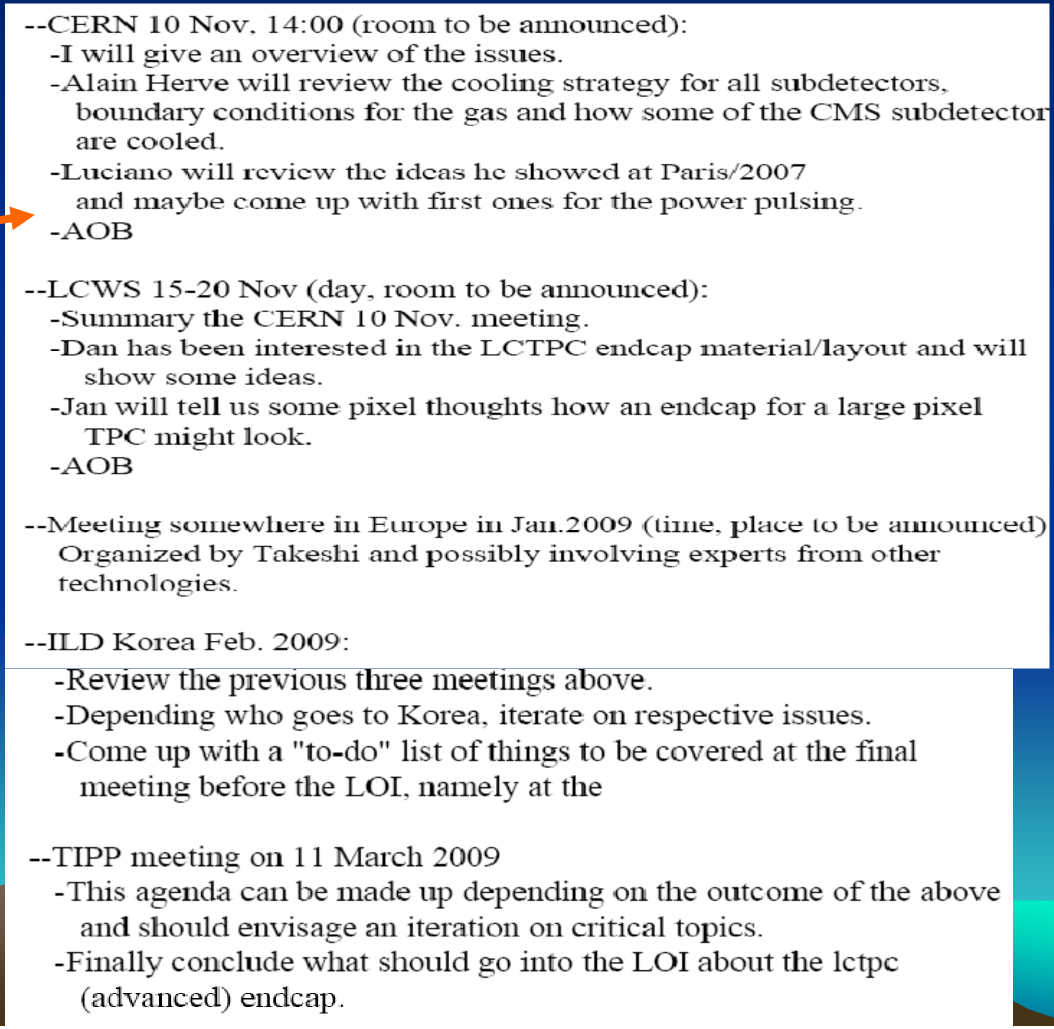
--#8 at TIPP09, on 11 March 2009 (place,time to be announced}

LCTPC engineering model for LOI

- "Advanced endplate" meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate. There were three meetings in 2007.
- The proposal for next steps (email 31.10.2008):

Reverse order today {

DAQ issues added



--CERN 10 Nov, 14:00 (room to be announced):
  -I will give an overview of the issues.
  -Alain Herve will review the cooling strategy for all subdetectors, boundary conditions for the gas and how some of the CMS subdetector are cooled.
  -Luciano will review the ideas he showed at Paris/2007 and maybe come up with first ones for the power pulsing.
  -AOB

--LCWS 15-20 Nov (day, room to be announced):
  -Summary the CERN 10 Nov. meeting.
  -Dan has been interested in the LCTPC endcap material/layout and will show some ideas.
  -Jan will tell us some pixel thoughts how an endcap for a large pixel TPC might look.
  -AOB

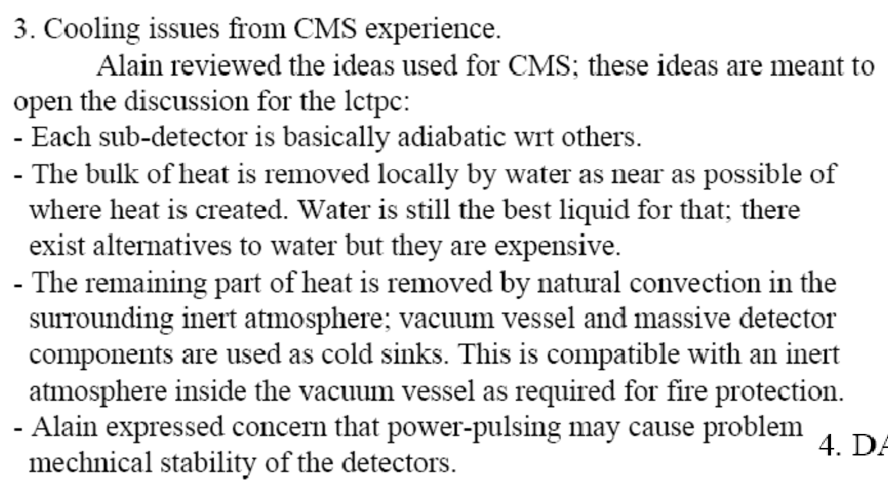
--Meeting somewhere in Europe in Jan.2009 (time, place to be announced) Organized by Takeshi and possibly involving experts from other technologies.

--ILD Korea Feb. 2009:
  -Review the previous three meetings above.
  -Depending who goes to Korea, iterate on respective issues.
  -Come up with a "to-do" list of things to be covered at the final meeting before the LOI, namely at the

--TIPP meeting on 11 March 2009
  -This agenda can be made up depending on the outcome of the above and should envisage an iteration on critical topics.
  -Finally conclude what should go into the LOI about the lctpc (advanced) endcap.

LCTPC engineering model for LOI

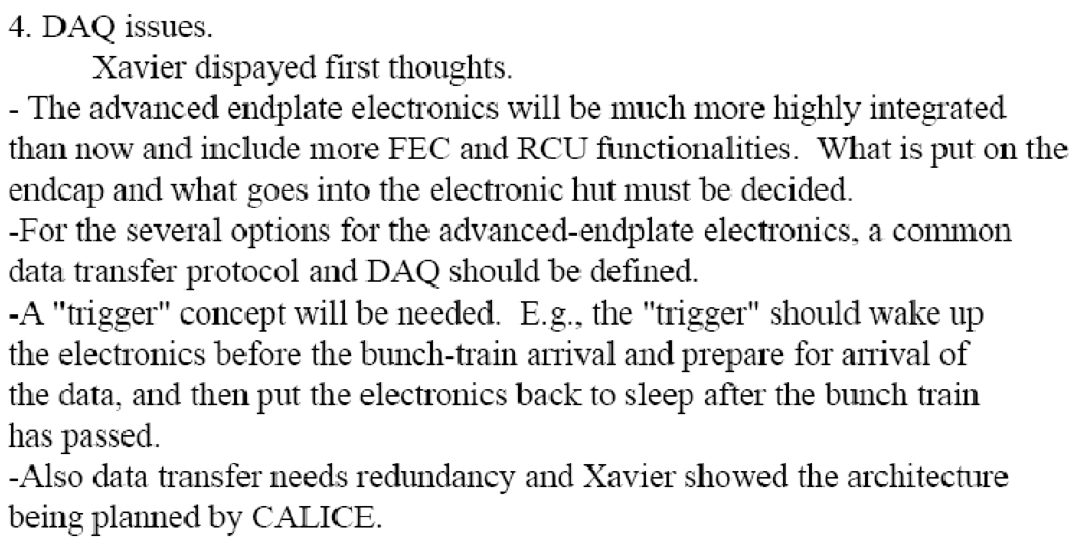
- “Advanced endcap” meeting#4, reminder about cooling and electronics (will come back to electronics in a moment):



3. Cooling issues from CMS experience.

Alain reviewed the ideas used for CMS; these ideas are meant to open the discussion for the lctpc:

- Each sub-detector is basically adiabatic wrt others.
- The bulk of heat is removed locally by water as near as possible of where heat is created. Water is still the best liquid for that; there exist alternatives to water but they are expensive.
- The remaining part of heat is removed by natural convection in the surrounding inert atmosphere; vacuum vessel and massive detector components are used as cold sinks. This is compatible with an inert atmosphere inside the vacuum vessel as required for fire protection.
- Alain expressed concern that power-pulsing may cause problem mechnical stability of the detectors.



4. DAQ issues.

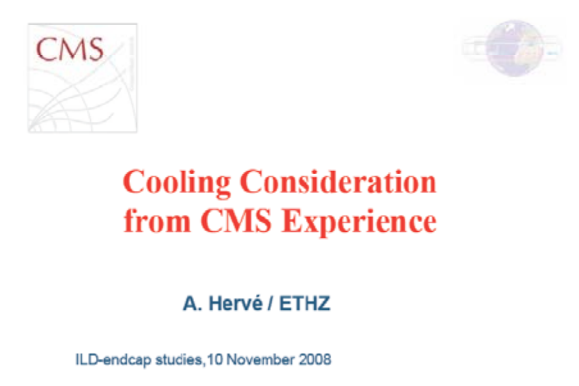
Xavier dispayed first thoughts.

- The advanced endplate electronics will be much more highly integrated than now and include more FEC and RCU functionalities. What is put on the endcap and what goes into the electronic hut must be decided.

-For the several options for the advanced-endplate electronics, a common data transfer protocol and DAQ should be defined.

-A "trigger" concept will be needed. E.g., the "trigger" should wake up the electronics before the bunch-train arrival and prepare for arrival of the data, and then put the electronics back to sleep after the bunch train has passed.

-Also data transfer needs redundancy and Xavier showed the architecture being planned by CALICE.

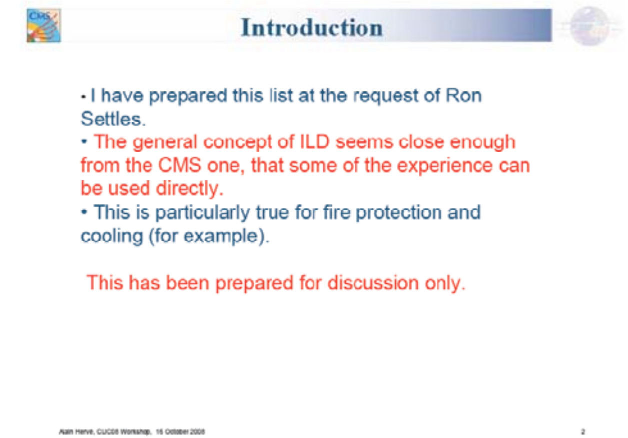


CMS

Cooling Consideration from CMS Experience

A. Hervé / ETHZ

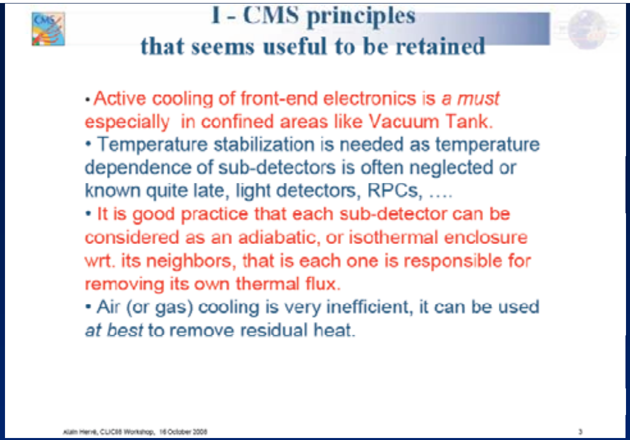
ILD-endcap studies,10 November 2008



Introduction

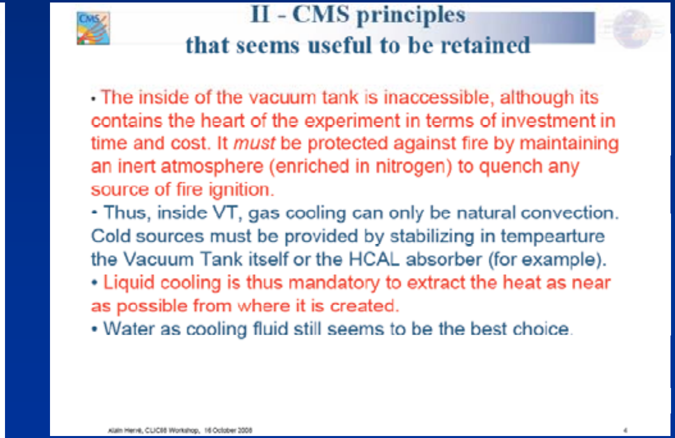
- I have prepared this list at the request of Ron Settles.
- The general concept of ILD seems close enough from the CMS one, that some of the experience can be used directly.
- This is particularly true for fire protection and cooling (for example).

This has been prepared for discussion only.



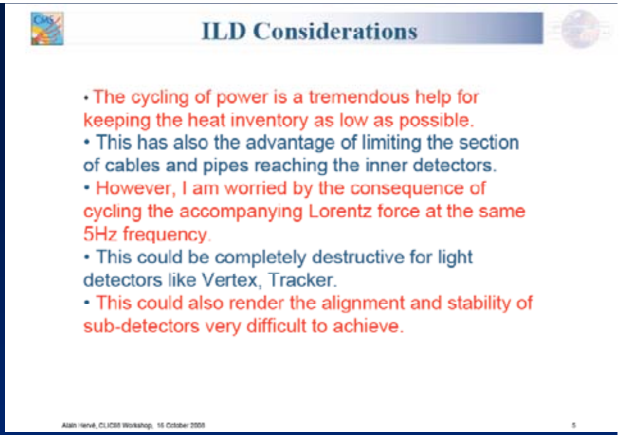
I - CMS principles that seems useful to be retained

- Active cooling of front-end electronics is *a must* especially in confined areas like Vacuum Tank.
- Temperature stabilization is needed as temperature dependence of sub-detectors is often neglected or known quite late, light detectors, RPCs, ….
- It is good practice that each sub-detector can be considered as an adiabatic, or isothermal enclosure wrt. its neighbors, that is each one is responsible for removing its own thermal flux.
- Air (or gas) cooling is very inefficient, it can be used *at best* to remove residual heat.



II - CMS principles that seems useful to be retained

- The inside of the vacuum tank is inaccessible, although its contains the heart of the experiment in terms of investment in time and cost. It *must* be protected against fire by maintaining an inert atmosphere (enriched in nitrogen) to quench any source of fire ignition.
- Thus, inside VT, gas cooling can only be natural convection. Cold sources must be provided by stabilizing in tempearture the Vacuum Tank itself or the HCAL absorber (for example).
- Liquid cooling is thus mandatory to extract the heat as near as possible from where it is created.
- Water as cooling fluid still seems to be the best choice.



ILD Considerations

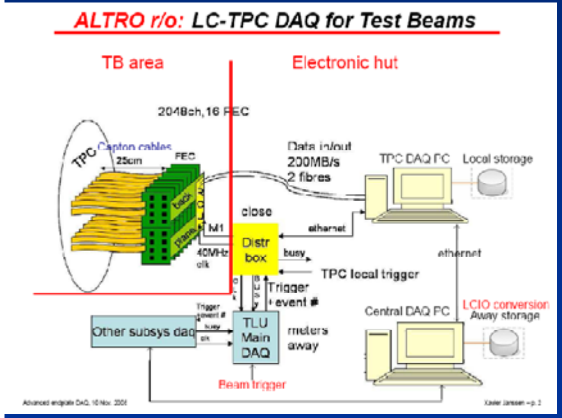
- The cycling of power is a tremendous help for keeping the heat inventory as low as possible.
- This has also the advantage of limiting the section of cables and pipes reaching the inner detectors.
- However, I am worried by the consequence of cycling the accompanying Lorentz force at the same 5Hz frequency.
- This could be completely destructive for light detectors like Vertex, Tracker.
- This could also render the alignment and stability of sub-detectors very difficult to achieve.

Xavier Janssen - Université Libre de Bruxelles

LP-TPC DAQ for Advanced Endplate

LCTPC Advanced Endplate Meeting, CERN, 10th Nov. 2008

Advanced endplate DAQ, 10 Nov. 2008 Xavier Janssen – p. 1



ALTRO r/o: LC-TPC DAQ for Test Beams

TB area

Electronic hut

2048ch,16 FEC

TPC

Capton cables

25cm

FEC

back

plane

ALTRO

M1

40MHz clk

close

Distr box

Data in/out 200MB/s 2 fibres

TPC DAQ PC

Local storage

ethernet

busy

TPC local trigger

ethernet

clk

busy

Trigger + event #

Trigger event #

busy

clk

Other subsys daq

TLU Main DAQ

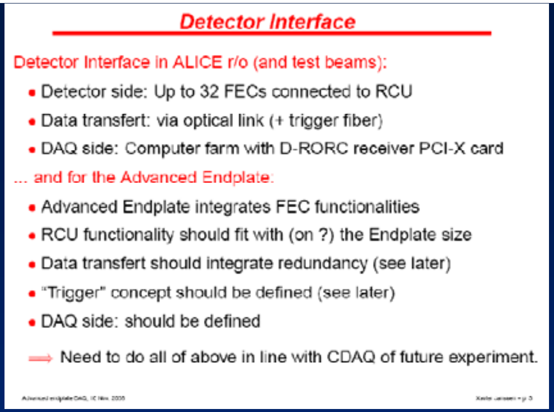
meters away

Central DAQ PC

LCIO conversion Away storage

Beam trigger

Advanced endplate DAQ, 10 Nov. 2008 Xavier Janssen – p. 2



Detector Interface

Detector Interface in ALICE r/o (and test beams):

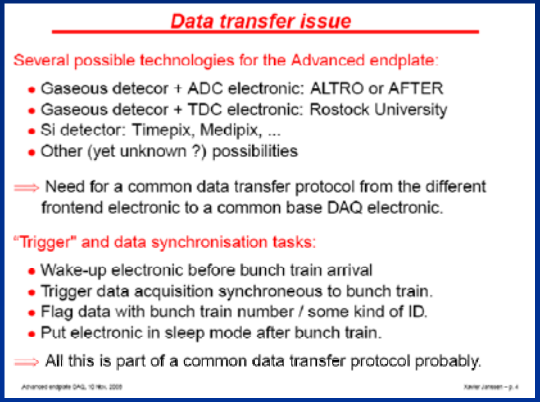
- Detector side: Up to 32 FECs connected to RCU
- Data transfert: via optical link (+ trigger fiber)
- DAQ side: Computer farm with D-RORC receiver PCI-X card

... and for the Advanced Endplate:

- Advanced Endplate integrates FEC functionalities
- RCU functionality should fit with (on ?) the Endplate size
- Data transfert should integrate redundancy (see later)
- "Trigger" concept should be defined (see later)
- DAQ side: should be defined

⟹ Need to do all of above in line with CDAQ of future experiment.

Advanced endplate DAQ, 10 Nov. 2008 Xavier Janssen – p. 3



Data transfert issue

Several possible technologies for the Advanced endplate:

- Gaseous detecor + ADC electronic: ALTRO or AFTER
- Gaseous detecor + TDC electronic: Rostock University
- Si detector: Timepix, Medipix, ...
- Other (yet unknown ?) possibilities

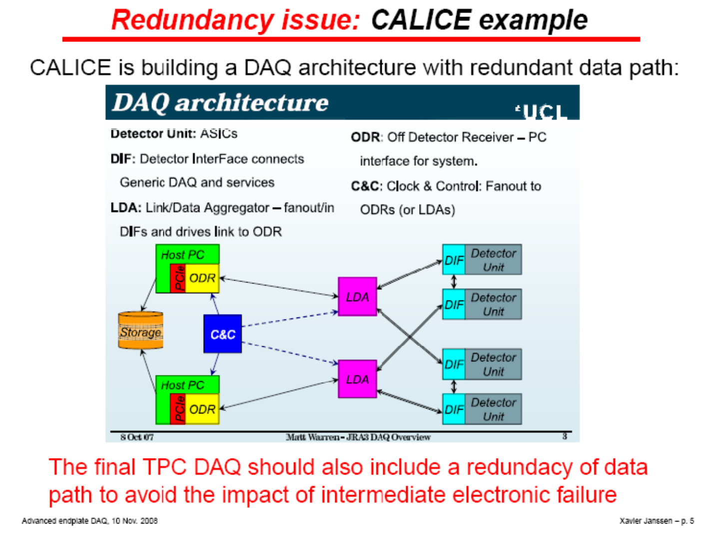
⟹ Need for a common data transfer protocol from the different frontend electronic to a common base DAQ electronic.

"Trigger" and data synchronisation tasks:

- Wake-up electronic before bunch train arrival
- Trigger data acquisition synchroneous to bunch train.
- Flag data with bunch train number / some kind of ID.
- Put electronic in sleep mode after bunch train.

⟹ All this is part of a common data transfer protocol probably.

Advanced endplate DAQ, 10 Nov. 2008 Xavier Janssen – p. 4



Redundancy issue: CALICE example

CALICE is building a DAQ architecture with redundant data path:

DAQ architecture

UCL

Detector Unit: ASICs

DIF: Detector InterFace connects Generic DAQ and services

LDA: Link/Data Aggregator – fanout/in DIFs and drives link to ODR

ODR: Off Detector Receiver – PC interface for system.

C&C: Clock & Control: Fanout to ODRs (or LDAs)

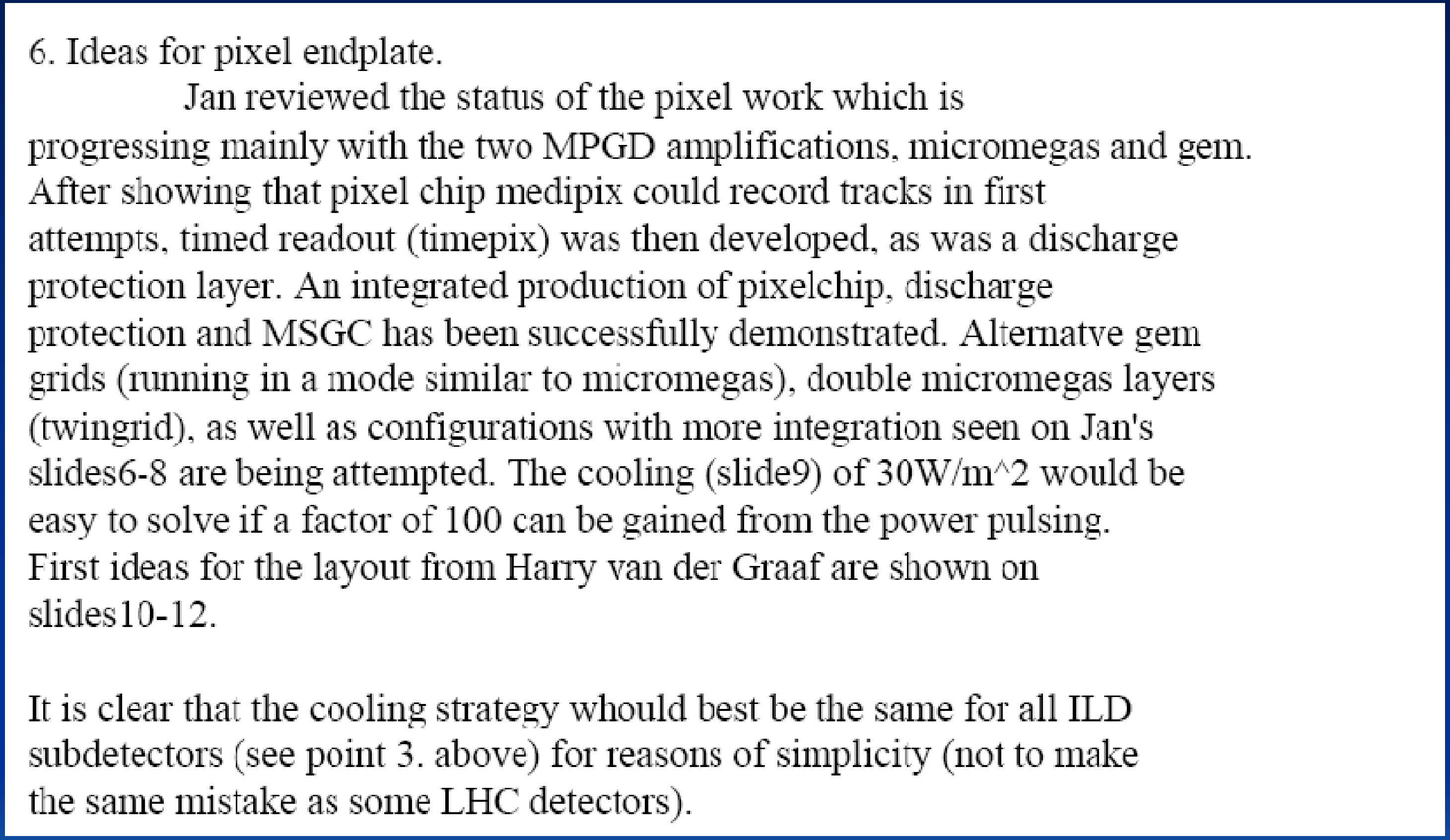
8 Oct 07 Matt Warren - JRA3 DAQ Overview 3

The final TPC DAQ should also include a redundacy of data path to avoid the impact of intermediate electronic failure

Advanced endplate DAQ, 10 Nov. 2008 Xavier Janssen – p. 5

LCTPC engineering model for LOI

- "Advanced endcap" meeting#5:



6. Ideas for pixel endplate.

Jan reviewed the status of the pixel work which is progressing mainly with the two MPGD amplifications, micromegas and gem. After showing that pixel chip medipix could record tracks in first attempts, timed readout (timepix) was then developed, as was a discharge protection layer. An integrated production of pixelchip, discharge protection and MSGC has been successfully demonstrated. Alternatve gem grids (running in a mode similar to micromegas), double micromegas layers (twingrid), as well as configurations with more integration seen on Jan's slides6-8 are being attempted. The cooling (slide9) of 30W/m^2 would be easy to solve if a factor of 100 can be gained from the power pulsing. First ideas for the layout from Harry van der Graaf are shown on slides10-12.

It is clear that the cooling strategy whould best be the same for all ILD subdetectors (see point 3. above) for reasons of simplicity (not to make the same mistake as some LHC detectors).

LCTPC engineering model for LOI

- "Advanced endcap" meeting#5, Jan example:

A Silicon TPC System

LPTPC endplate discussion
Chicago, 15 November 2008

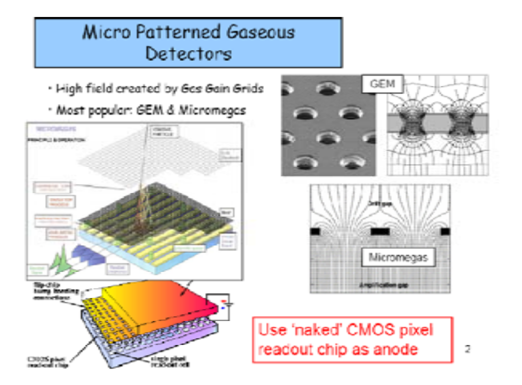
Jan Timmermans
NIKHEF

Multichip boards

- Bonn: two 4-chip boards for LCTPC
- Saclay: 8-chip board for LCTPC
- NIKHEF: 4-chip board (working in readout)

All had problems with power(regulation); being solved

- NIKHEF also aiming for 8x8-chip system in 2009/10



Micro Patterned Gaseous Detectors

- High field created by Gas Gain Grids
- Most popular: GEM & Micromegas

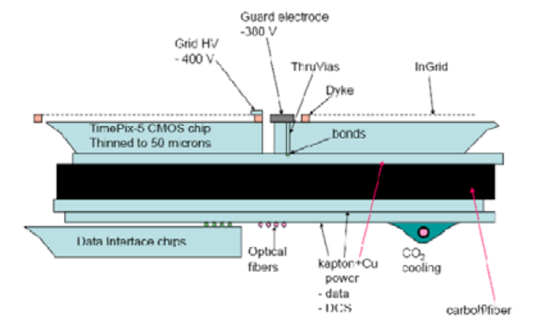
Use 'naked' CMOS pixel readout chip as anode

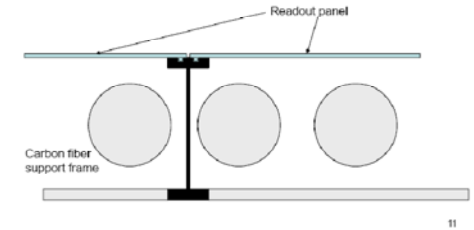
Cooling

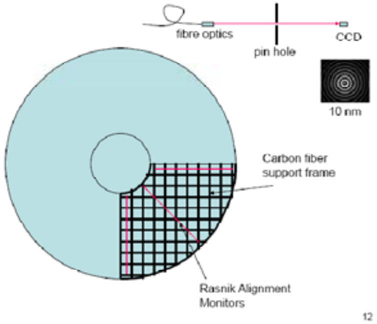
- Timepix power consumption:
  - static digital 0.44 W/chip @ 2.2V Vdd,100MHz
  - max. analog 0.42 W/chip @2.2V Vdd
- Total ~ 3kW/m^2 , w. pulsed power ~30 W/m^2 ?
  \+ power for data readout (outside gas)!
- Timepix-2 version (0.13 μm CMOS) should consume much less
- Experience at NIKHEF with CO_2 cooling (LHCb)
- But no engineering work done yet for TPC endplate

Follow some slides by Harry van der Graaf:

Cross section of standard GridPix readout panel

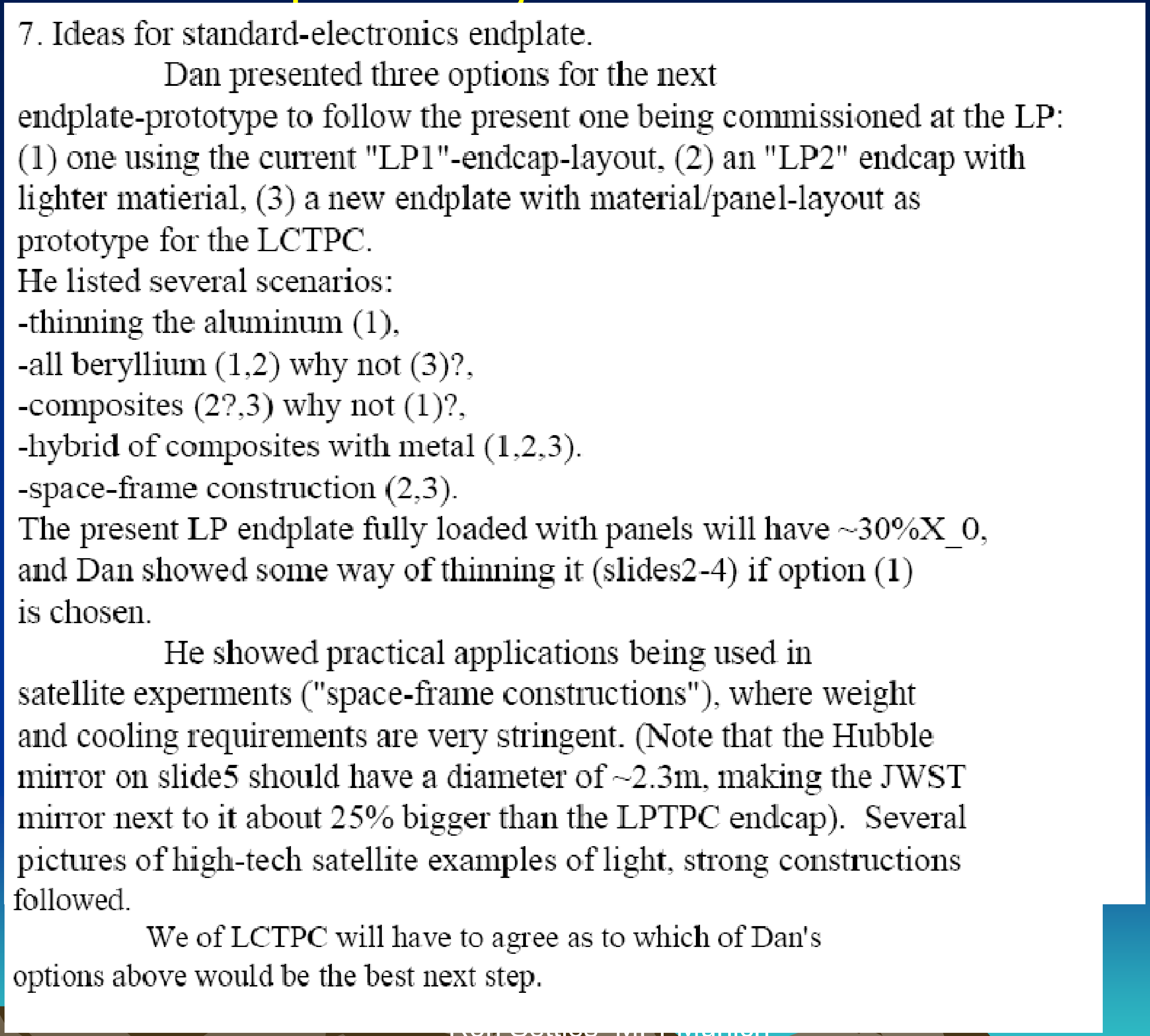






LCTPC engineering model for LOI

- **“Advanced endcap” meeting#5:**



7. Ideas for standard-electronics endplate.

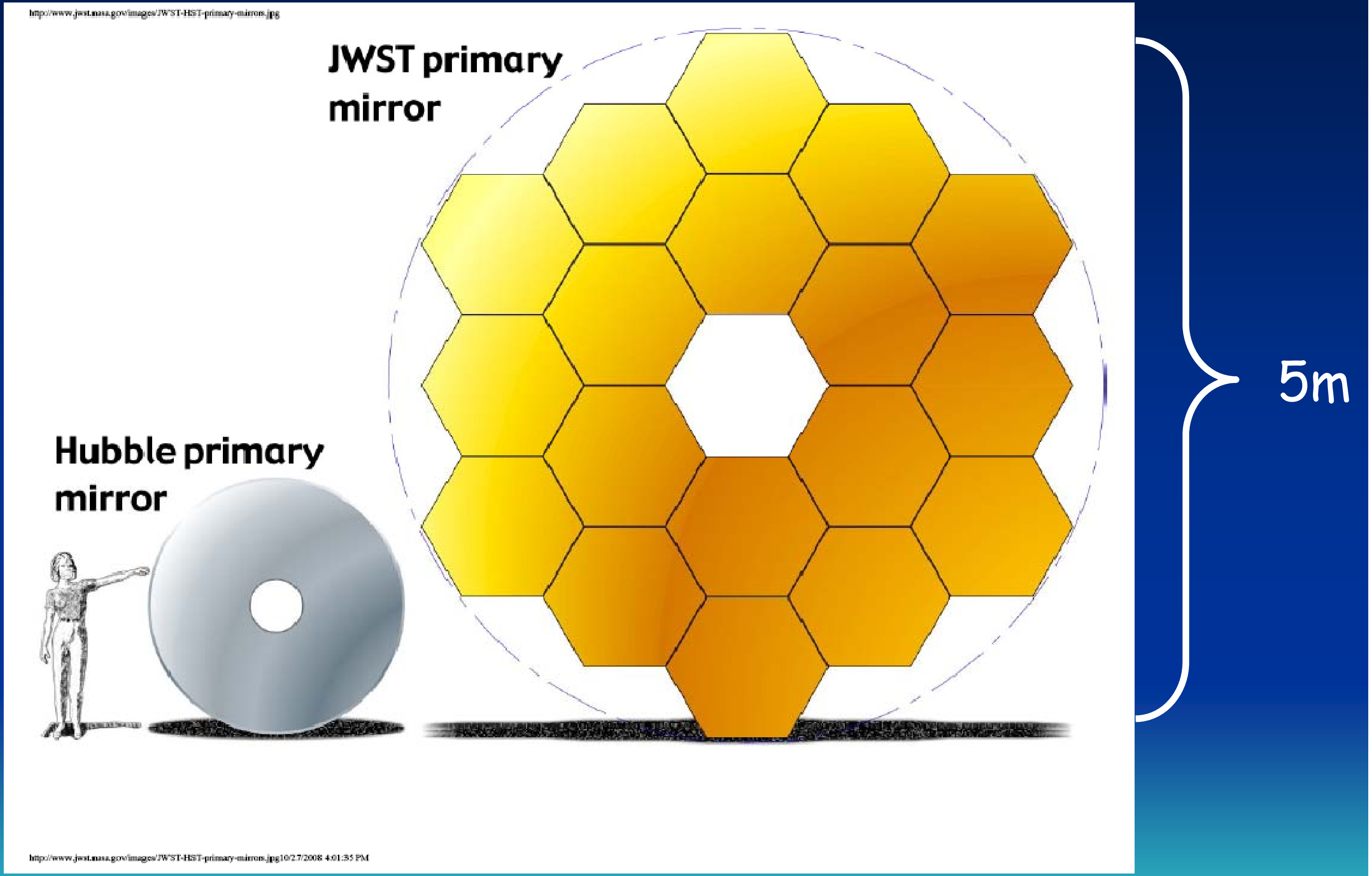
Dan presented three options for the next endplate-prototype to follow the present one being commissioned at the LP: (1) one using the current "LP1"-endcap-layout, (2) an "LP2" endcap with lighter matierial, (3) a new endplate with material/panel-layout as prototype for the LCTPC.
He listed several scenarios:
-thinning the aluminum (1),
-all beryllium (1,2) why not (3)?,
-composites (2?,3) why not (1)?,
-hybrid of composites with metal (1,2,3).
-space-frame construction (2,3).
The present LP endplate fully loaded with panels will have ~30%X_0, and Dan showed some way of thinning it (slides2-4) if option (1) is chosen.

He showed practical applications being used in satellite experments ("space-frame constructions"), where weight and cooling requirements are very stringent. (Note that the Hubble mirror on slide5 should have a diameter of ~2.3m, making the JWST mirror next to it about 25% bigger than the LPTPC endcap). Several pictures of high-tech satellite examples of light, strong constructions followed.

We of LCTPC will have to agree as to which of Dan's options above would be the best next step.

LCTPC engineering model for LOI

- “Advanced endcap” meeting#5, Dan example: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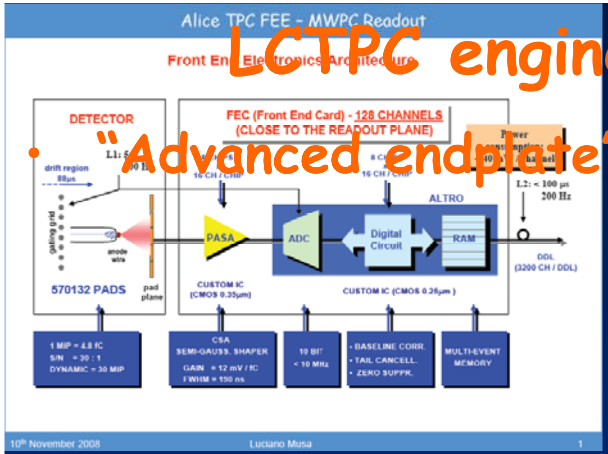
LCTPC engineering model for LOI

• Endplate, electronics, power

- This is about “standard” electronics (CMOS pixel-electronics require a separate study).
- “Advanced endplate” meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate.
- The (sometimes self-contradicting) requirements:
  - Number of pads: as many as possible
    (~10^6 channels per endcap)
  - Power to cool: as small as possible
    0.5mW/channel with **power pulsing->big issue!!!**
    (cooling medium liquid/gas)
  - Endplate material: as stiff and as thin (X_0) as possible
    (purpose of the present exercise)

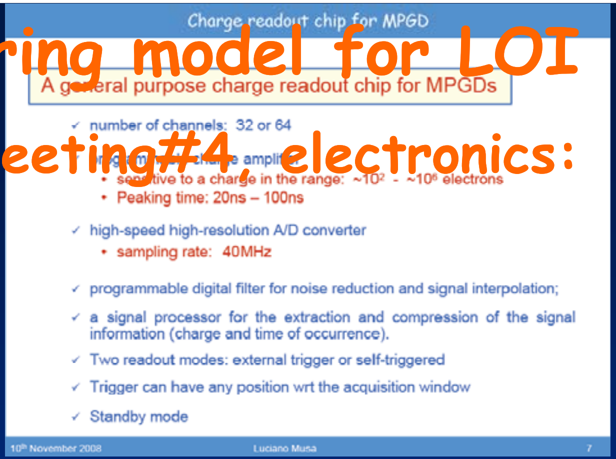
LCTPC engineering model for LOI

- “Advanced endplate” meeting#4, electronics:



Alice TPC FEE - MWPC Readout

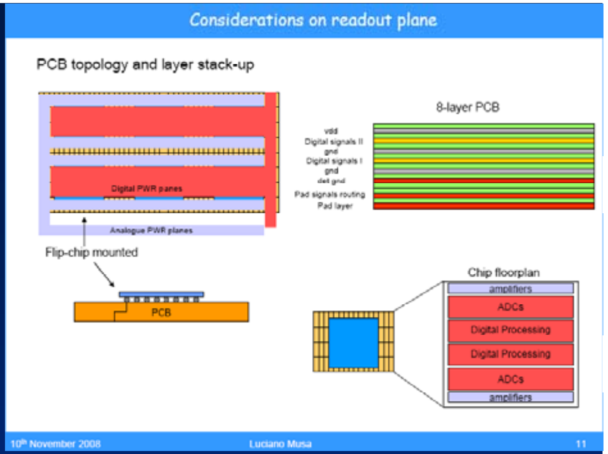
Front End Electronics Architecture



Charge readout chip for MPGD

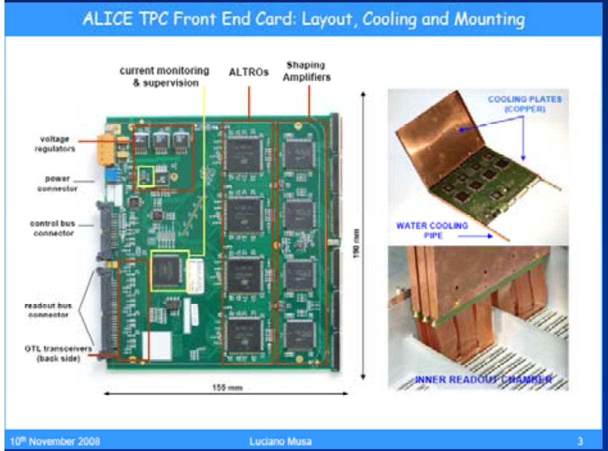
A general purpose charge readout chip for MPGDs

- ✓ number of channels: 32 or 64
- ✓ programmable charge amplifier:
  - sensitive to a charge in the range: ~10^2 - ~10^6 electrons
  - Peaking time: 20ns – 100ns
- ✓ high-speed high-resolution A/D converter
  - sampling rate: 40MHz
- ✓ programmable digital filter for noise reduction and signal interpolation;
- ✓ a signal processor for the extraction and compression of the signal information (charge and time of occurrence).
- ✓ Two readout modes: external trigger or self-triggered
- ✓ Trigger can have any position wrt the acquisition window
- ✓ Standby mode

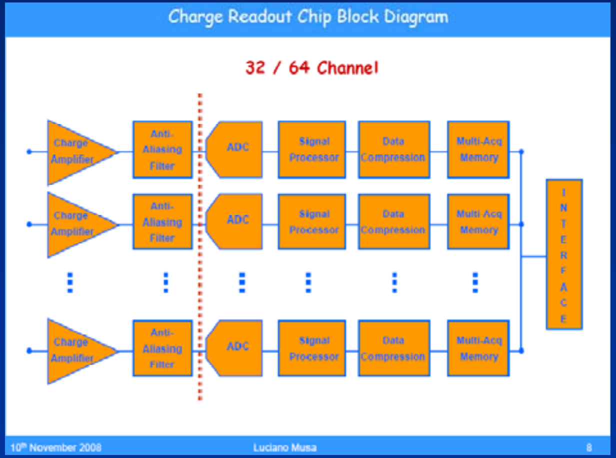


Considerations on readout plane

PCB topology and layer stack-up

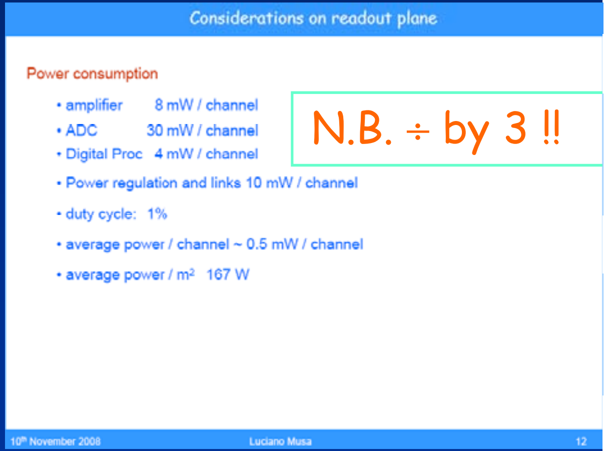


ALICE TPC Front End Card: Layout, Cooling and Mounting



Charge Readout Chip Block Diagram

32 / 64 Channel



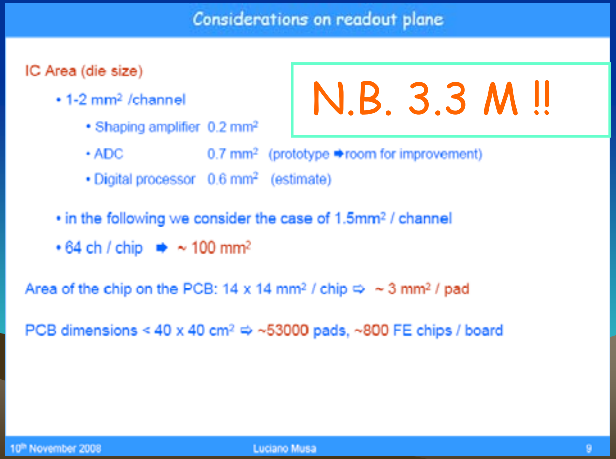
Considerations on readout plane

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- average power / m^2 167 W

N.B. ÷ by 3 !!

Installation of ALICE Front End Electronics (Feb-May '06)



Considerations on readout plane

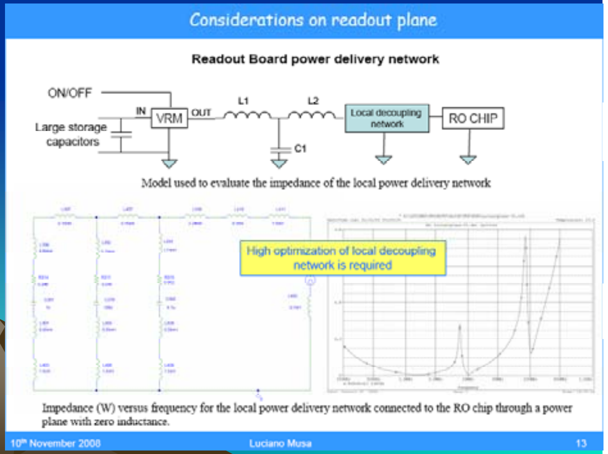
IC Area (die size)

- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.7 mm^2 (prototype ➡room for improvement)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

PCB dimensions < 40 x 40 cm^2 ⇨ ~53000 pads, ~800 FE chips / board

N.B. 3.3 M !!



Considerations on readout plane

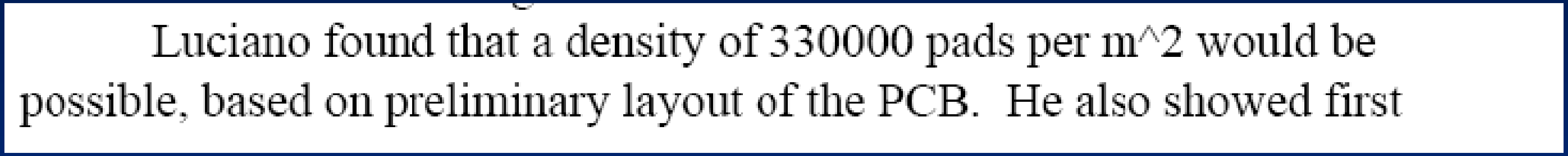
Readout Board power delivery network

Model used to evaluate the impedance of the local power delivery network

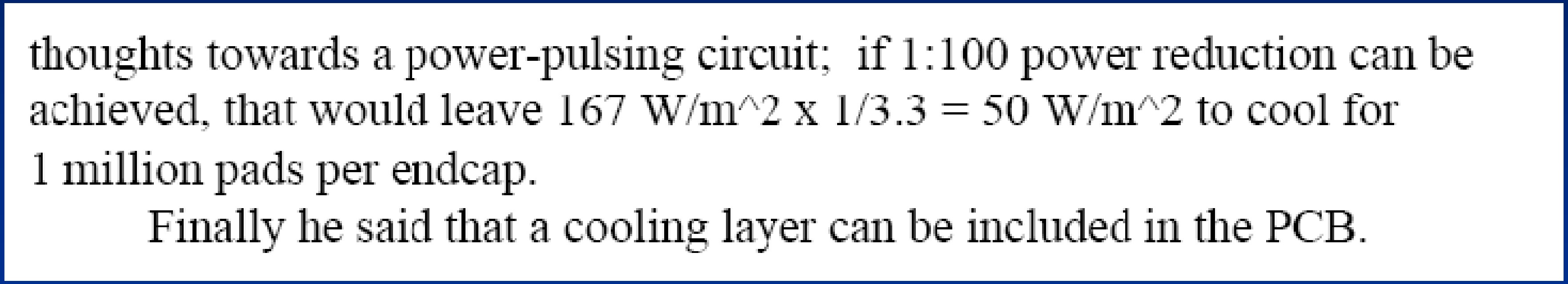
Impedance (W) versus frequency for the local power delivery network connected to the RO chip through a power plane with zero inductance.

LCTPC engineering model for LOI

- Advanced endcap electronics on 10 Nov:



Luciano found that a density of 330000 pads per m^2 would be possible, based on preliminary layout of the PCB. He also showed first

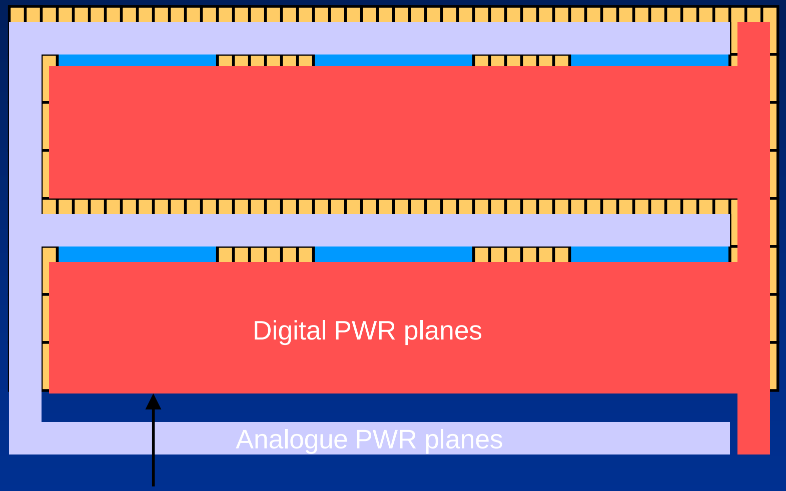


thoughts towards a power-pulsing circuit; if 1:100 power reduction can be achieved, that would leave 167 W/m^2 x 1/3.3 = 50 W/m^2 to cool for 1 million pads per endcap.

Finally he said that a cooling layer can be included in the PCB.

“Considerations on readout plane” (Luciano 10Nov.)

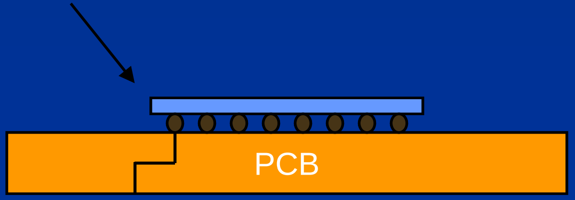
PCB topology and layer stack-up



Digital PWR planes

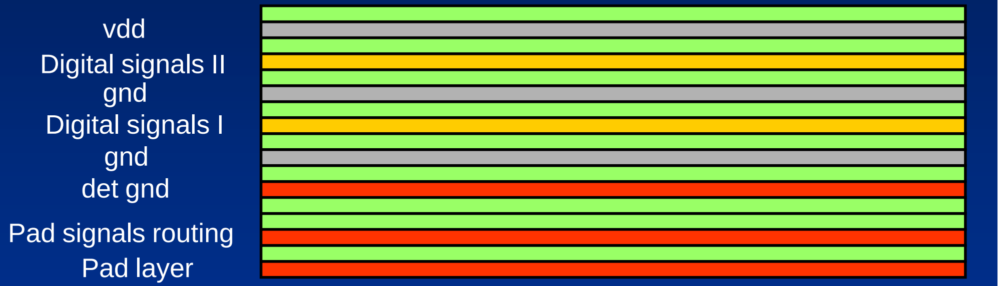
Analogue PWR planes

Flip-chip mounted



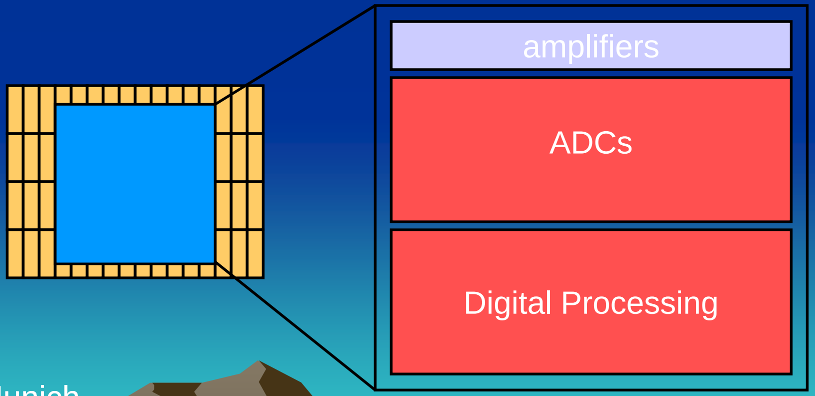
PCB

8-layer PCB



vdd
Digital signals II
gnd
Digital signals I
gnd
det gnd
Pad signals routing
Pad layer

Chip floorplan



amplifiers

ADCs

Digital Processing

More on readout plane

IC Area (die size)

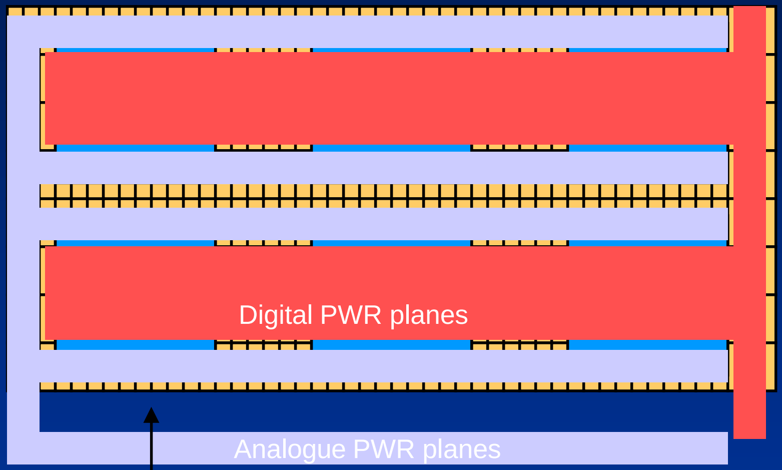
- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.6 mm^2 (estimate)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

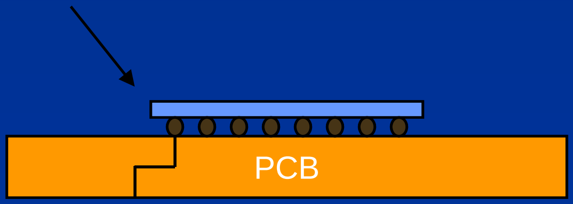
Pads: 64 ch times 1.27mm x 6.3mm pads (8mm2) = 512mm2 of pads/chip

If this is correct, then

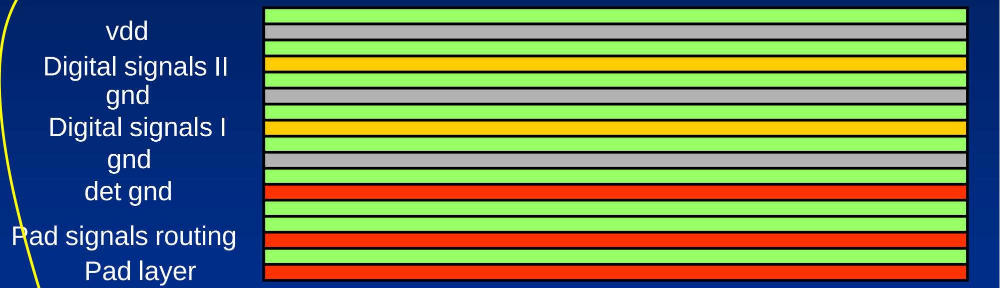
PCB topology and layer stack-up



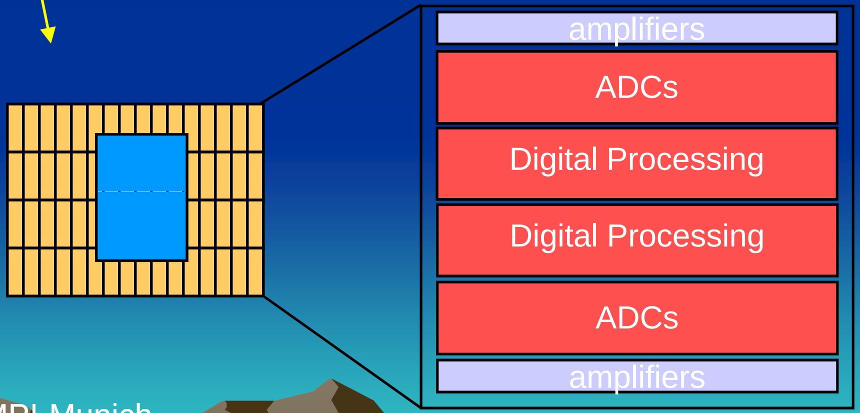
Flip-chip mounted



8-layer PCB



Chip floorplan

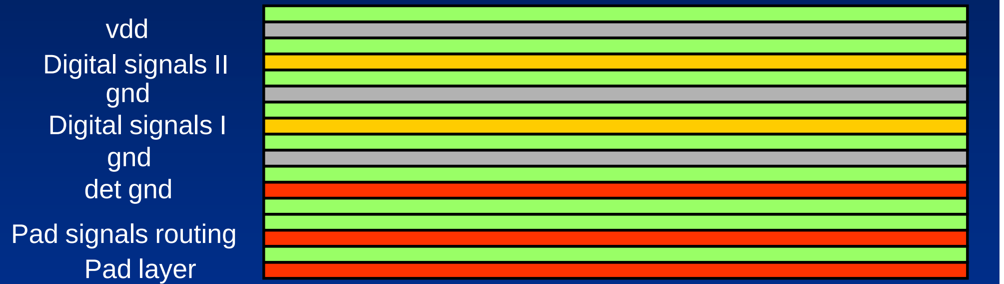


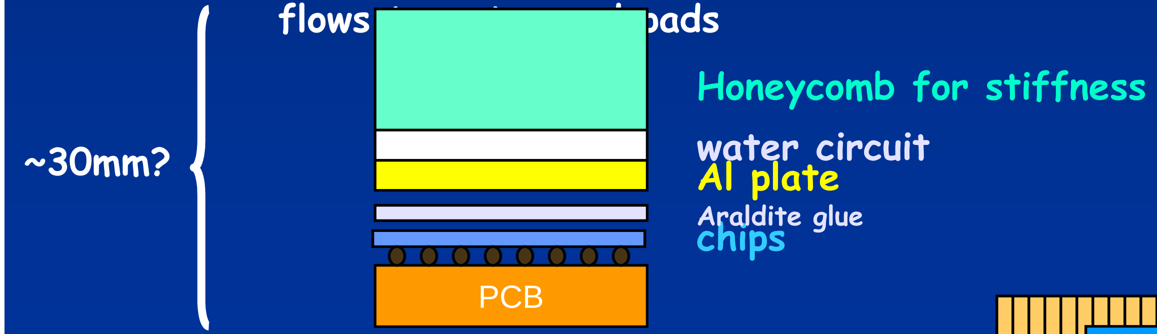
Questions

8-layer PCB:
1. **How thick?**
2. **Thermal conduct. = G10?**

Possible **module** layout thicknesses:
- 5?mm PCB+chips
- 2mm Al plate
- 5mm water circuit
- 10mm honeycomb

λ/d G10 = 100 W/m^2 °K
λ/d Al = 10^5 W/m^2 °K
-> 80W/m^2 and 20W/m^2)
flows [illegible] pads





Honeycomb for stiffness

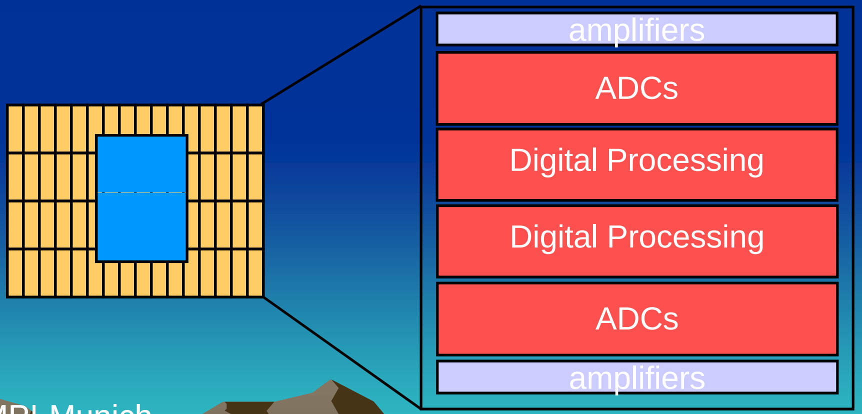
water circuit

Al plate

Araldite glue

chips

Chip floorplan O.K.?



Scenario for readout plane

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- **average power / m^2 50 W -> assume 100 W to be safe**

Layout:

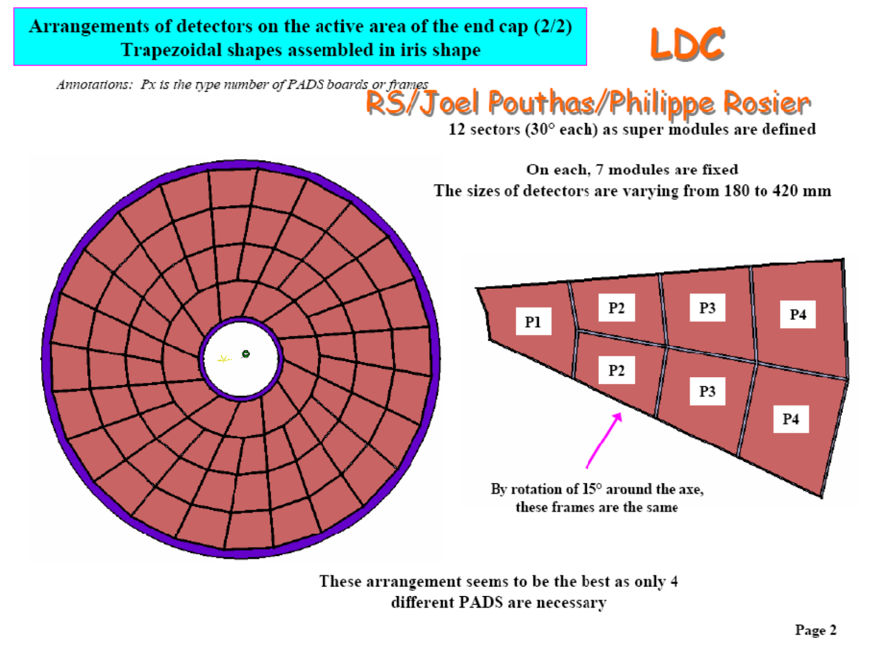
- 10 m^2 per endcap
- 0.1 m^2 per module => 100 modules/endcap
- 10000 pads/module=> .08 m^2 pads, .02m^2 “services”
- 10 W per module

Scenario for readout plane

10000 pads/module => 156 chips per module

LCTPC engineering model for LOI

- "Advanced endcap" Dan: I am in contact with him about the module layout on the endcap. Past examples:



Arrangements of detectors on the active area of the end cap (2/2)
Trapezoidal shapes assembled in iris shape

LDC

Annotations: Px is the type number of PADS boards or frames

RS/Joel Pouthas/Philippe Rosier

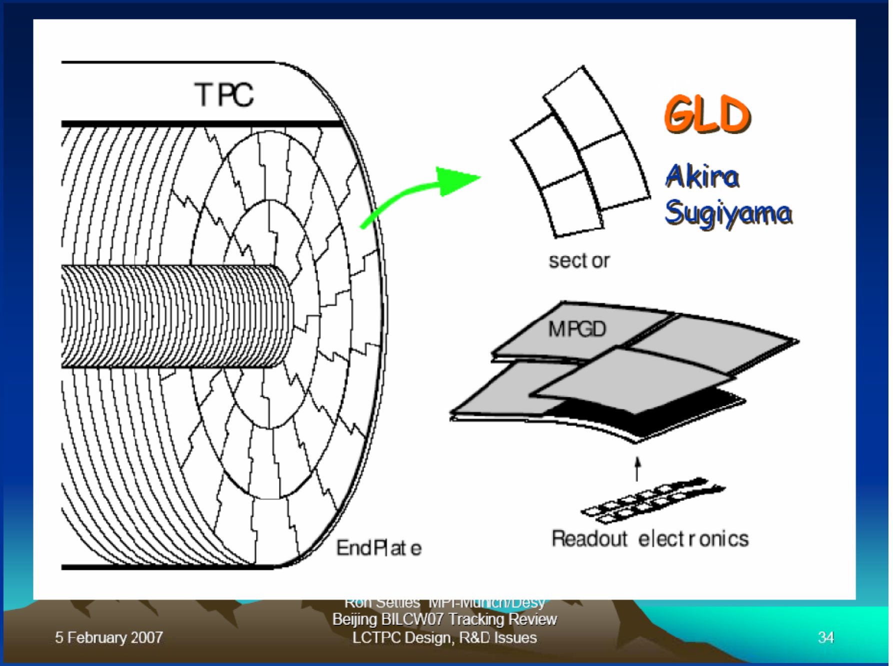
12 sectors (30° each) as super modules are defined

On each, 7 modules are fixed
The sizes of detectors are varying from 180 to 420 mm

By rotation of 15° around the axe, these frames are the same

These arrangement seems to be the best as only 4 different PADS are necessary

Page 2



GLD

Akira Sugiyama

5 February 2007

Ron Settles MPI-Munich/Desy
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LCTPC Design, R&D Issues

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Arrangements of detectors on the active area of the end cap (2/2)
Trapezoidal shapes assembled in iris shape

Annotations: Px is the type number of PADS boards or frames

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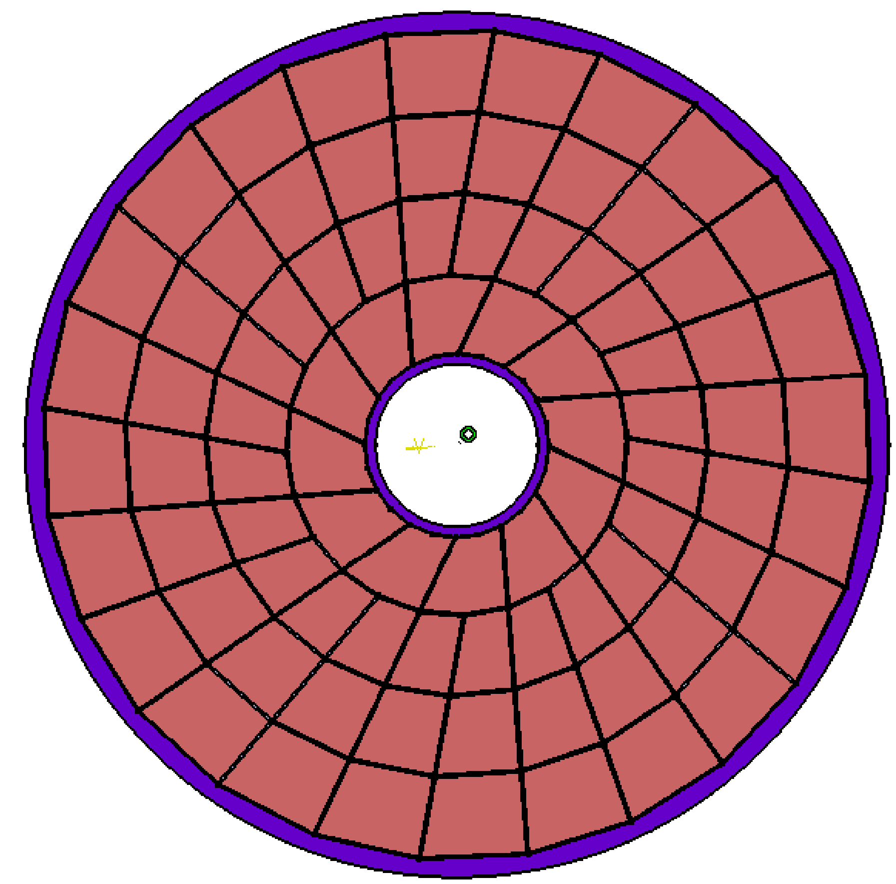
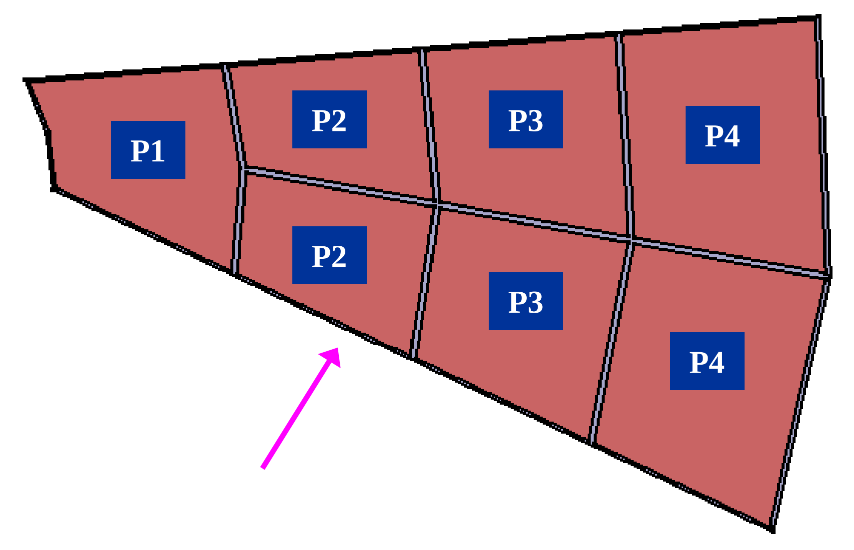
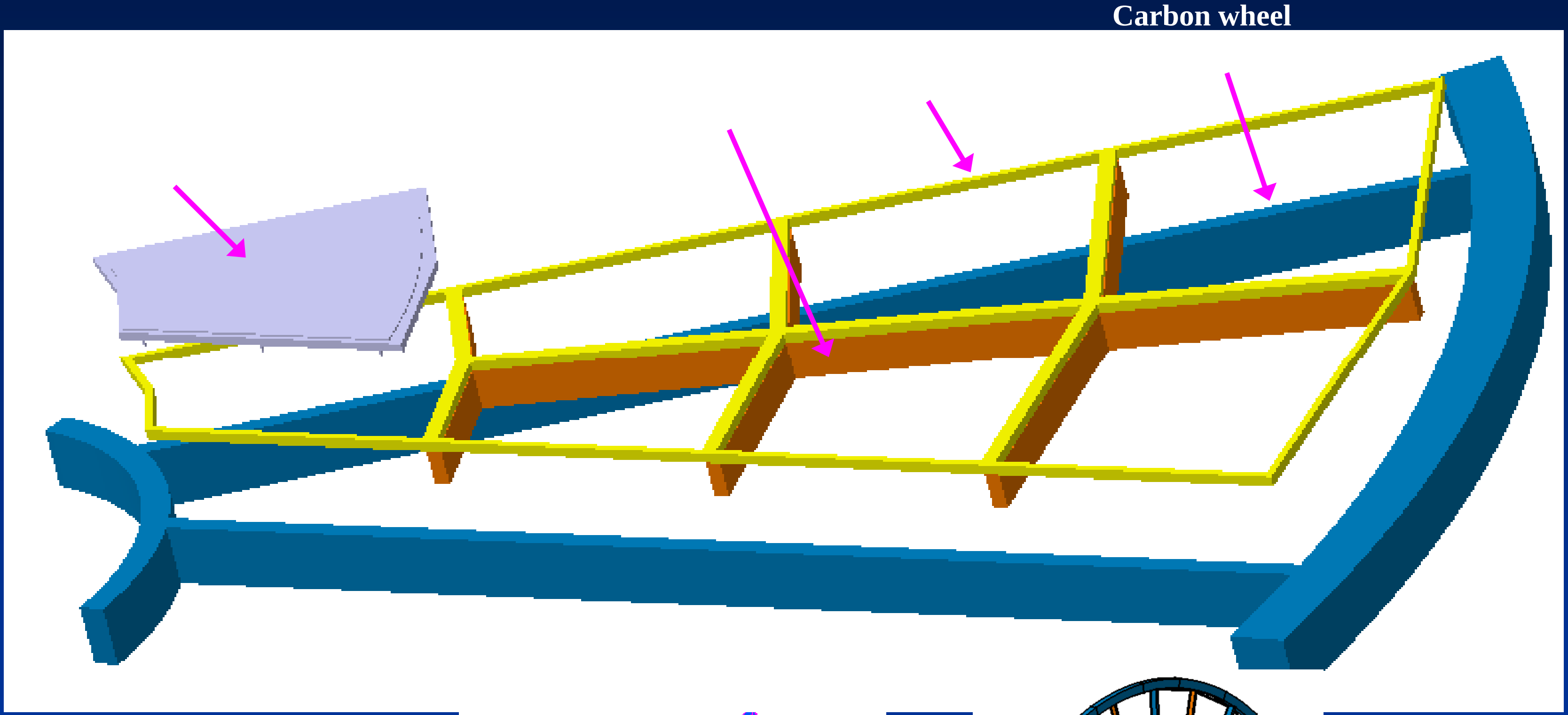




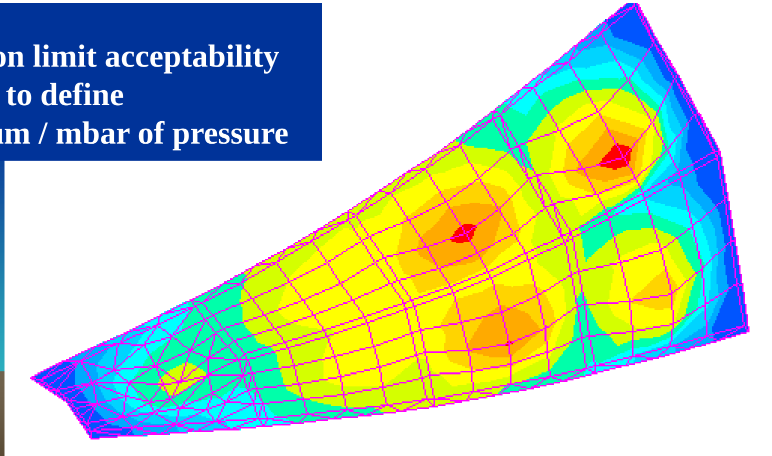
these frames are the same

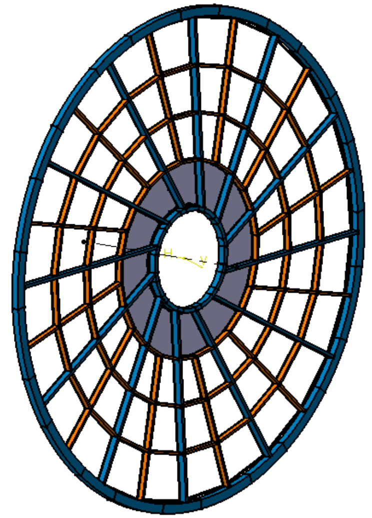
These arrangement seems to be the best as only 4 different PADS are necessary

Principle for a Super Module equipped with detector 1



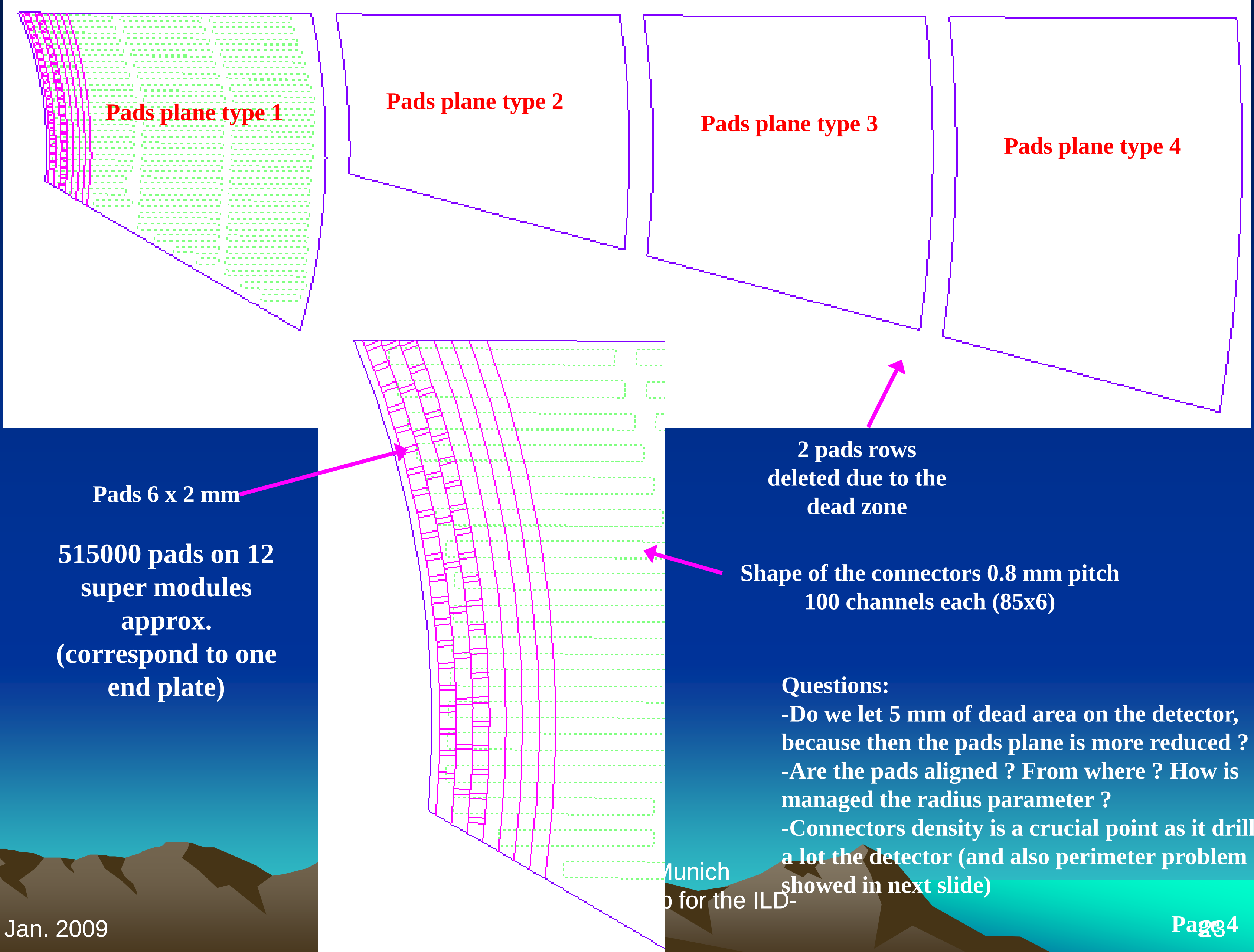
Deformation limit acceptability
to define
Here is 20 µm / mbar of pressure





Complete wheel
with 12 super
modules

Principle for the 4 types of Pads plane



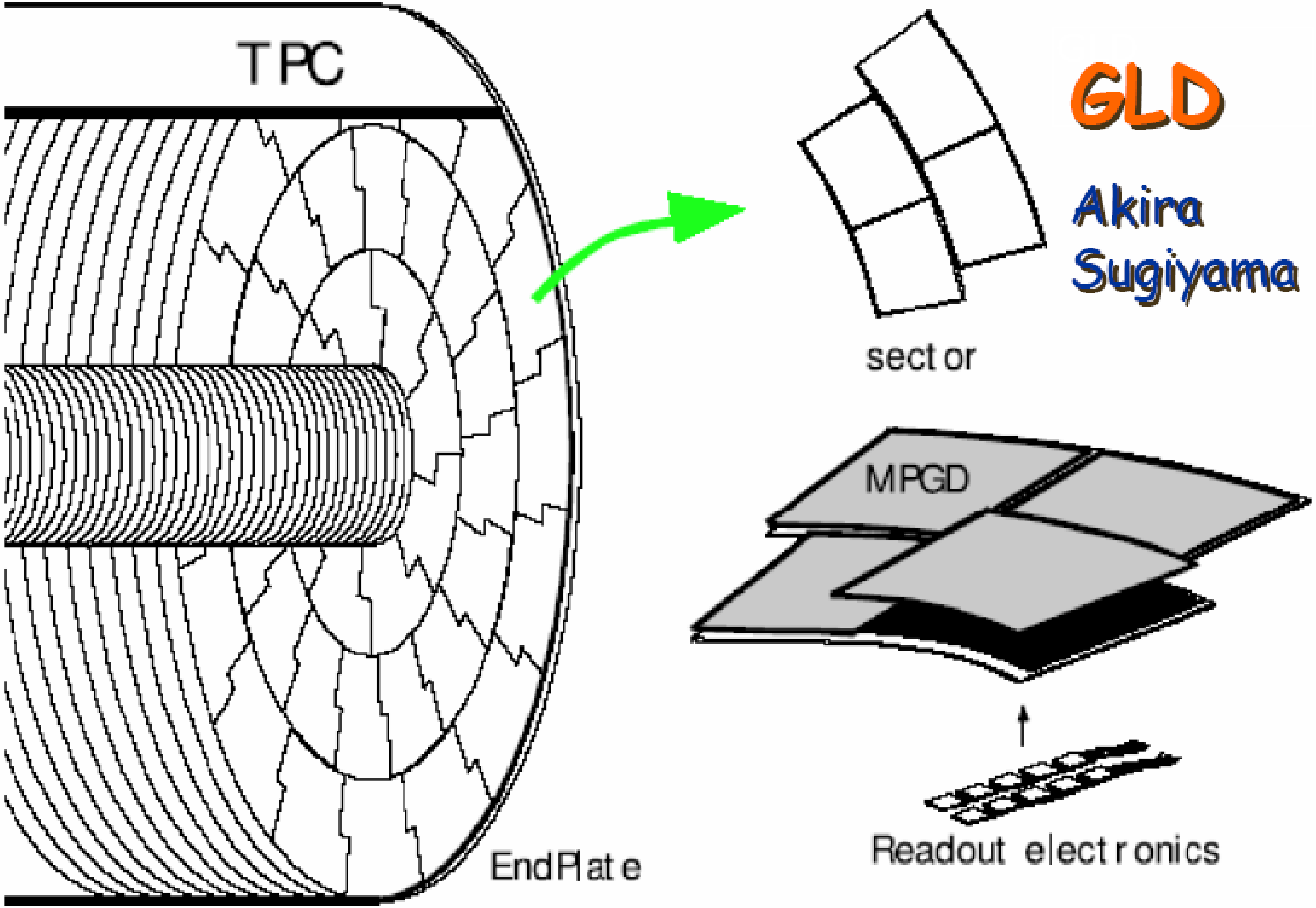
2 pads rows
deleted due to the
dead zone

Pads 6 x 2 mm

515000 pads on 12
super modules
approx.
(correspond to one
end plate)

Shape of the connectors 0.8 mm pitch
100 channels each (85x6)

Questions:
-Do we let 5 mm of dead area on the detector, because then the pads plane is more reduced ?
-Are the pads aligned ? From where ? How is managed the radius parameter ?
-Connectors density is a crucial point as it drills a lot the detector (and also perimeter problem showed in next slide)



GLD

Akira Sugiyama

LCTPC engineering model for LOI

- “Advanced endcap” proposal to Dan, use LP layout and scale to LCTPC size:

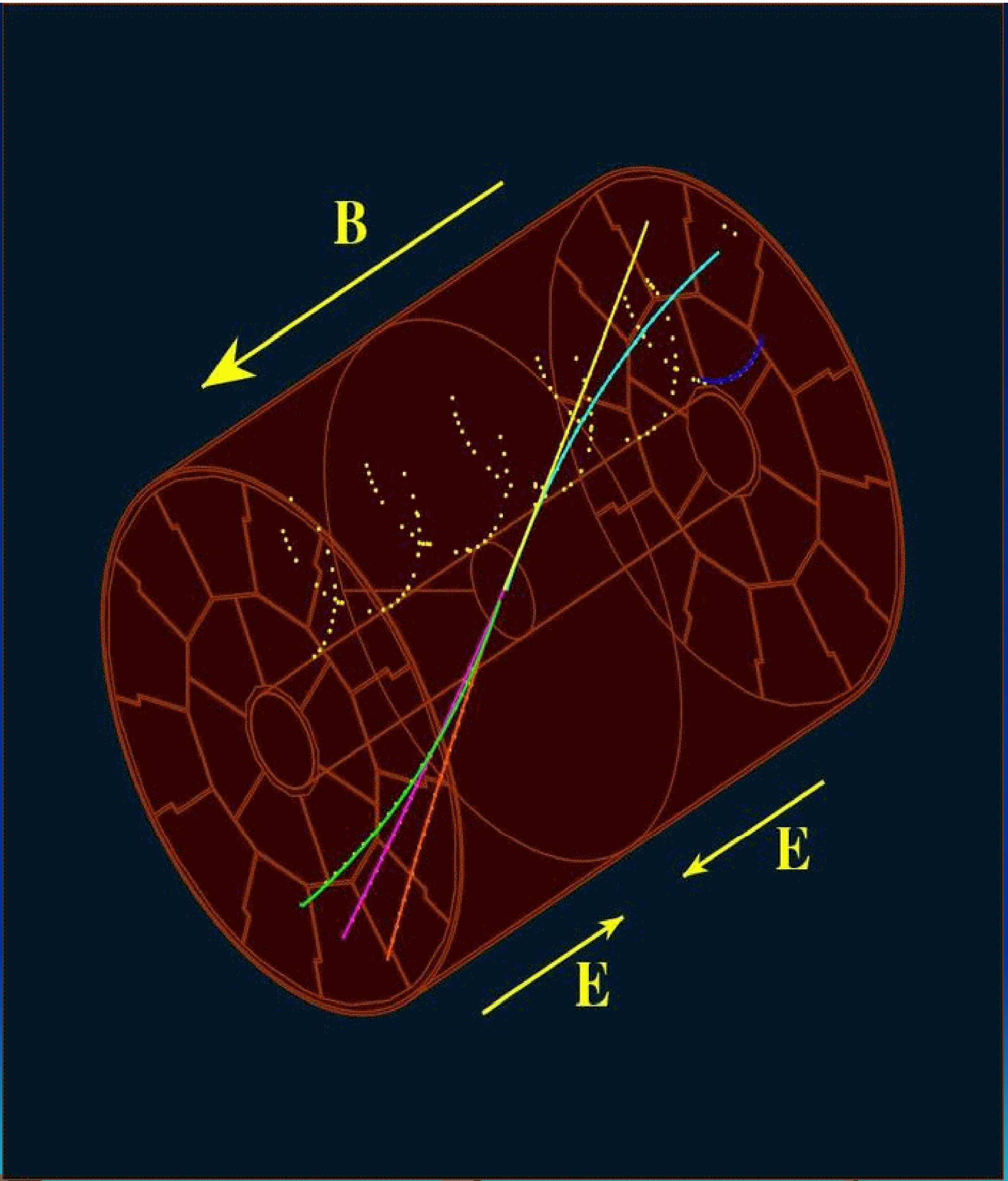
LP:

400cm^2

/module

LCTPC layout:

- 10 m^2 per endcap
- 0.1 m^2 (1000cm^2) per module => 100 modules per endcap
- 10 W per module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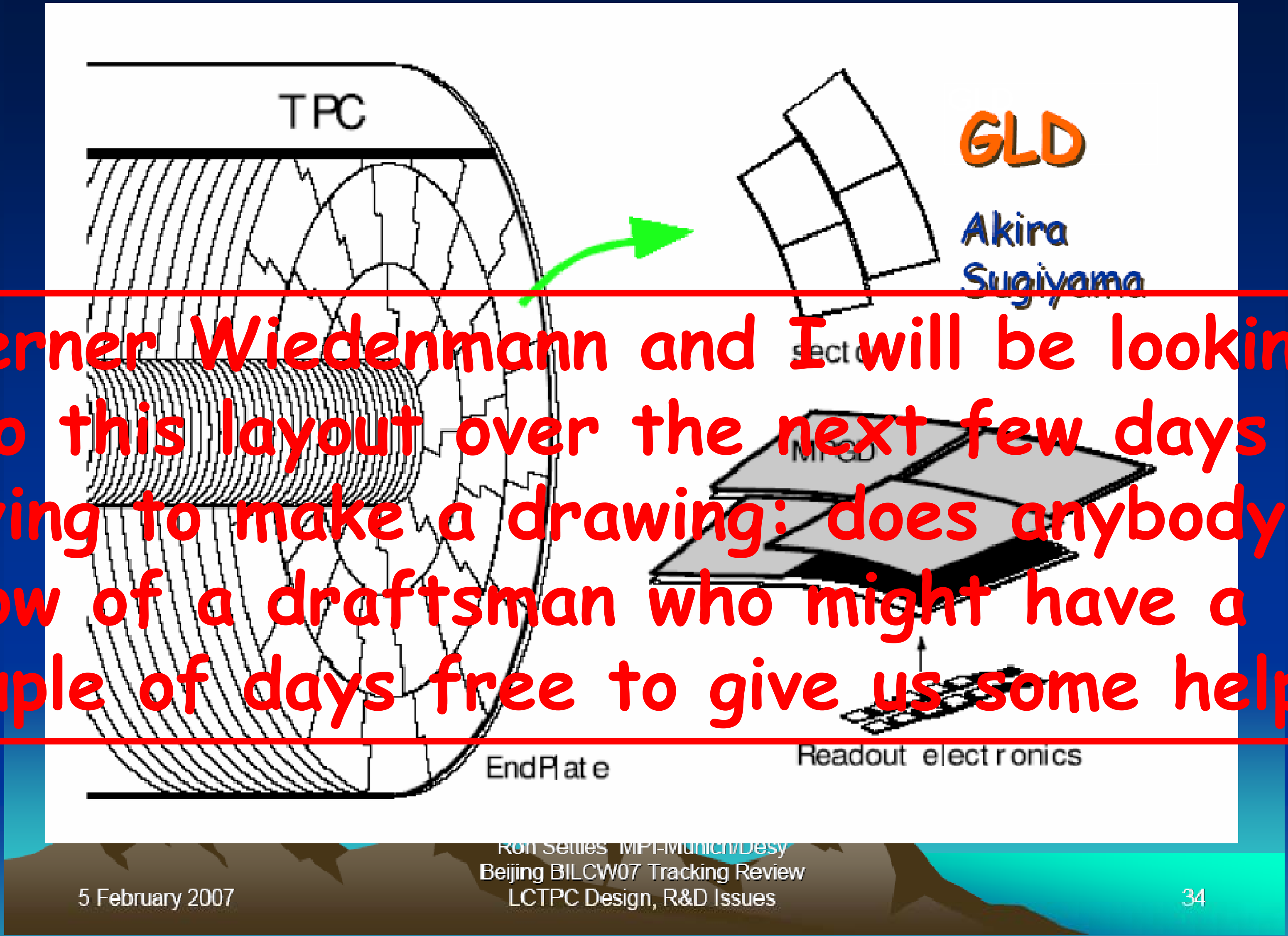

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Werner Wiedenmann and I will be looking into this layout over the next few days and trying to make a drawing: does anybody know of a draftsman who might have a couple of days free to give us some help?