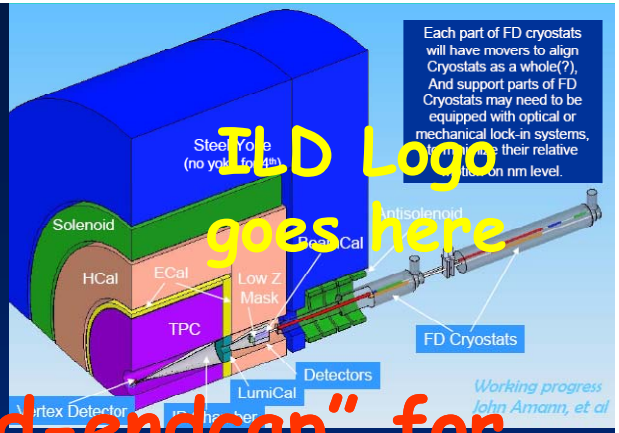
Worldwide Study of the Physics and Detectors for Future Linear e^+e^- Colliders



ILD Logo goes here

Iteration#6b on LCTPC "advanced-endcap" for the ILD LOI… 10.02.2009

LCTPC engineering model for LOI

- "Advanced endcap" meetings now continuing.
- Next steps (updated):

Here is the updated planning up for advanced-endcap meetings up to the ILD LOI.

2007:

--Three meetings #1 14June, #2 26July, #3 10Oct

2008:

--#4 at CERN on 10 Nov 2008: summary see below.

--#5 at LCWS2008 on 15Nov 2008: summary see below.

2009:

--#6a at CERN on 19Jan 2009: summary see below.

--#6b at Desy on 10Feb 2009 8:30-10:00 (room to be announced)

--#7 at ILD Korea (16-18 Feb 2009), advanced endcap during ILD meeting if needed.

--#8 at TIPP09, on 11 March 2009 (place,time to be announced}

LCTPC engineering model for LOI

• Endplate, electronics, power

- This is about "standard" electronics (CMOS pixel-electronics require a separate study).
- "Advanced endplate" meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate.
- The (sometimes self-contradicting) requirements:
  - Number of pads: as many as possible
    (~10^6 channels per endcap)
  - Power to cool: as small as possible
    0.5mW/channel with **power pulsing->big issue!!!**
    (cooling medium liquid/gas)
  - Endplate material: as stiff and as thin (X_0) as possible
    (purpose of the present exercise)

LCTPC engineering model for LOI

- "Advanced endplate" meetings now continuing to understand the electronic density that will allow building a coolable, stiff, thin endplate. From meeting #4 10.Nov.2008:

Advanced-Endcap#4 10/11/2008
http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=3123
Agenda:
---
1. TPC-endcap issues (15')
Introduction by Ron Settles
2. LCTPC electronics issues (15')
by Luciano Musa
3. Cooling issues from CMS experience (15')
by Alain Herve
4. DAQ issues (15')
by Xavier Janssen

Summary:
---
1. TPC-endcap issues.
- We had three advanced-endcap meetings last year: 14 June, 26 July 2007 and 10 October 2007. The first two covered mainly the new electronics and the third included first thoughts by Luciano on the layout of and heat generated by the "advanced-endcap" electronics.
- There are three main, highly-correlated and sometimes self-contradicting aspects: electronics (as many pads as possible), cooling (as little heat generated as possible) and mechanics (as thin as possible). In addition there are two main developments: standard TPC or pixel TPC.
- The density we choose will be governed by cooling (heat) and mechanics (X_0), as well as by the momentum resolution we want.
How the problem was solved by Aleph was shown: 25% X_0 for 22000 pads a
1.3kW per side cooled using combined water and forced-air cooling.
- The heat generated will depend not only on the electronic density but also on how well the power-switching works. If it turns out we are generating too much heat or the endcap is too thick due to electonic density, we will have to reduce the number of pads and there are ideas as

LCTPC engineering model for LOI

- "Advanced endcap" meeting#4, reminder about cooling

(will come back to electronics in a moment):

3. Cooling issues from CMS experience.

Alain reviewed the ideas used for CMS; these ideas are meant to open the discussion for the lctpc:

- Each sub-detector is basically adiabatic wrt others.
- The bulk of heat is removed locally by water as near as possible of where heat is created. Water is still the best liquid for that; there exist alternatives to water but they are expensive.
- The remaining part of heat is removed by natural convection in the surrounding inert atmosphere; vacuum vessel and massive detector components are used as cold sinks. This is compatible with an inert atmosphere inside the vacuum vessel as required for fire protection.
- Alain expressed concern that power-pulsing may cause problems for the mechnical stability of the detectors.

CMS

Cooling Consideration from CMS Experience

A. Hervé / ETHZ

ILD-endcap studies, 10 November 2008

Introduction

- I have prepared this list at the request of Ron Settles.
- The general concept of ILD seems close enough from the CMS one, that some of the experience can be used directly.
- This is particularly true for fire protection and cooling (for example).

This has been prepared for discussion only.

I - CMS principles that seems useful to be retained

- Active cooling of front-end electronics is *a must* especially in confined areas like Vacuum Tank.
- Temperature stabilization is needed as temperature dependence of sub-detectors is often neglected or known quite late, light detectors, RPCs, ...
- It is good practice that each sub-detector can be considered as an adiabatic, or isothermal enclosure wrt. its neighbors, that is each one is responsible for removing its own thermal flux.
- Air (or gas) cooling is very inefficient, it can be used *at best* to remove residual heat.

II - CMS principles that seems useful to be retained

- The inside of the vacuum tank is inaccessible, although its contains the heart of the experiment in terms of investment in time and cost. It *must* be protected against fire by maintaining an inert atmosphere (enriched in nitrogen) to quench any source of fire ignition.
- Thus, inside VT, gas cooling can only be natural convection. Cold sources must be provided by stabilizing in tempearture the Vacuum Tank itself or the HCAL absorber (for example).
- Liquid cooling is thus mandatory to extract the heat as near as possible from where it is created.
- Water as cooling fluid still seems to be the best choice.

ILD Considerations

- The cycling of power is a tremendous help for keeping the heat inventory as low as possible.
- This has also the advantage of limiting the section of cables and pipes reaching the inner detectors.
- However, I am worried by the consequence of cycling the accompanying Lorentz force at the same 5Hz frequency.
- This could be completely destructive for light detectors like Vertex, Tracker.
- This could also render the alignment and stability of sub-detectors very difficult to achieve.

LCTPC engineering model for LOI

- "Advanced endcap" meeting#4, reminder about cooling daq

(will come back to electronics in a moment):

4. DAQ issues.

Xavier dispayed first thoughts.

- The advanced endplate electronics will be much more highly integrated than now and include more FEC and RCU functionalities. What is put on the endcap and what goes into the electronic hut must be decided.

-For the several options for the advanced-endplate electronics, a common data transfer protocol and DAQ should be defined.

-A "trigger" concept will be needed. E.g., the "trigger" should wake up the electronics before the bunch-train arrival and prepare for arrival of the data, and then put the electronics back to sleep after the bunch train has passed.

-Also data transfer needs redundancy and Xavier showed the architecture being planned by CALICE.

Xavier Janssen - Université Libre de Bruxelles

LP-TPC DAQ for Advanced Endplate

LCTPC Advanced Endplate Meeting, CERN, 10th Nov. 2008

Detector Interface

Detector Interface in ALICE r/o (and test beams):

- Detector side: Up to 32 FECs connected to RCU
- Data transfert: via optical link (+ trigger fiber)
- DAQ side: Computer farm with D-RORC receiver PCI-X card

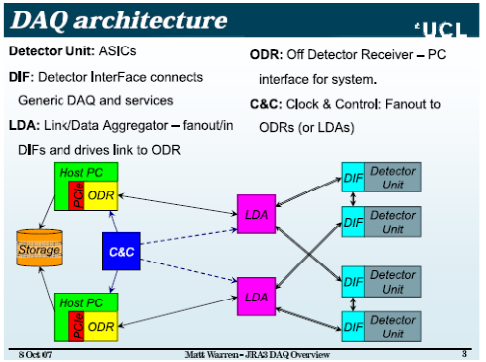
... and for the Advanced Endplate:

- Advanced Endplate integrates FEC functionalities
- RCU functionality should fit with (on ?) the Endplate size
- Data transfert should integrate redundancy (see later)
- "Trigger" concept should be defined (see later)
- DAQ side: should be defined

⟹ Need to do all of above in line with CDAQ of future experiment.

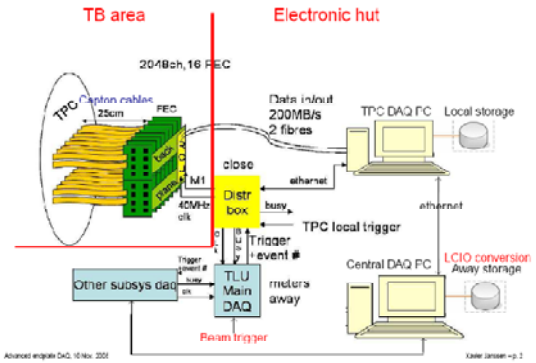
Redundancy issue: CALICE example

CALICE is building a DAQ architecture with redundant data path:



The final TPC DAQ should also include a redundancy of data path to avoid the impact of intermediate electronic failure

ALTRO r/o: LC-TPC DAQ for Test Beams



Data transfer issue

Several possible technologies for the Advanced endplate:

- Gaseous detecor + ADC electronic: ALTRO or AFTER
- Gaseous detecor + TDC electronic: Rostock University
- Si detector: Timepix, Medipix, ...
- Other (yet unknown ?) possibilities

⟹ Need for a common data transfer protocol from the different frontend electronic to a common base DAQ electronic.

"Trigger" and data synchronisation tasks:

- Wake-up electronic before bunch train arrival
- Trigger data acquisition synchroneous to bunch train.
- Flag data with bunch train number / some kind of ID.
- Put electronic in sleep mode after bunch train.

⟹ All this is part of a common data transfer protocol probably.

LCTPC engineering model for LOI

- "Advanced endcap" meeting#5:

6. Ideas for pixel endplate.

Jan reviewed the status of the pixel work which is progressing mainly with the two MPGD amplifications, micromegas and gem. After showing that pixel chip medipix could record tracks in first attempts, timed readout (timepix) was then developed, as was a discharge protection layer. An integrated production of pixelchip, discharge protection and MSGC has been successfully demonstrated. Alternatve gem grids (running in a mode similar to micromegas), double micromegas layers (twingrid), as well as configurations with more integration seen on Jan's slides6-8 are being attempted. The cooling (slide9) of 30W/m^2 would be easy to solve if a factor of 100 can be gained from the power pulsing. First ideas for the layout from Harry van der Graaf are shown on slides10-12.

It is clear that the cooling strategy whould best be the same for all ILD subdetectors (see point 3. above) for reasons of simplicity (not to make the same mistake as some LHC detectors).

LCTPC engineering model for LOI

- "Advanced endcap" meeting#5, Jan example:

A Silicon TPC System

LPTPC endplate discussion
Chicago. 15 November 2008

Jan Timmermans
NIKHEF

1

Multichip boards

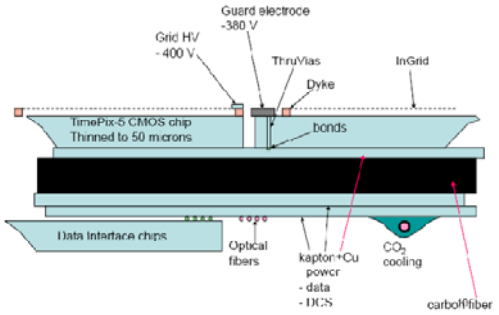
- Bonn: two 4-chip boards for LCTPC
- Saclay: 8-chip board for LCTPC
- NIKHEF: 4-chip board (working in readout)

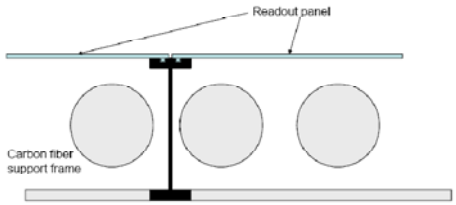
All had problems with power(regulation); being solved

- NIKHEF also aiming for 8x8-chip system in 2009/10

8

Cross section of standard GridPix readout panel

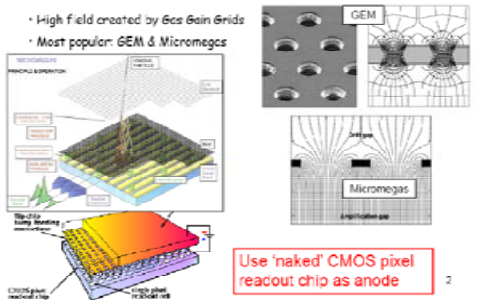




11

Micro Patterned Gaseous Detectors

- High field created by Gas Gain Grids
- Most popular: GEM & Micromegas



Use 'naked' CMOS pixel readout chip as anode

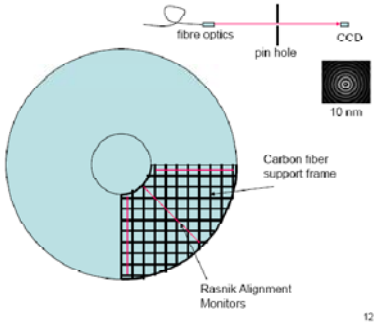
2

Cooling

- Timepix power consumption:
  - static digital 0.44 W/chip @ 2.2V Vdd,100MHz
  - max. analog 0.42 W/chip @2.2V Vdd
- Total ~ 3kW/m^2 , w. pulsed power ~30 W/m^2 ?
  + power for data readout (outside gas)!
- Timepix-2 version (0.13 µm CMOS) should consume much less
- Experience at NIKHEF with CO_2 cooling (LHCb)
- But no engineering work done yet for TPC endplate

Follow some slides by Harry van der Graaf:

9



12

LCTPC engineering model for LOI

- "Advanced endcap" meeting#5:

7. Ideas for standard-electronics endplate.

Dan presented three options for the next endplate-prototype to follow the present one being commissioned at the LP: (1) one using the current "LP1"-endcap-layout, (2) an "LP2" endcap with lighter matierial, (3) a new endplate with material/panel-layout as prototype for the LCTPC.

He listed several scenarios:

-thinning the aluminum (1),

-all beryllium (1,2) why not (3)?,

-composites (2?,3) why not (1)?,

-hybrid of composites with metal (1,2,3).

-space-frame construction (2,3).

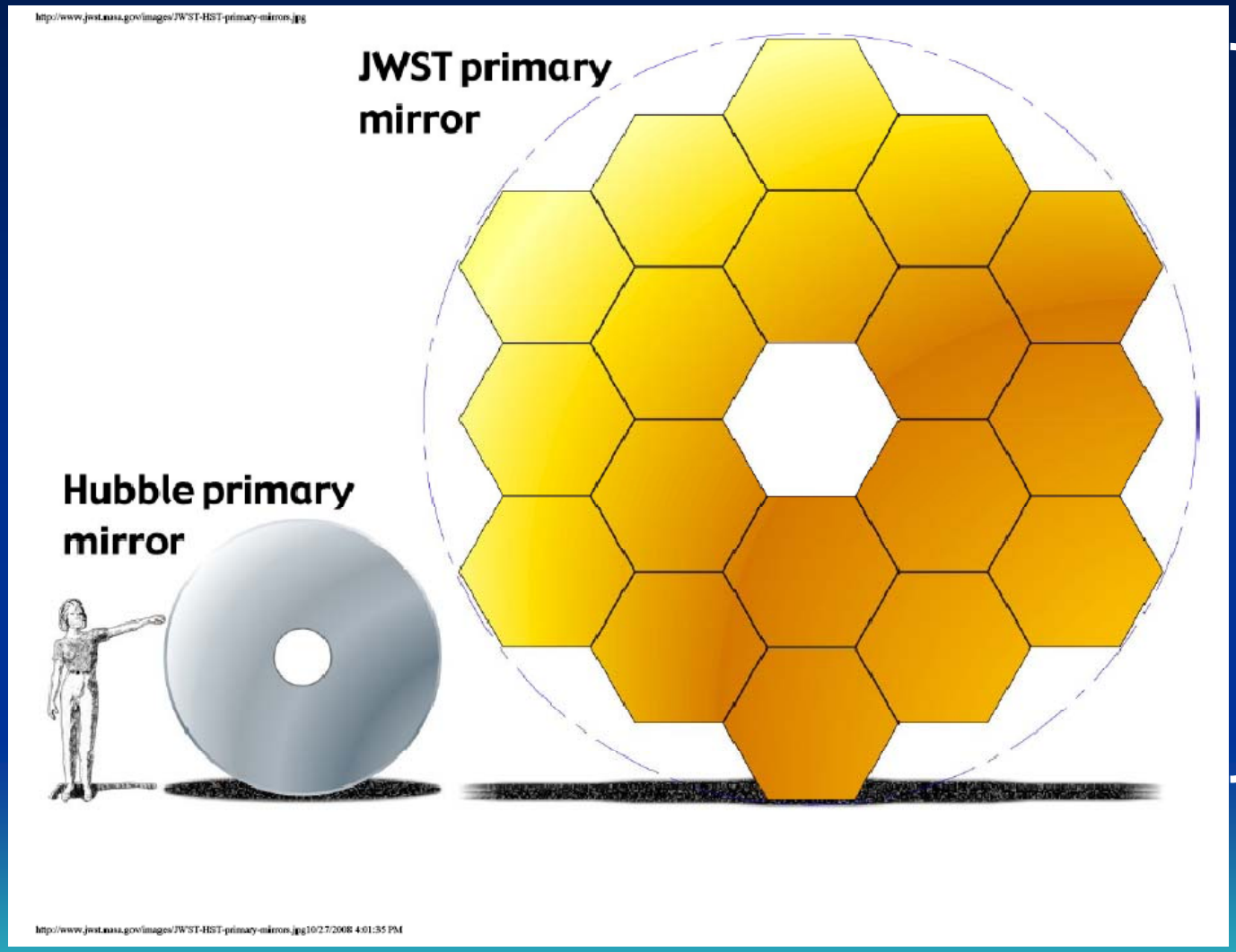
The present LP endplate fully loaded with panels will have ~30%X_0, and Dan showed some way of thinning it (slides2-4) if option (1) is chosen.

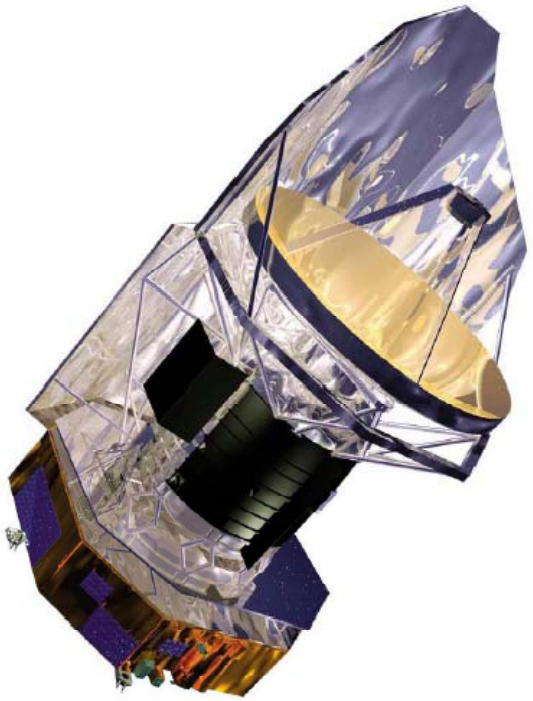
He showed practical applications being used in satellite experments ("space-frame constructions"), where weight and cooling requirements are very stringent. (Note that the Hubble mirror on slide5 should have a diameter of ~2.3m, making the JWST mirror next to it about 25% bigger than the LPTPC endcap). Several pictures of high-tech satellite examples of light, strong constructions followed.

We of LCTPC will have to agree as to which of Dan's options above would be the best next step.

LCTPC engineering model for LOI

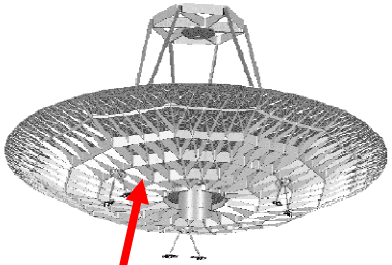
- "Advanced endcap" meeting#5, Dan example:

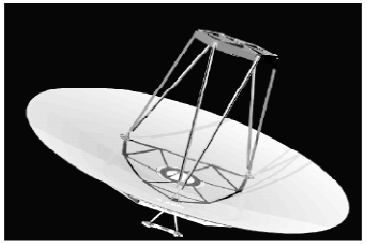




Hershel Telescope
to be launched with Plank

http://herschel.jpl.nasa.gov/
http://sci.esa.int/science-e/www/area/index.cfm?fareaid=16





SiC

3.5m

Ron Settle
LCTPC advance

10 Feb. 2009

This also has a space-frame.
It appears to be a rigid object.

The sensor support is cool.

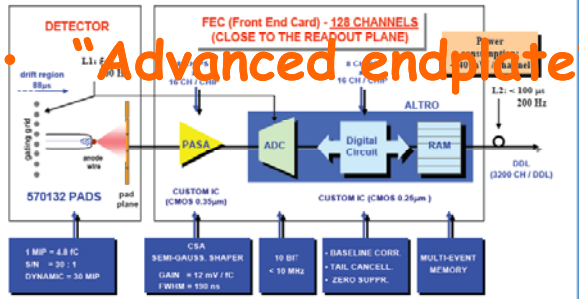
Note the little cones.

LCTPC engineering model for LOI

- "Advanced endplate" meeting#4 electronics:

Alice TPC FEE - MWPC Readout

Front End Electronics Architecture



10th November 2008 Luciano Musa 1

Charge readout chip for MPGD

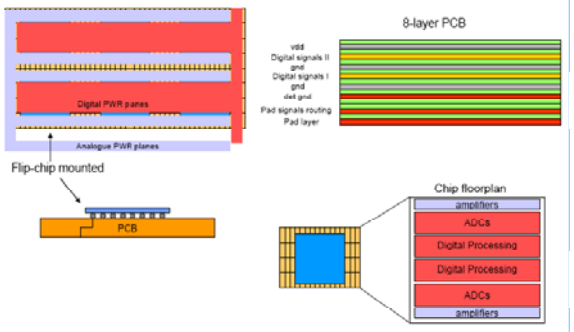
A general purpose charge readout chip for MPGDs

- ✓ number of channels: 32 or 64
- ✓ charge amplifier
  - sensitive to a charge in the range: ~10^2 - ~10^6 electrons
  - Peaking time: 20ns – 100ns
- ✓ high-speed high-resolution A/D converter
  - sampling rate: 40MHz
- ✓ programmable digital filter for noise reduction and signal interpolation;
- ✓ a signal processor for the extraction and compression of the signal information (charge and time of occurrence).
- ✓ Two readout modes: external trigger or self-triggered
- ✓ Trigger can have any position wrt the acquisition window
- ✓ Standby mode

10th November 2008 Luciano Musa 7

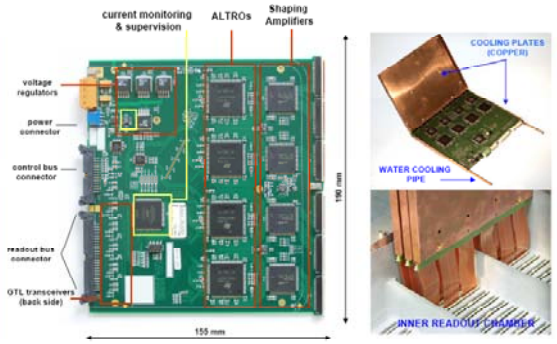
Considerations on readout plane

PCB topology and layer stack-up



10th November 2008 Luciano Musa 11

ALICE TPC Front End Card: Layout, Cooling and Mounting



10th November 2008 Luciano Musa 3

Charge Readout Chip Block Diagram

10th November 2008 Luciano Musa 8

Considerations on readout plane

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- average power / m² 167 W

N.B. ÷ by 3 !!

10th November 2008 Luciano Musa 12

Installation of ALICE Front End Electronics (Feb-May '06)

10th November 2008 Luciano Musa 5

Considerations on readout plane

IC Area (die size)

- 1-2 mm² /channel
  - Shaping amplifier 0.2 mm²
  - ADC 0.7 mm² (prototype ➡ room for improvement)
  - Digital processor 0.6 mm² (estimate)
- in the following we consider the case of 1.5mm² / channel
- 64 ch / chip ➡ ~ 100 mm²

N.B. 3.3 M !!

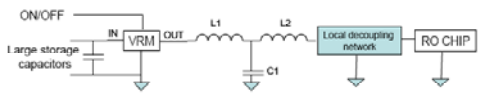
Area of the chip on the PCB: 14 x 14 mm² / chip ⇨ ~ 3 mm² / pad

PCB dimensions < 40 x 40 cm² ⇨ ~53000 pads, ~800 FE chips / board

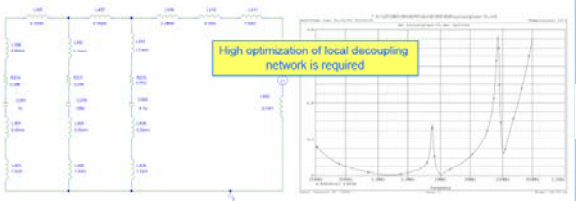
10th November 2008 Luciano Musa 9

Considerations on readout plane

Readout Board power delivery network



Model used to evaluate the impedance of the local power delivery network



Impedance (W) versus frequency for the local power delivery network connected to the RO chip through a power plane with zero inductance.

10th November 2008 Luciano Musa 13

LCTPC engineering model for LOI

- Advanced endcap electronics on 10 Nov:

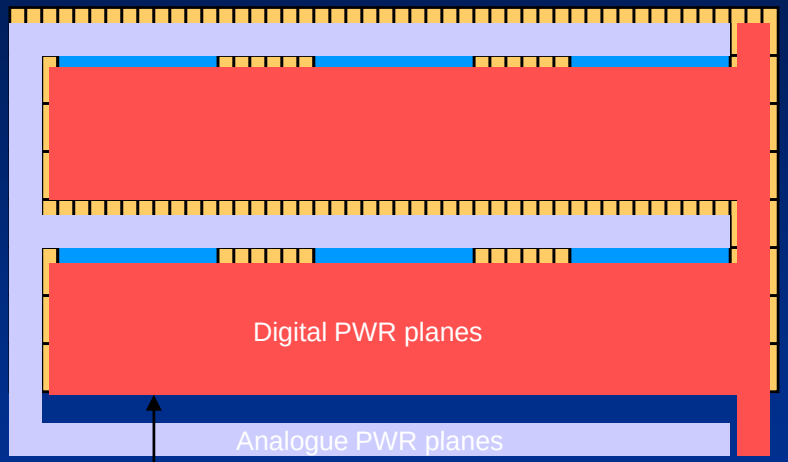
Luciano found that a density of 330000 pads per m^2 would be possible, based on preliminary layout of the PCB. He also showed first

thoughts towards a power-pulsing circuit; if 1:100 power reduction can be achieved, that would leave 167 W/m^2 x 1/3.3 = 50 W/m^2 to cool for 1 million pads per endcap.

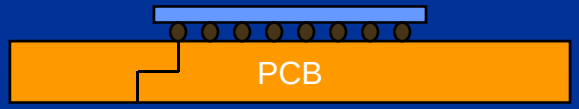
Finally he said that a cooling layer can be included in the PCB.

"Considerations on readout plane" (Luciano 10Nov.)

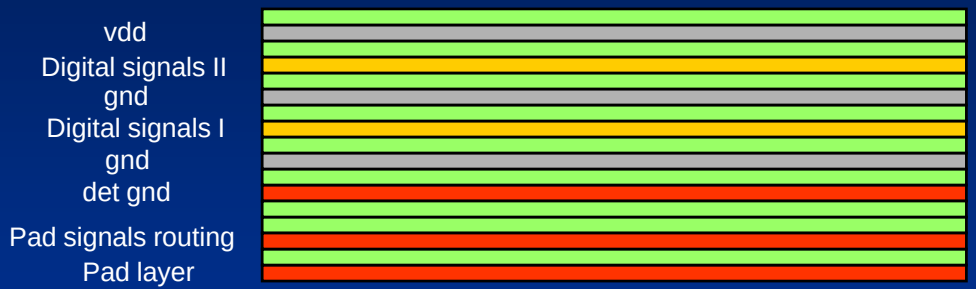
PCB topology and layer stack-up



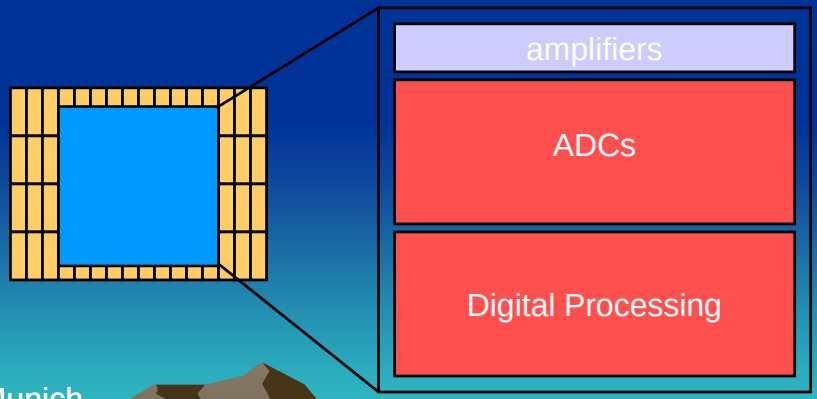
Flip-chip mounted



8-layer PCB



Chip floorplan



Advanced-Endcap#6a 19/01/2009
http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=3334

Summary:

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1. TPC-endcap: summary of progress up to now.

-In addition to the happenings at #4 and #5 below (the line of $$$$), discussions between Luciano Musa, Alain Herve and RS yieled some approximate numbers:
..average power/m2 -> assume 100 W to be safe (Safety Factor=2)
..10 m^2 per endcap
..0.1 m^2 per module => 100 modules/endcap
..10000 pads/module=> .08 m^2 pads, .02m^2 "services"
..10 W per module
-On slide-17 there is a first attempt to put the components together and calculate the heat transfer to the cooling plate and to the padplane.
-RS showed ideas for layouts looked at during the last couple of years
..from Philippe Rosier IPN Orsay (LDC DOD)
..from Akira Sugiyama Saga (GLG DOD)
..from Dan Peterson (for the LP TPC at Desy)
-RS would like to explore Akira's/Dan's ideas (Saclay ideas are very similar, see below) and will be working with Werner Wiedenmann and othe interested colleagues to develop a layout for the ILD LOI. (N.B. The design put into the LOI will by no means represent a final decision since the LOI will just be a start towards a TDR to be submitted in two years.)

More on readout plane

IC Area (die size)

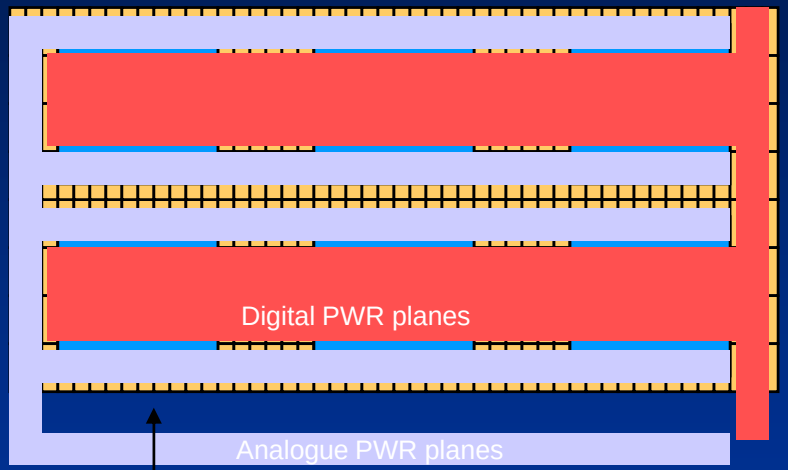
- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.6 mm^2 (estimate)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

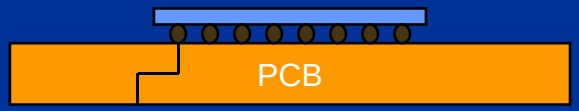
Pads: 64 ch times 1.27mm x 6.3mm pads (8mm2) = 512mm2 of pads/chip

If this is correct, then

PCB topology and layer stack-up

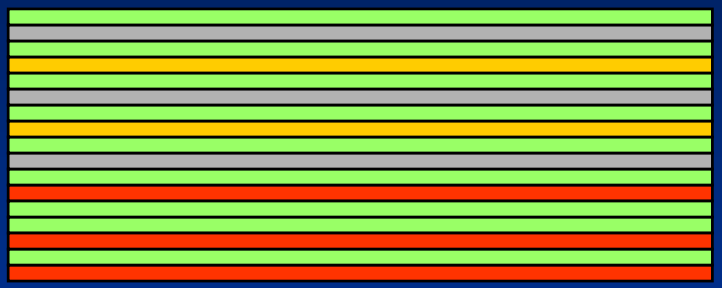


Flip-chip mounted

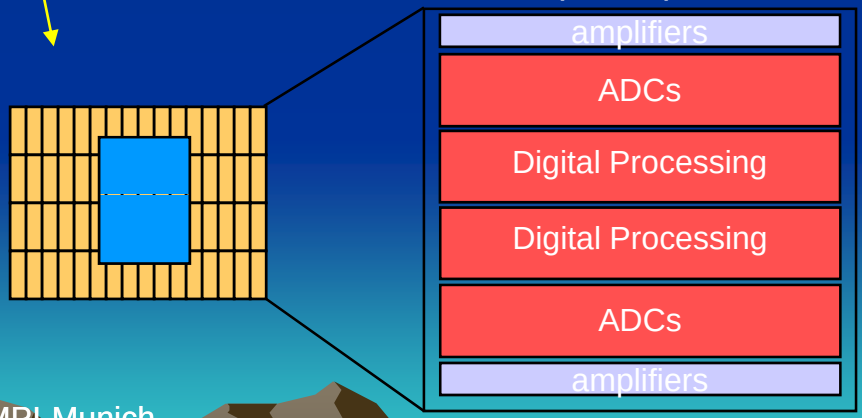


8-layer PCB

vdd
Digital signals II
gnd
Digital signals I
gnd
det gnd
Pad signals routing
Pad layer



Chip floorplan



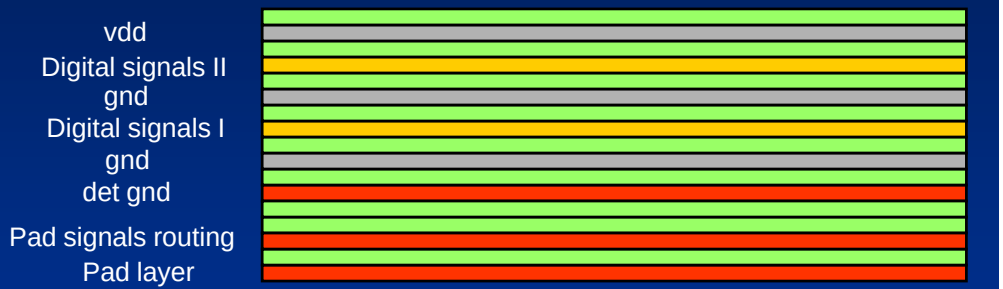
Questions

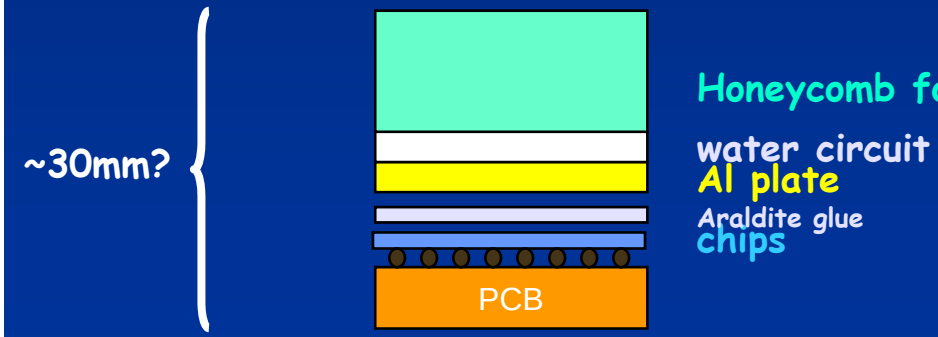
Possible **module** layout thicknesses:

- 5?mm PCB+chips
- 2mm Al plate
- 5mm water circuit
- 10mm honeycomb

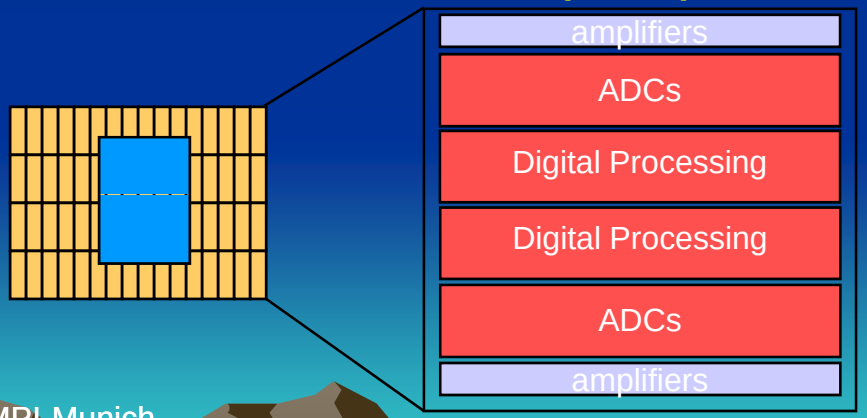
λ/d G10 = 100 W/m^2 °K
λ/d Al = 10^5 W/m^2 °K
-> 80W/m^2 and 20W/m^2)
flows to water and pads

8-layer PCB:
1. **How thick?**
2. **Thermal conduct. = G10?**





Chip floorplan O.K.?



Scenario for readout plane

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- **average power / m^2 50 W -> assume 100 W to be safe**

Layout:

- 10 m^2 per endcap
- 0.1 m^2 per module => 100 modules/endcap
- 10000 pads/module=> .08 m^2 pads, .02m^2 “services”
- 10 W per module

Advanced-Endcap#6a 19/01/2009
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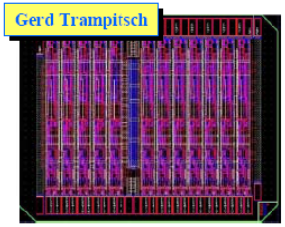
2. LCTPC electronics progress at CERN.
-Magnus reviewed the Alice electronics and the characteristics of the new submission for a new general-purpose charge readout chip for MPGDs. The new submission will have the analog amplifier (already used in the LP) and an ADC prototype combined into one chip (this joining of analog/digital is an attempt, to see if the idea is viable). Dimensions are shown on slide-12 and layout on slide-13. Slide-14 shows how cooling pipes can be inserted at the level of the chips improving the heat-transfer characteristics showed by RS slide-17 above. This idea will be developed further, and the electronics to transfer the data to the outside world will be included.

Charge Readout Chip Development
&
System Level Considerations

19th January 2009 M. Mager - L. Musa 1

Charge Readout Chip – Amplifier and ADC

Gerd Trampitsch



Layout of 12-channel PASA prototype

16 channel Shaping amplifier prototype

- 16-channel 4th order CSA
- programmable polarity
- programmable gain: 12-27 mV/fC
- Programmable peaking time: 30-120ns
- Process: IBM CMOS 0.13 µm
- area: 3 mm²
- 1.5 V single supply, power: <8mW/channel
- **MPR samples (1000): May 07**

Hugo Franca Santos

Layout of 2-channel ADC prototype

2-channel ADC prototype

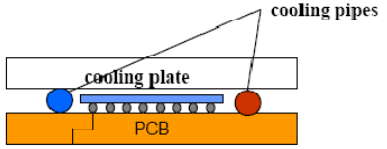
- 10-bit ADC, 40Mhz sampling frequency
- Pipelined differential architecture
- Process: IBM CMOS 0.13 µm
- area: 0.7 mm²
- 1.5 V single supply
- Power/channel: 33mW @ 40Mhz, 10mW @ 20Mhz
- **MPR samples (40): Jan 09**

19th January 2009 M. Mager - L. Musa 10

Considerations on power consumption & cooling

Power consumption (for 30ns peaking time, 40Mhz sampling, 3mm² pad)

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%
- average power / channel ~ 0.5 mW / channel
- average power / m² 167 W



19th January 2009 M. Mager - L. Musa 14

Advanced-Endcap#6a 19/01/2009
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Summary:
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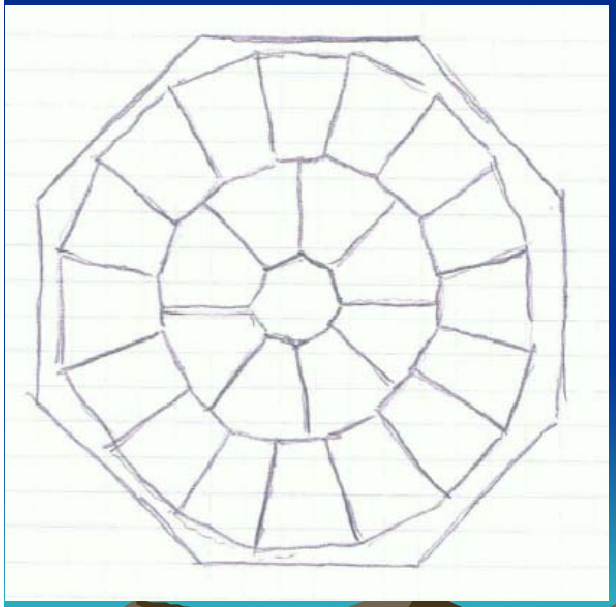
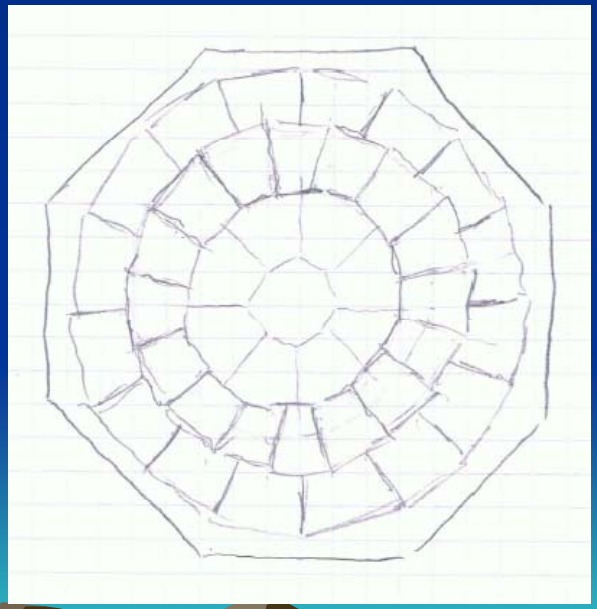
1. TPC-endcap: summary of progress up to now.
-In addition to the happenings at #4 and #5 below (the line of $$$$), discussions between Luciano Musa, Alain Herve and RS yieled some approximate numbers:
..average power/m2 -> assume 100 W to be safe (Safety Factor=2)
..10 m^2 per endcap
..0.1 m^2 per module => 100 modules/endcap
..10000 pads/module=> .08 m^2 pads, .02m^2 "services"
..10 W per module
-On slide-17 there is a first attempt to put the components together and calculate the heat transfer to the cooling plate and to the padplane.
-RS showed ideas for layouts looked at during the last couple of years
..from Philippe Rosier IPN Orsay (LDC DOD)
..from Akira Sugiyama Saga (GLG DOD)
..from Dan Peterson (for the LP TPC at Desy)
-RS would like to explore Akira's/Dan's ideas (Saclay ideas are very similar, see below) and will be working with Werner Wiedenmann and other interested colleagues to develop a layout for the ILD LOI. (N.B. The design put into the LOI will by no means represent a final decision since the LOI will just be a start towards a TDR to be submitted in two years.)

General ideas for number of sector-rows

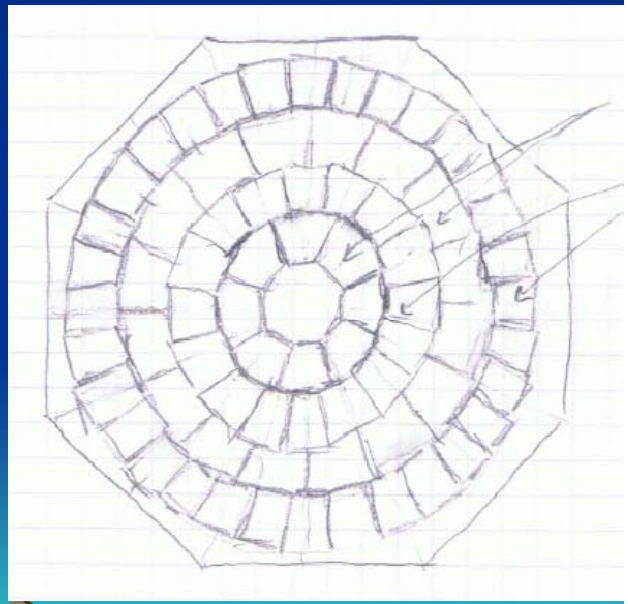
2-rows (Aleph)

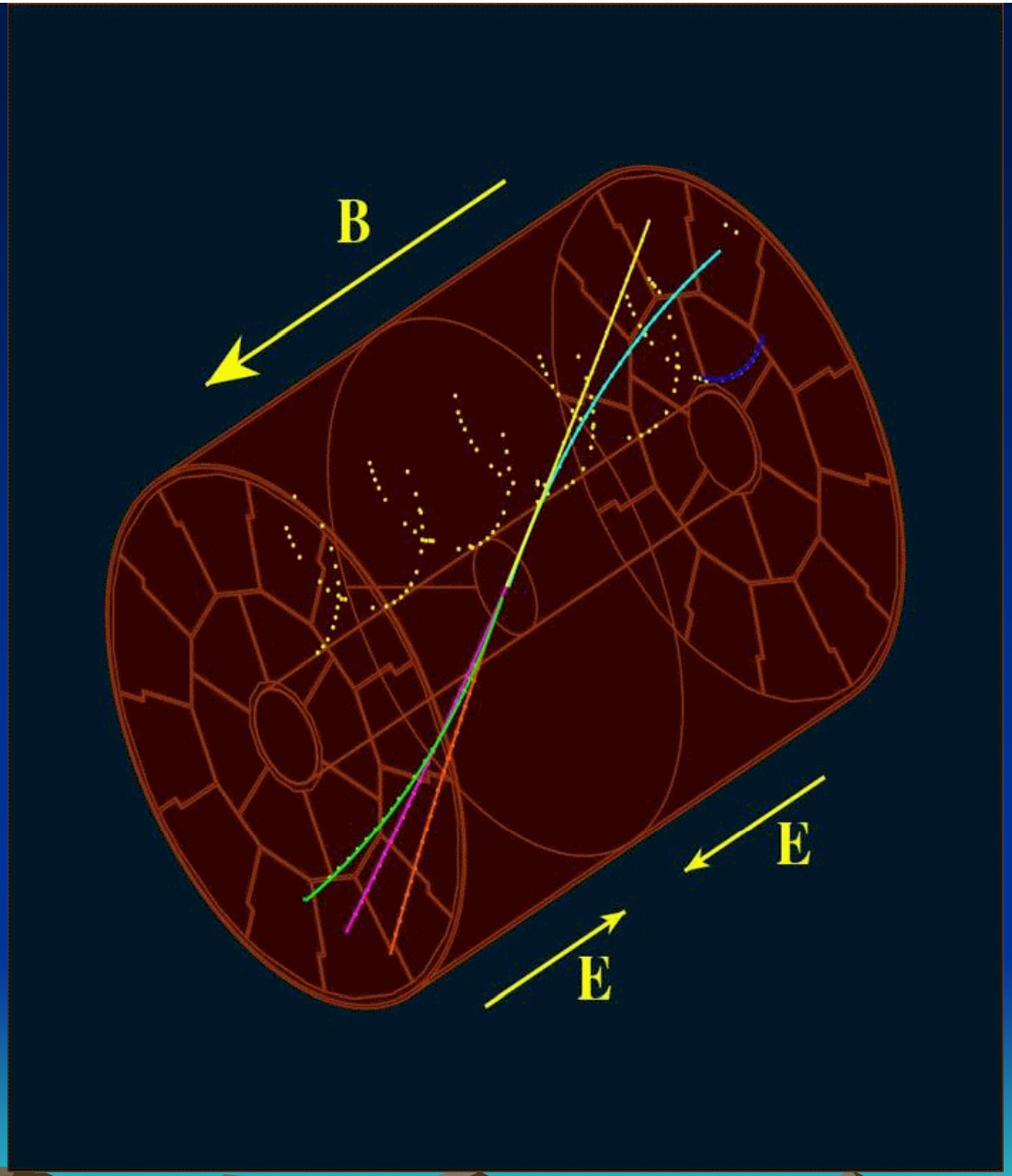


3-rows (Akira)



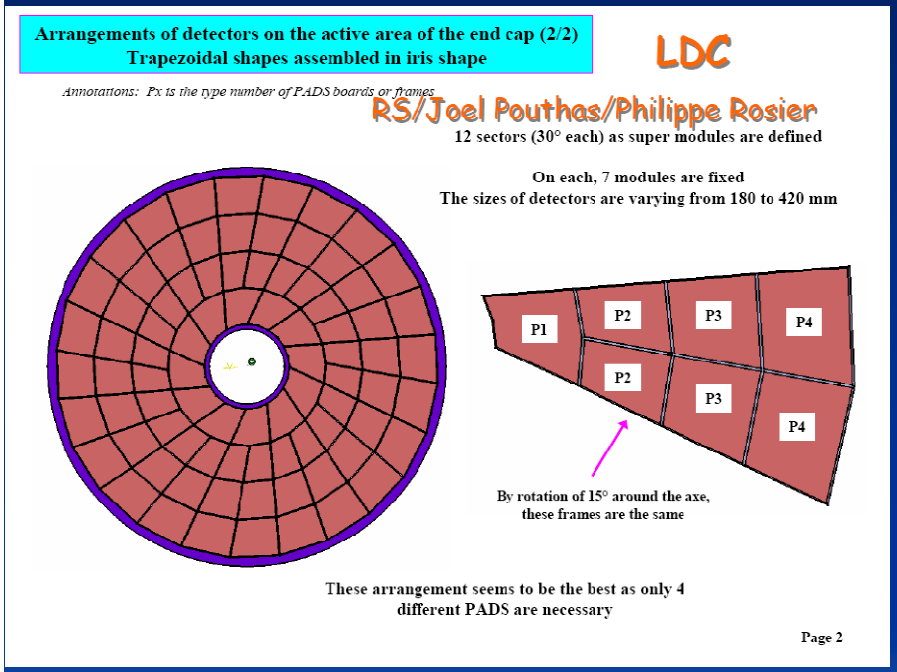
4-rows (Philippe)
(David,Paul,Marc,Michael)

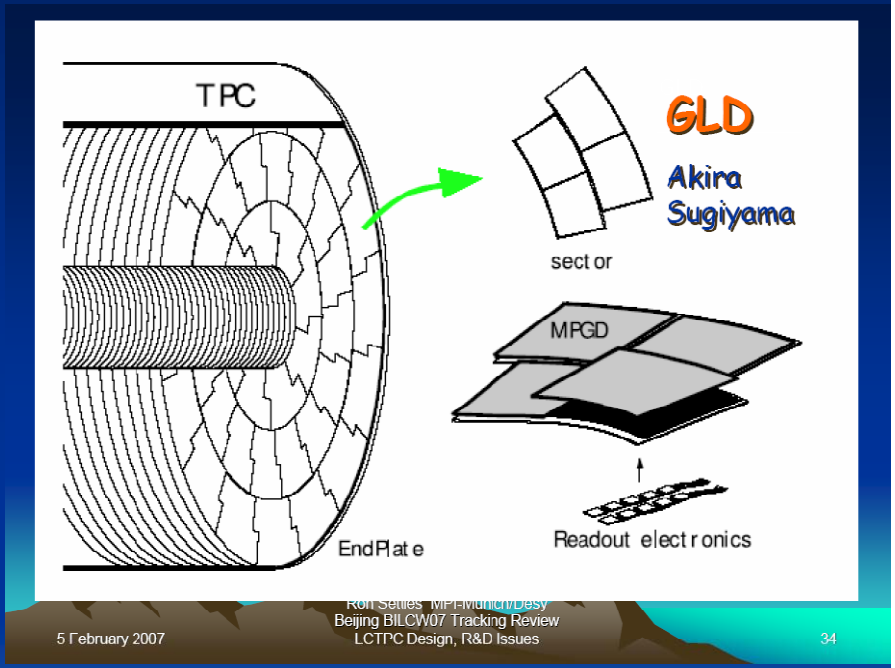



B
E
E

LCTPC engineering model for LOI

- "Advanced endcap" Dan: I am in contact with him about the module layout on the endcap. Past examples:





LCTPC engineering model for LOI

- "Advanced endcap" proposal to Dan, use LP layout and scale to LCTPC size:

LP:

400cm^2

/module

LCTPC layout:

- 10 m^2 per endcap
- 0.1 m^2 (1000cm^2) per module => 100 modules per endcap
- 10 W per module

Advanced-Endcap#6a 19/01/2009
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3. Ideas from Saclay.
-David/Paul/Marc/Michael showed drawings of a four-module-layer endcap, along similar lines as designed by Akira for GLD and Dan for the LP endcap. The "resistive-anode" pad size was used (400,000 per endcap), although this doesn't really affect the module/sector-layout. RS suggested trying the three-sector-layer endcap layout similar to Akira. It is clear that reflections about pad-sizes should strive for the same electronic density everwhere, so that the thermal-household is the uniform over the whole endcap.

Drawings for an ILC-TPC endplate

D. Attié, P. Colas, M. Riallot

Endplate panels

Dimensions from 'after-Cambridge'
Panel height 336 mm
Panel width : from 278 to 454
About 6800 pads per panel