Scintillator HCAL hardware status and plans

ALCPG 2009

Albuquerque, New Mexico, October 1, 2009

Felix Sefkow
Outline

- Technological prototype overview and goals
- Mechanical structures
- Electronics integration
- Scintillator options
The task

• We have only half-way realized the integration potential of the novel SiPM technology for highly granular detectors
• What needs to be done:
  • ASICs into volume
  • DAQ in barrel endcap gap (or barrel coil gap)
  • Eliminate FE cooling with power pulsing
  • On-detector zero suppression
Goals

- Compact and hermetic mechanical structure, minimum dead spaces
- Economic solution with tight tolerances
- Read-out layer integration
- Compact interfaces
- Establish operational stability with power pulsing and on-line thresholds
Mechanical overview

- Install ECAL modules
- The middle modules you can install only with the second AHCAL half barrel in place
- ECAL cable slot
- Integration motivated by ILD, but many generic issues
real size test setup
vertical

2 short length (360 mm) absorber sub-modules mounted to a short length module

360 mm = 1 HBU length

- delivery tolerances
  flatness, thickness
- machining
  tendering, processing, handling, tolerances, costs
- sub-module mounting
  stacking and shape tolerances, module interconnection, stability
- sensitive layer installation
  handling, tolerances, vertical and horizontal layer connection, cabling and cooling routing
real size test setup vertical

360 mm sub-module

- flatness measured of 4 raw plates 3000 mm x 1500 mm Order 2 batch 1 (not roller leveled)
- order 2 batch 1 water cut to individual plate size
- flatness measured for each plate before machining
- sub-module Nr.1 mounting in horizontal position
- gap size measured in horizontal position (front)
- sub-module Nr.1 turned vertical
- gap size checked by cassette prototype

- 2 positions where the cassette does not fit into the gap
- gaps must be measured also in depth
- plate position must be measured

- flatness measured of 4 raw plates 3000 mm x 1500 mm Order 2 batch 2 (roller leveled)
- production finished of sub-module Nr.2
- mounting started
real size test setup
horizontal

4 full length (2160 mm)
absorber plates mounted to
a fraction of a sub-module

2160 mm = 6 HBU
outer position = broadest plates
(~ 1300 mm)

• delivery tolerances
  flatness, thickness
• machining
  tendering, processing, handling,
tolerances, costs
• sub-module mounting
  stacking and shape tolerances,
module interconnection, stability
• sensitive layer installation
  handling, tolerances, vertical and
horizontal layer connection, cabling
and cooling routing
real size test setup
horizontal

2160 mm sub-module
plates layer 43 to 46

- flatness measured from 4 raw plates 2500 mm x 1500 mm
- Order 1 batch 1 (not roller leveled)
- order 1 batch 1 water cut to individual size
- plate flatness measured
- roller leveling done
- plate flatness measured
- horizontal mounted
plate measurement

measurement of flatness and thickness deviation according EN10029 (steel plates t ≥15<25 mm

- flatness class N, steel group H
  - L(1000): max 10mm
  - L(2000): max 13mm

- thickness class B
  - min: -0,3 mm
  - max: +1,6 mm
  - measured at the edges only

measurement setup

2160 mm sub-module plates before roller leveling max 8 mm deviation

2160 mm sub-module plates after roller leveling max 1 mm deviation
Roller leveling

FlatMaster from company arku

capacity: \( t \leq 50 \text{ mm} \)
flatness: \( \pm 1 \text{ mm} \)
Test beam setup V2

2 HCAL vertical test absorber structures with sensitive layers

1 ECAL JRA3 prototype
Mechanics status:

- Economic solution for achieving 1mm flatness tolerances without machining found
- Prototypes available to experimentally test whole barrel stability
- Realistic environment to address electronics integration
  - Large area
  - Multi-layer
- Scalable towards a full-size integrated test beam set-up
New ASICs: SPIROC

- Electronics is the key
- See R. Poeschl’s talk on 2nd generation ASIC family
- Power pulsing: 40 μW / channel
- Auto-trigger
- Analogue pipeline
- ADC and TDC integrated
- Shown to work with SiPM
- Digital part tested with DHCAL

➡ Major challenges
- Establish full readout and calibration chain
- On-detector zero suppression requires on-line control of thresholds
Electronics Integration

Mathias Reinecke | CALICE week Lyon | Sept. 16th – 18th, 2009 | Page 16

Connectors:
- Signal Power SPIROC2
- USB / DAQ Flexleads

2 setups available
- DIF FPGA
- CALIB
- ASCR Prague
- Flexleads

CALIB (fibres); ASCR Prague

36 cm
CALIB and POWER Modules

CALIB module: 11 x 10 cm²

POWER module: 12.5 x 11 cm²

> 4 Modules of both types finished, in operation.
> First tests successful.

Sizes and heights: To be adapted to ILC mechanics later.
About 80 connection cycles up to now - still ok.

Compensate HBU misalignments in distance.

Fulfill AHCAL height requirements.

Tests ok concerning:
- Signal allocation
- Signal quality
- Resistance for power
Reflector Foil Assembly

HBU backside

Reflector Foil (assembled in 4 steps)
Reflector Foil Assembly

2.5 mm

Alignment pin

SiPM pins

LED

Alignment ‘Reflector Foil – HBU’
Assembled tiles ‘just before soldering’.
Commissioning – Signal Chain for LED operation

Concept: December 2007

Mathias Reinecke | CALICE week Lyon | Sept. 16th – 18th, 2009 | Page 22
Commissioning (status last Friday)

SPIROC2 output: LEDs firing, 3 events (triggers), 18 tiles assembled

Hit Bit (internal channel trigger)
The Next Generation

Cassette (=slab)

HBU

SPIROC

Sector Connecting Plate

Central Interface Board with DIF, CALIB and POWER

Not in scale!!

Mathias Reinecke | CALICE week Lyon | Sept. 16th – 18th, 2009 | Page 24
Not in scale!!
To be minimized
EUDET Tiles

12 tiles of new generation arrived from ITEP

Tiles can be cut to accommodate varying layer width without affecting PCB grid
Electronics status and plans:

- Readout chain established with LEDs
- First base unit ready for beam test
- DAQ preparations underway (still USB based)
- Will adapt EUDET scheme following DHCAL commissioning

- 2010: Full slab (6 HBUs) tests within horizontal absorber structure
  - Requires new HBU layout with SPIROC-2
- 2011: equip em. shower size volume (12 layers, single HBU) for electron beam tests
  - Requires redesign of layer end interfaces
- Extension to hadronic volume possible if funded
Other coupling schemes

- Surface-mounted MPPCs
- Scintillator cells with dimple to compensate non-uniformity
  - See NIM paper by NIU group and D. Chakraborty’s talk

- Strips a la Sci ECAL

- New idea from MPI group
  - Dimple for direct coupling from the side

All require no or minimal modification to electronics board.
CLIC issues

- Density: jet energy performance at high energy limited by leakage ➔ study denser absorber material: tungsten
  - Test G4 simulation including neutron timing
  - Particle flow with different $\lambda / X_0$ texture
  - Even more aggressive integration demands
  - ➔ see talk by C.Grefe for further discussion

- Time stamping
  - SPIROC TDC provides $O(\text{ns})$ resolution
  - Scintillators and sensors to be optimized
Large time-walk at small charges => Problematic in calibration mode

Results consistent with Orsay
Summary

• After end of physics prototype beam tests, integration issues move into focus

• Technological prototype components are available - mostly

• Put them together and make system work - exciting commissioning phase just started

• Staged prototype roadmap

• High energy issues to be tackled next