ÉCOLE POLYTECHNIQUE

Status of the Data Concentrator Card (DCC)

Vincent Boudry
Antoine Matthieu
Franck Gastaldi

31 March 2009
DESY

ÉCOLE POLYTECHNIQUE

Goal of DCC (reminder)

- Main specification:

Reduce the number of LDA and ODR for the DHCAL & optimise the data flux

- Without DCC :

    3 Difs/layer (40 Layers)

    10 Difs/LDA => 12 LDA and 3 ODR

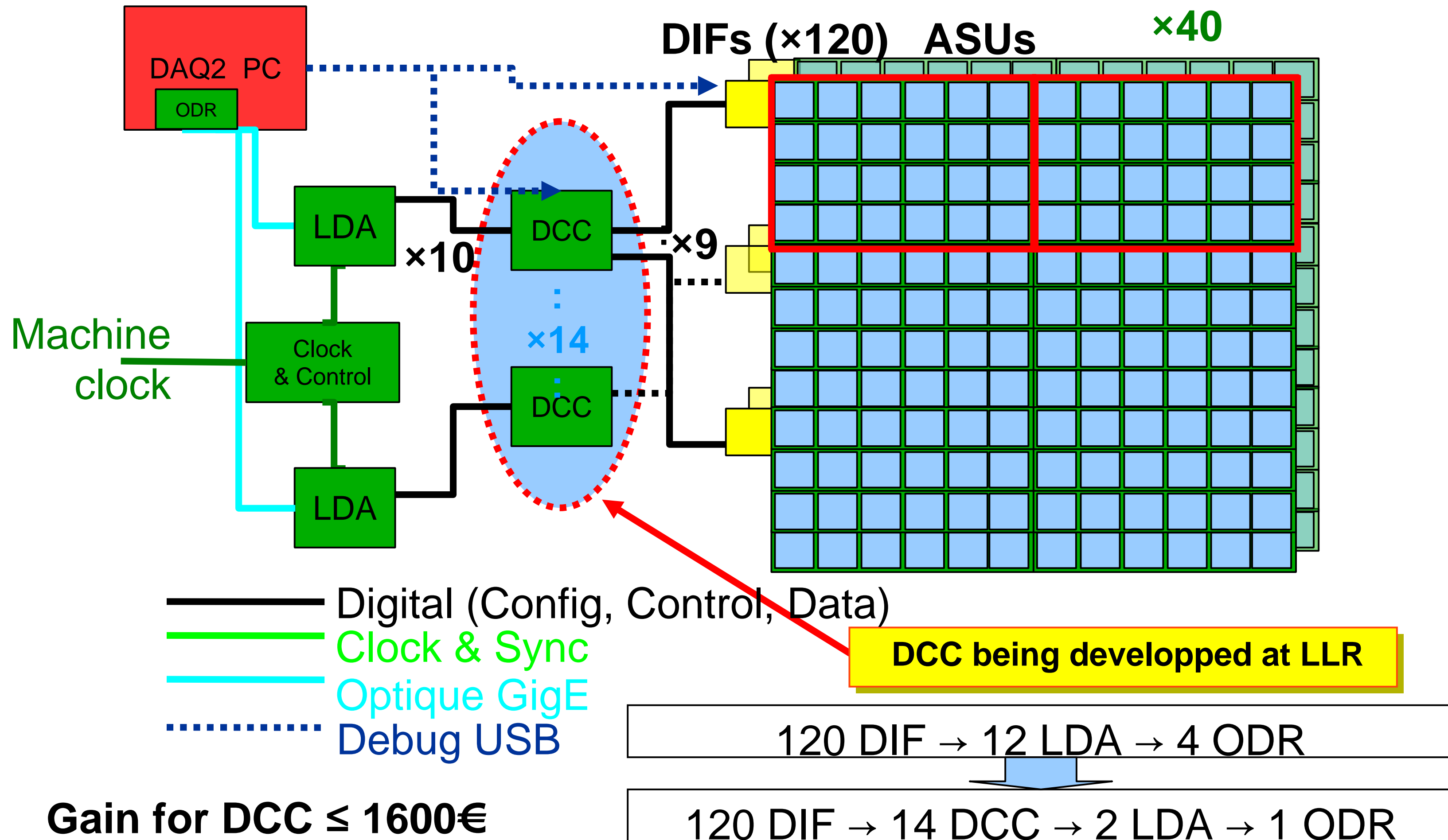
- With DCC, we have need of:
- 9 DIFs/DCC => 14 DCC => 2 LDA and 1 ODR
- Characteristics
  - Need to be transparency between DIF and LDA
  - Broadcast all fast command from LDA to all DIF
  - *<u>Need to define the slow control block transfer</u>*
  - Send the packet r/o one after the others
  - Read 9 DIFs (objective)
  - Availability of USB access
- Firmware : Reuse as far as possible existing VHDL blocks (Marc, Clement, Guillaume)
- Custom card
  - Cheaper: objective (max 1000€/card) for the production

ÉCOLE POLYTECHNIQUE

DAQ test Beam contingencies

- ASIC's in auto trig
- DHCAL Data rates in TB
  - 5 ASIC'S touched in average (max 18)/plane
  - ALL on the central DIF
- 1 evt = 160 bits
  - Readout time 1 ASIC @ 5Mb/s = 0.032 ms
  - R/O 1 plane ~0.16 ms
- 1 full HR (128 events) = 20480 bits
  - Readout time 1 full HR @5 Mb/s = 4 ms

DAQ overview

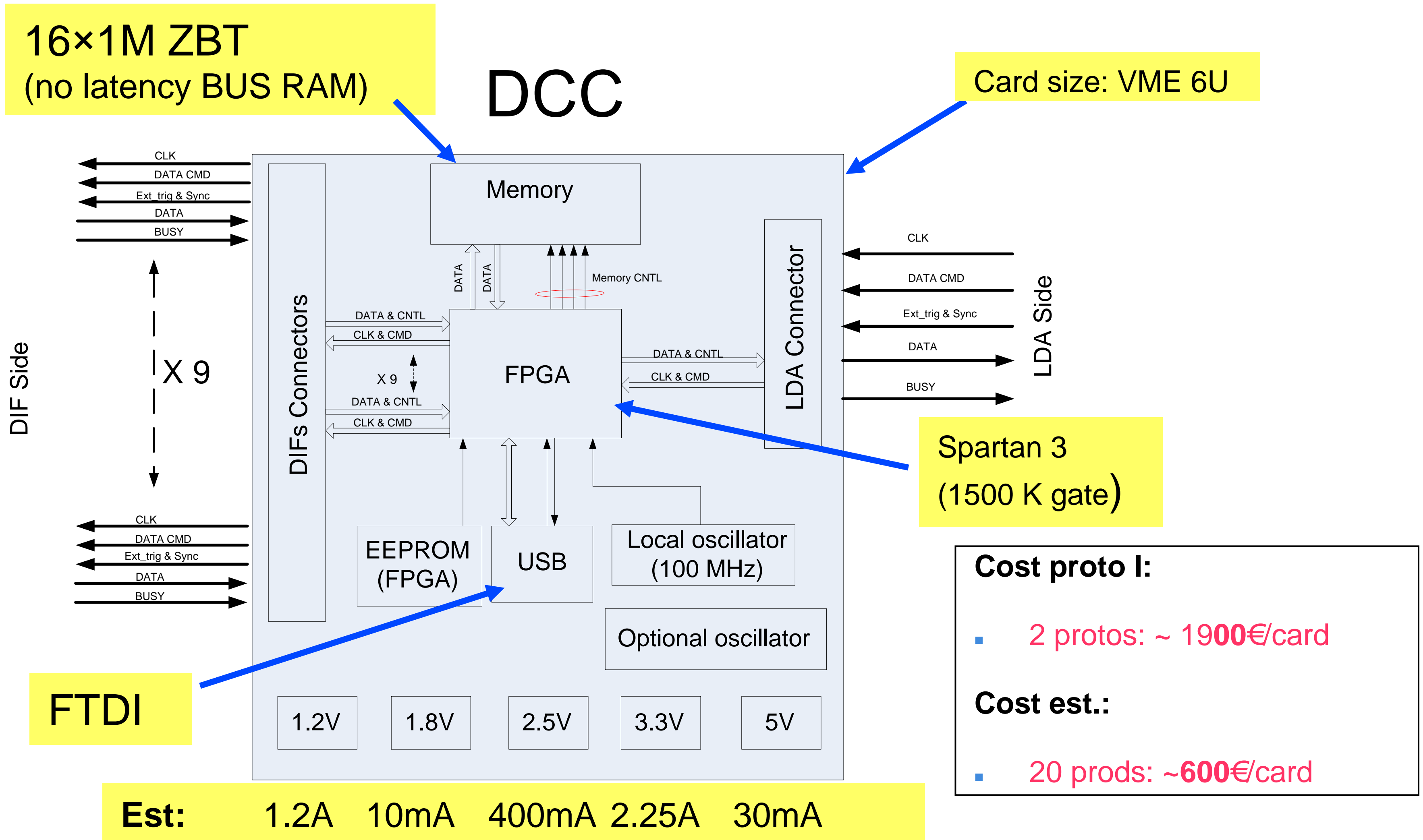


120 DIF → 12 LDA → 4 ODR

120 DIF → 14 DCC → 2 LDA → 1 ODR

Gain for DCC ≤ 1600€

Card overview



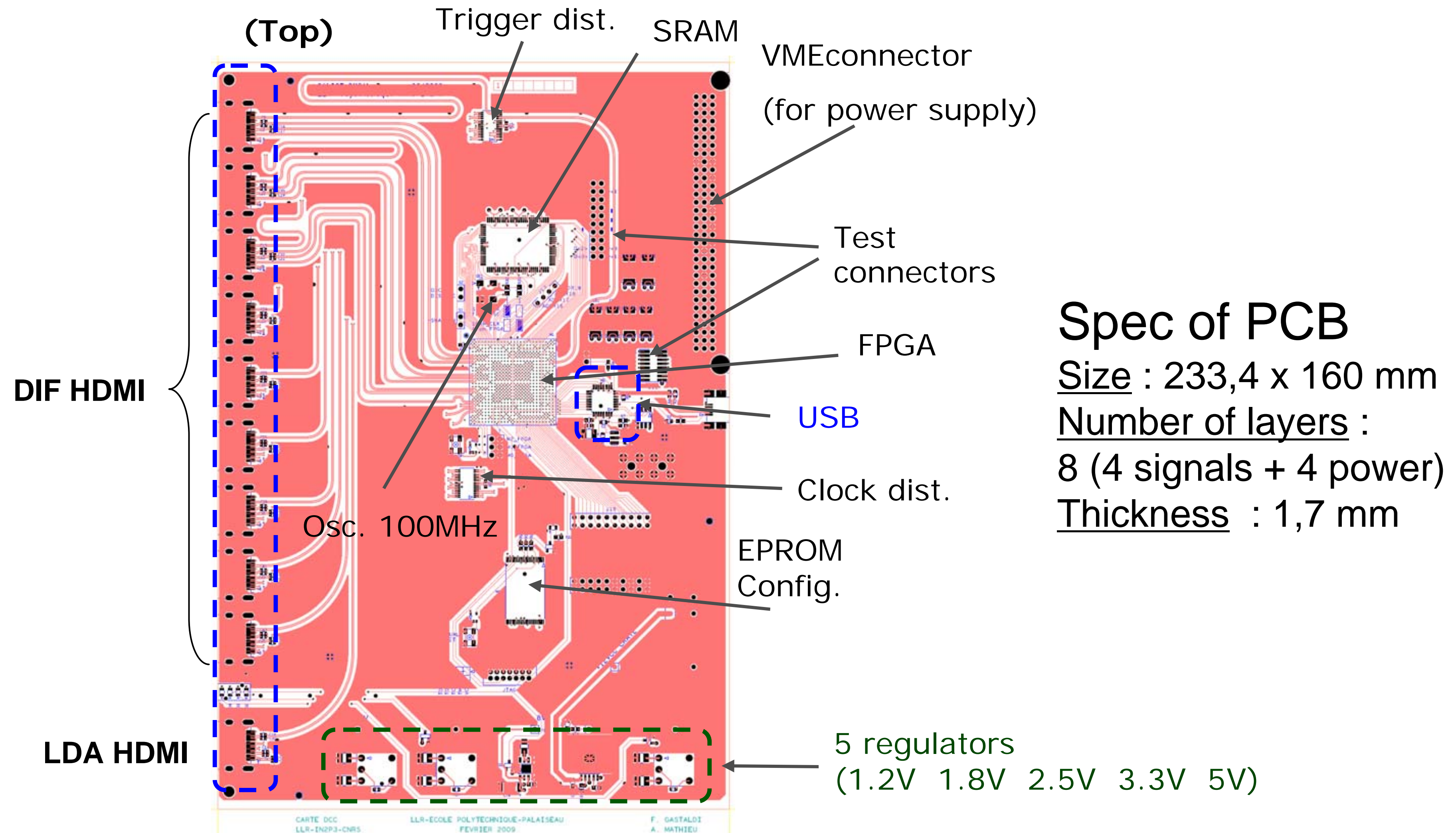
Cost proto I:

- 2 protos: ~ 19**00**€/card

Cost est.:

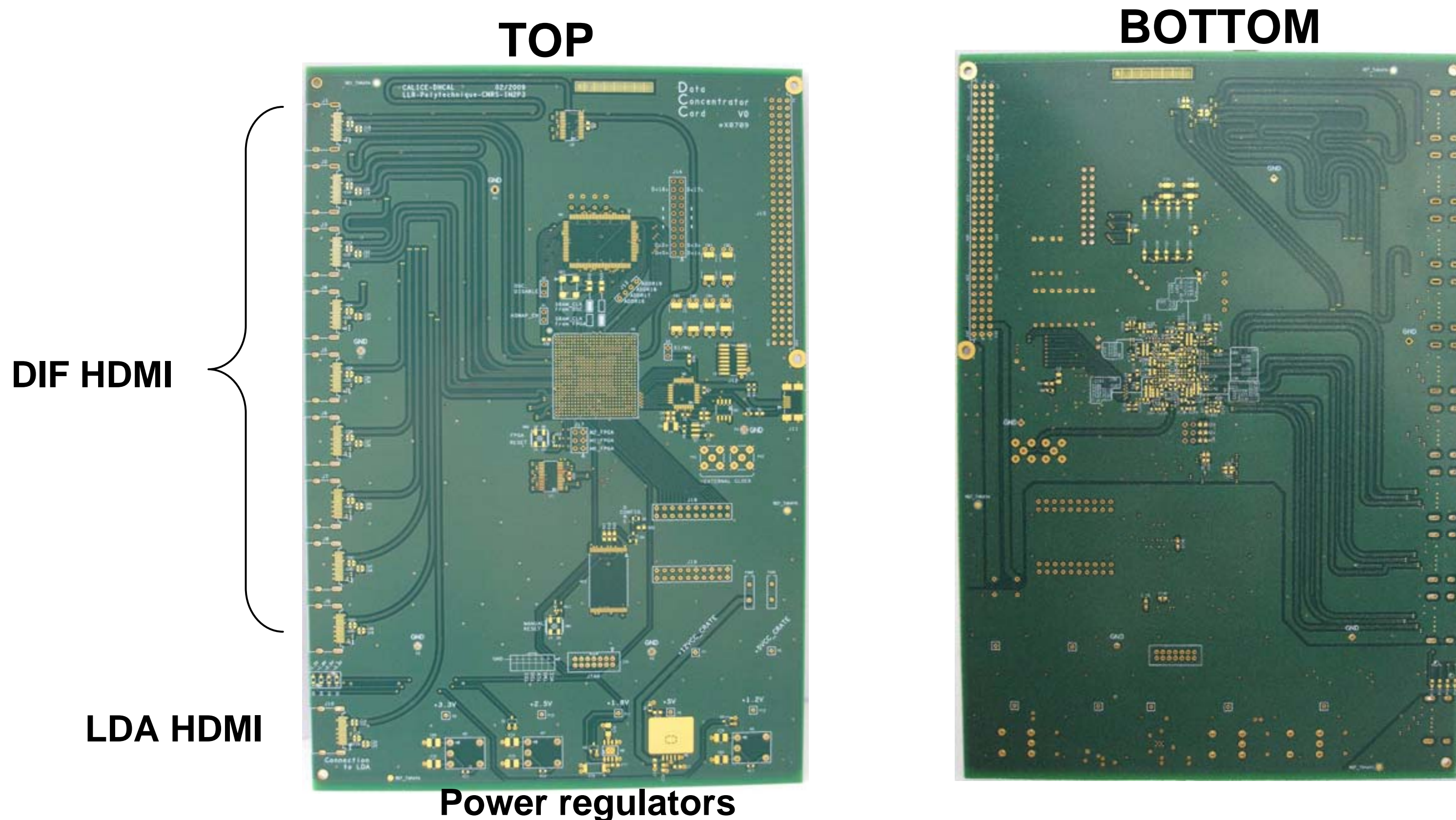
- 20 prods: ~**600**€/card

Placement overview



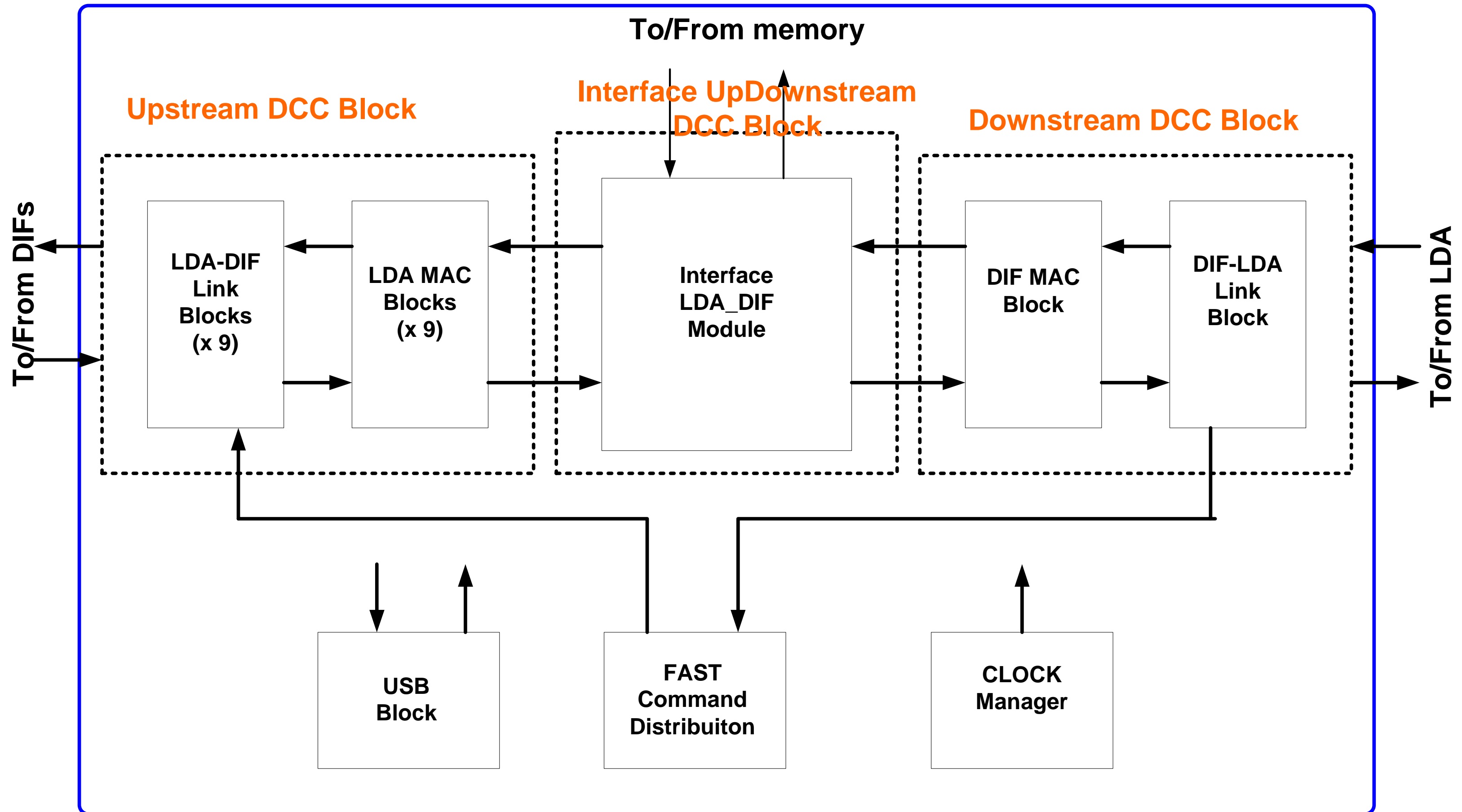
ÉCOLE POLYTECHNIQUE

PCB pictures (proto I)



We have received 2 pcb and sent to the assembling company. We think to receive the board at the end of April (due to the supply of components)

FPGA architecture by functionalities



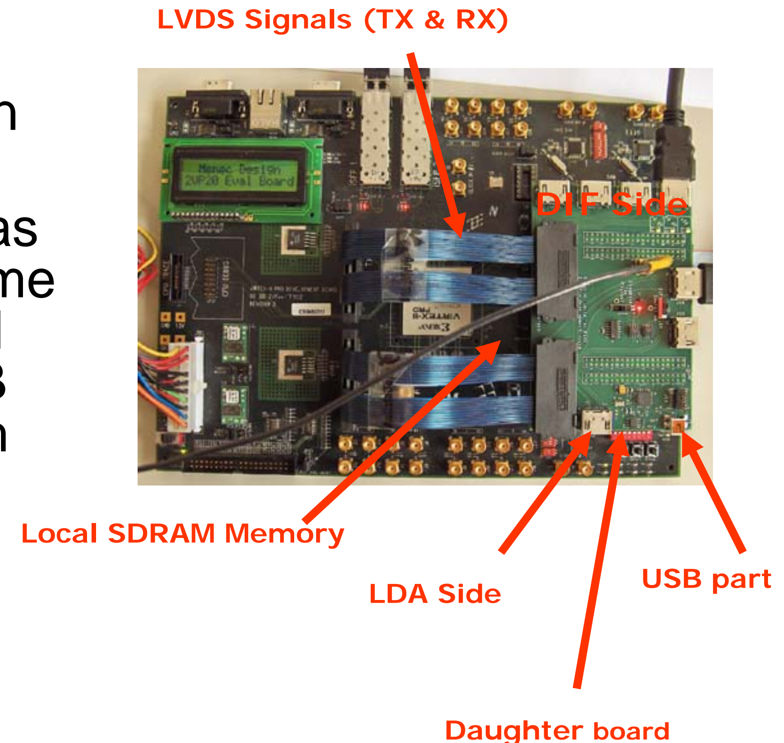
DCC Firmware

Our goal:
Try to stay on standard with DHCAL/AHCAL/ECAL
Ensure the transparencies between LDA and DIFs
Reusing as far as possible existing code: For that, Thanks to Marc ,Guillaume and Clement for share their codes

- DCC functionalities:
  - Upstream block:
    - LDA-DIF link is the same than Marc (it's the LDA module)
    - LDA Mac block is on the same idea and uses a reference design from XILINX (LocalLink FIFO)
  - Downstream block:
    - DIF-LDA link is the DIF module slightly modified (dif packet is transferred in DIF Mac block)
    - DIF Mac block with the "dif packet" is on the same idea than LDA Mac block (always base XILINX reference LocalLink FIFO)
  - **Interface Up Downstream block**:
    - Allows to select the channel to read and send the packet to the LDA. These packet must be clearly identified to allow for proper reorganization by the software
      - *Ex.: Send (packet1(dif1) – packet1(dif3) – packet2(dif1) – packet1(dif2) – packet2(dif3) …..)*
    - ***Receive the block transfer by the LDA and send it on correct DIF link. We need to put in place a strategies for this case. Add a special field in block and thus, re-route the packet on correct link***
  - USB block :
    - Used for debug and local tests or emulate a DIF or LDA. For this case, we use the memory (yet in brainstorming)
  - Fast Command Block:
    - Received by the LDA and broadcast on each DIFs.
  - Clock Manager:
    - We use the clock machine for the LDA-DIF link (LDA module) and DIF-LDA link (DIF module)
    - We use the local clock for the interface module.

Firmware testing

- We test parts of code through our XILINX evaluation card
- Some functionalities of USB have been tested
- Access to local memory on the card has been tested but not validate due to some problems with the refresh SDRAM and synchronization process between USB and read/write memory. (identified with XILINX ChipScope)



ÉCOLE POLYTECHNIQUE

Planning for next tests

We will think make the tests like this:

1 - Tests the "LDA module" alone via USB

2 - Tests the "DIF module" alone via USB

3 - Tests one channel DCC via USB

(LDA module – interface – DIF module)

4 – Tests a true DAQ channel:

(DIF ⇔ DCC ⇔ LDA ⇔ ODR)

5 - Add one DIF and make the tests

6 - And so on…

ÉCOLE POLYTECHNIQUE

Conclusion

- Proto I is under assembling
- Firmware is under integration block by block
- April-June
  - Validation and tests of vhdl code
- July
  - Depend on the results, start to think to launch the production
    - 15 days for administrative documents (CNRS)
    - 20 days for PCB fabrication
    - Around 8 weeks to order components
    - One month for cabling
  - 20 days for PCB and One month for the cabling are the delays to get a cheap price.