IN2P3

CSNSM LAL LUR IPN Orsay

Omega

FEV Status

Stéphane Callier, Dominique Cuisy, Julien Fleury

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Orsay MicroElectronics Group Associated

Schedule 2009

Omega

2009 Q1 Q2 Q3 Q4

Q1	Q2	Q3	Q4
-FEV7 design -FEV7 Layout -FEV7 prototyping -SPIROC in SKIROC mode meas. -SKIROC2 design -Schematic -Simulation	-FEV7 bonding -FEV7 debug & first test -SPIROC in SKIROC mode meas. -SKIROC2 design -Layout -Floorplaning	-PRODUCTION ROC Chips -Prototyping test bench design -Production test bench studies & design - FEV7 test	-Prototyping test of SKIROC2 -FEV7 test

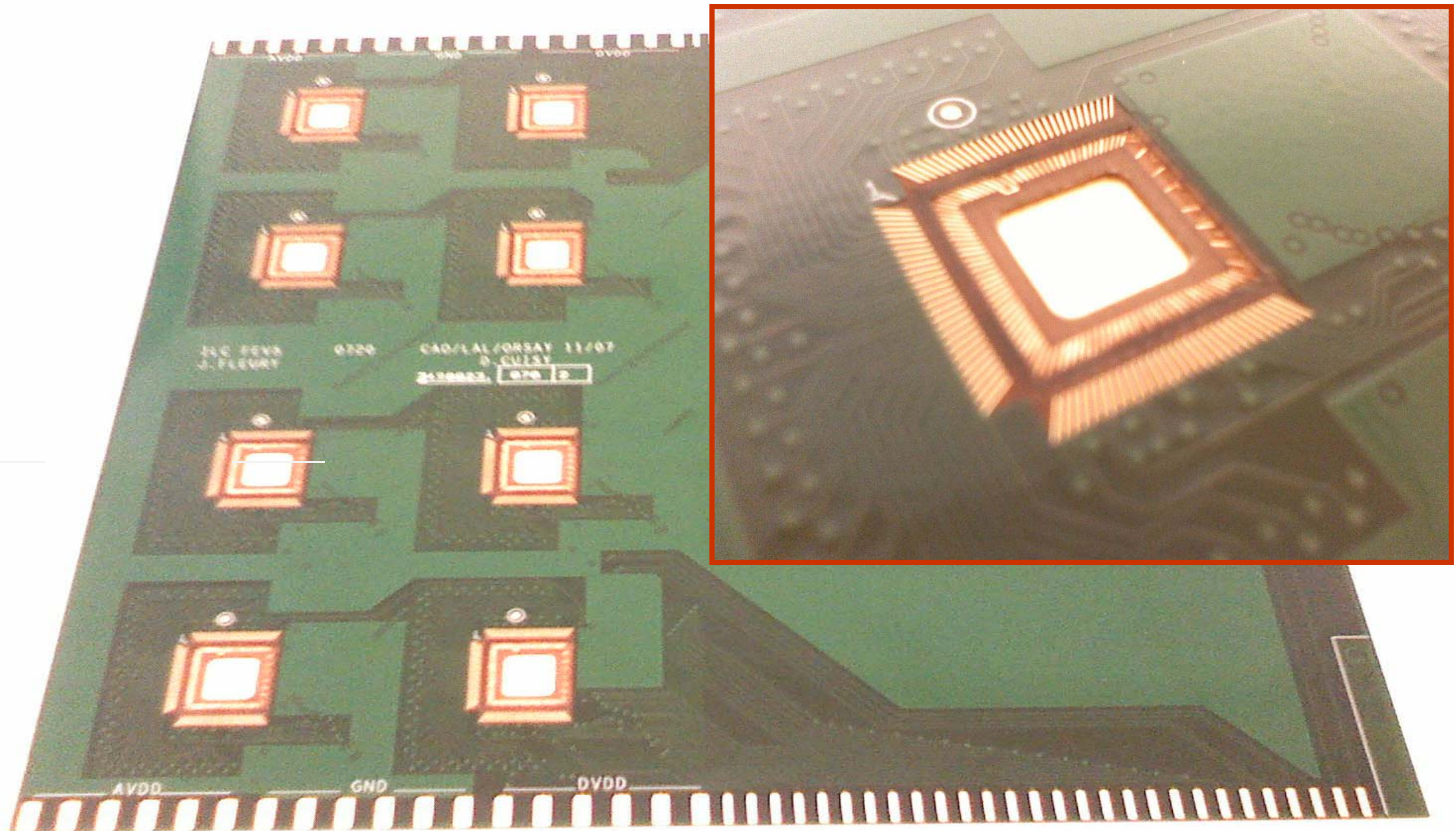
Schedule 2010

Omega

2010 Q1 Q2 Q3 Q4

Q1	Q2	Q3	Q4
-FEV8 design -FEV8 Layout -FEV8 prototyping -SKIROC2 meas. -Testbench design	-SKIROC2 production test	-SKIROC2 assembling on FEV8 -FEV8 test	-FEV8 production -FEV8 prod assembling -FEV8 prod test

Reminder : FEV5 design issues



Chip Embedding + PCB Pile-up

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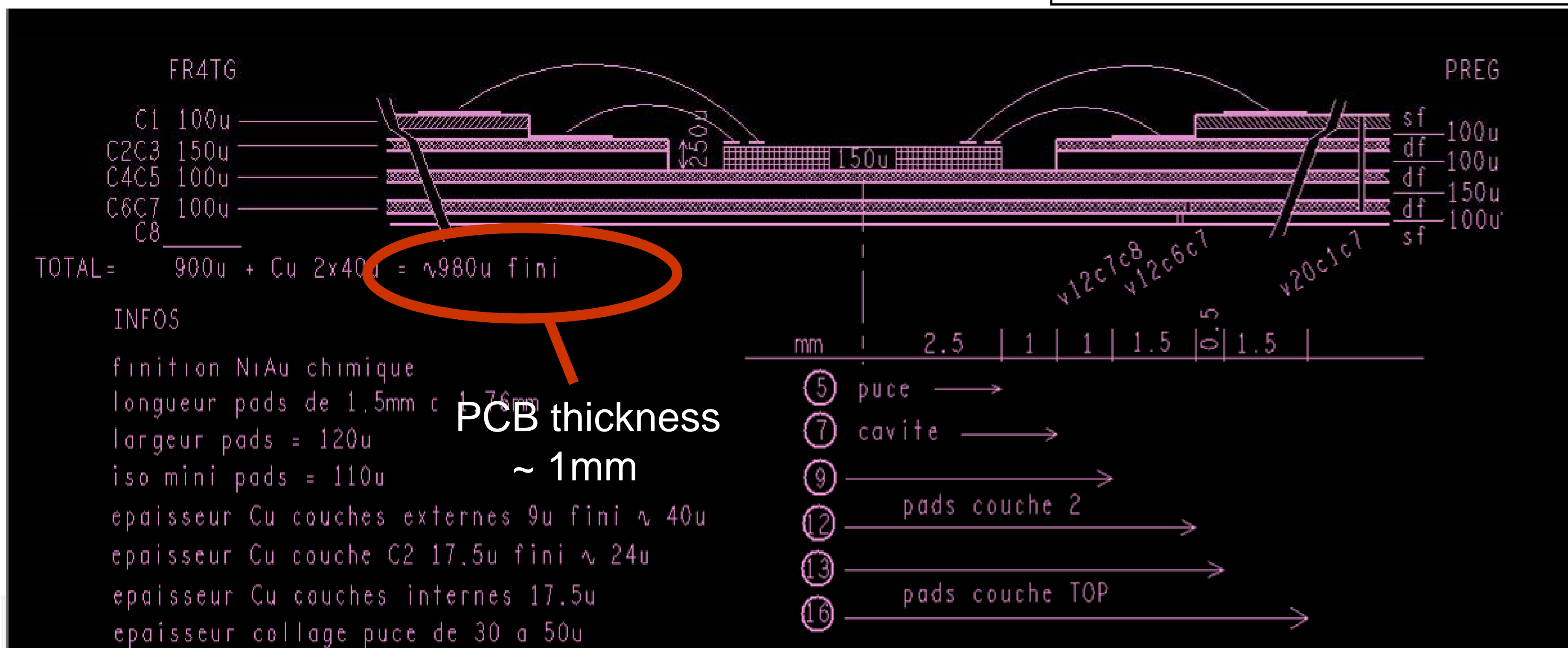
Pile-up	
TOP	GND+routing
C2	AVDD+routing
C3	AVDD+DVDD
C4	GND + horizontal routing
C5	AVDD+ vertical routing
C6	GND+pads routing
C7	GND (pads shielding)
BOT	PADS

FEV 5

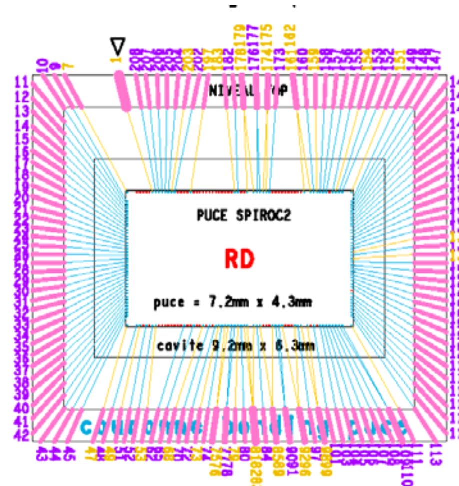
3 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C1-C7



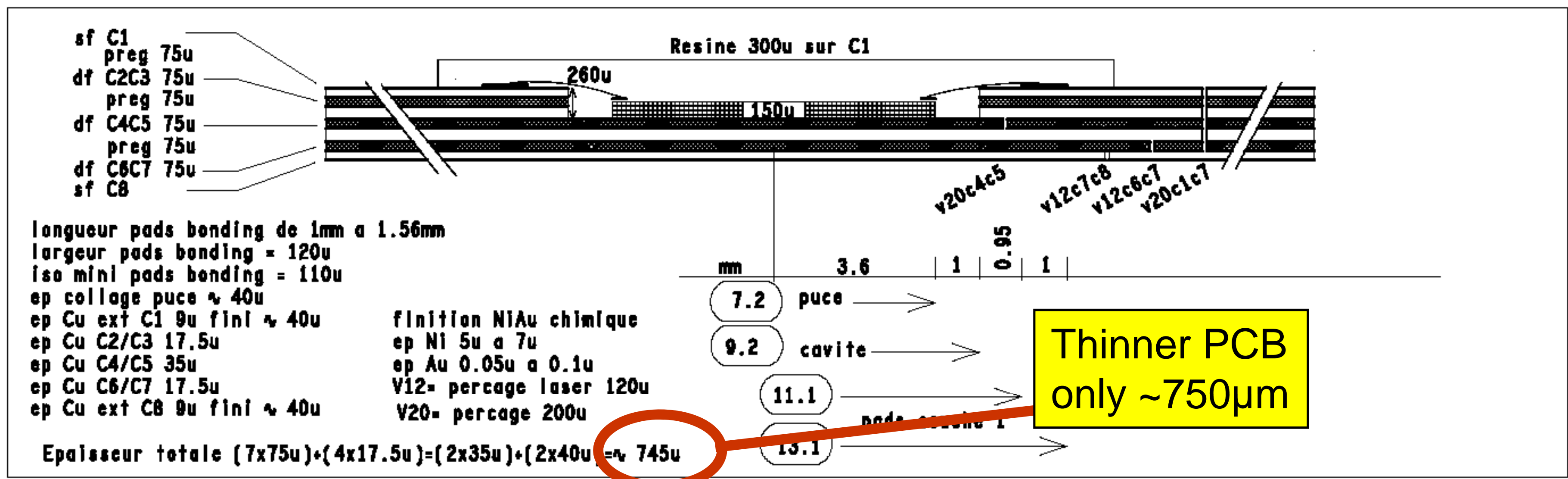
Chip Embedding + New PCB Pile-up

Pile-up	
TOP	GND + Input chip signal
C2	horizontal routing
C3	AVDD + DVDD
C4	GND + vertical routing
C5	GND (pads signal shielding)
C6	GND + pads routing
C7	GND (pads shielding)
BOT	PADS

FEV 7



4 drilling sequences :
- Laser C7-C8 120µ filled
- Laser C6-C7 120µ
- Mechanical C2-C7
- Mechanical C4-C5



FEV7 Board(s)

5 mm x 5 mm pads size
180 mm x 180 mm wafer size
-> 324 pads on a ¼ board

use of SPIROC2 (36 ch)
in SKIROC mode
-> 144 Channels (4 x 36)
will be used for Wafer
Characterization

Why such a board ?
- Due to the troubles with
FEV5 manufacturing

Purpose :
- EUDET deliverable
- Allow SLAB + DIF debug
- Allow mechanical integration

FEV7 board

2nd board !

36 channel areas

Chip on Board

Chip in Package

4 PADS merged

9 PADS merged

Wafer footprint

J.FLEURY S.CALLIER ILC FEV7_CIP 0911 CAO/LAL/ORSAY D.CUISY 0164468536

Epaisseur max CI 12/10 CI 8 couches

Conclusion

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- 2 boards to fit the schedule : work in parallel
  - Eudet deliverable : 30th June 2009
  - First EUDET full compliant PCB, using SPIROC2 in SKIROC mode.
- Halfway from expected granularity and physics prototype granularity : several pads merged for each electronics input
- Schematic using 4 SPIROC2 chip finished
- FEV8 plan to use skiroc2
  - Opportunity to have 256 ch. Wafers (5.5mm pads)
  - Wafer size : 90 x 90 mm → 16 x 16 pixels