Design of High Dynamic Range DAC for the Calibration of CALICE readout electronics

L. Gallin-Martel, D. Dzahini, F. Rarbi, O. Rossetto

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Laurent.gallin-martel@lpsc.in2p3.fr

Outline

- Choice of the DAC architecture.
- Design and test results of a 12 bit DAC.
- Design and test results of a 14 bit DAC.

DAC architecture

Switched Capacitors Array & Dynamic Element Matching

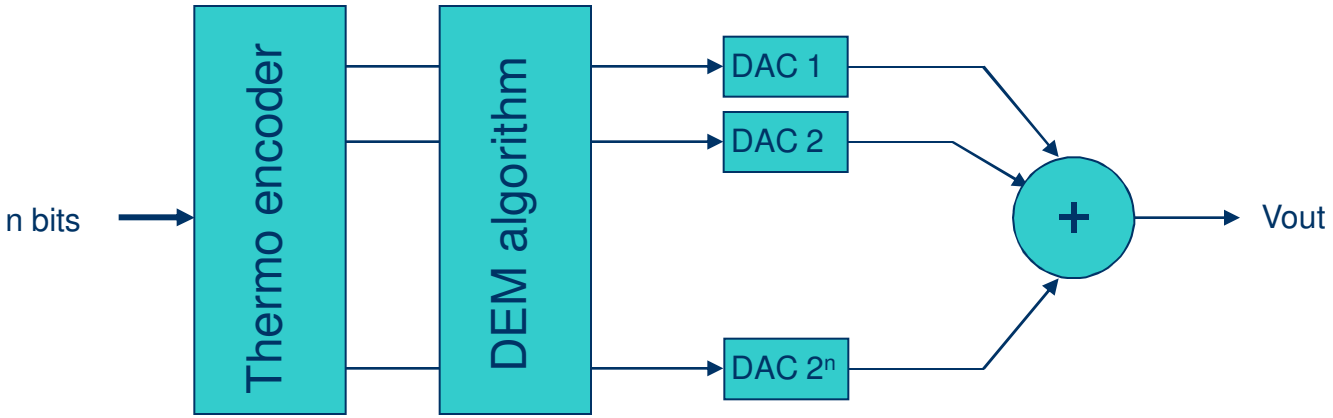
- Power consumption constraint => switched capacitors architecture.
- The linearity will limited by the matching errors of the capacitors.
- => Linearization methods have to be used.
- The **Dynamic Element Matching** (DEM) is commonly used in high resolution Sigma-Delta converters.
- The DEM **turns harmonic distortion into noise**, this noise is then reduced by the converter's low pass filter.
- The DEM can be **effective in a calibration** process if **several samples** are accumulated for each calibration point.
- The response of the chip under calibration will be given by the mean value of the resulting distribution.

DAC architecture

Dynamic Element Matching : block diagram

The DEM algorithm has to be coupled to a Thermometer DAC.

Such n bit DAC uses 2^n equally weighted converters.



Without DEM : Input code = 3 => Vout = DAC1 + DAC2 + DAC3

With DEM : the selected DACs are different for each conversion (scrambling)

=> the effects of the matching errors are spread over the whole dynamic range.

Design of a 12 bit, 5 Msps Digital to Analog Converter

DAC Modeling - High level simulations - Layout considerations - test

- Design of low power, 12 bit, 5 Msps DAC to provide a MEMS sensor with pure sinusoidal waveform.
- The sampling rate is higher than the Nyquiste rate and the DAC output will be processed by a LPF.
- => The DEM should improve the INL and the THD of the DAC.
- The DEM efficiency can be demonstrated using either a statistical approach or a spectral analysis. In both cases a large number of samples have to be accumulated.
- Electrical simulations (SPECTRE) would require several days !
- DEM algorithms can be easily described in simulation => arrays reordering.
- => Based on a model of the DAC, the DEM efficiency will be evaluated using high level simulations (Labview, Matlab,..)

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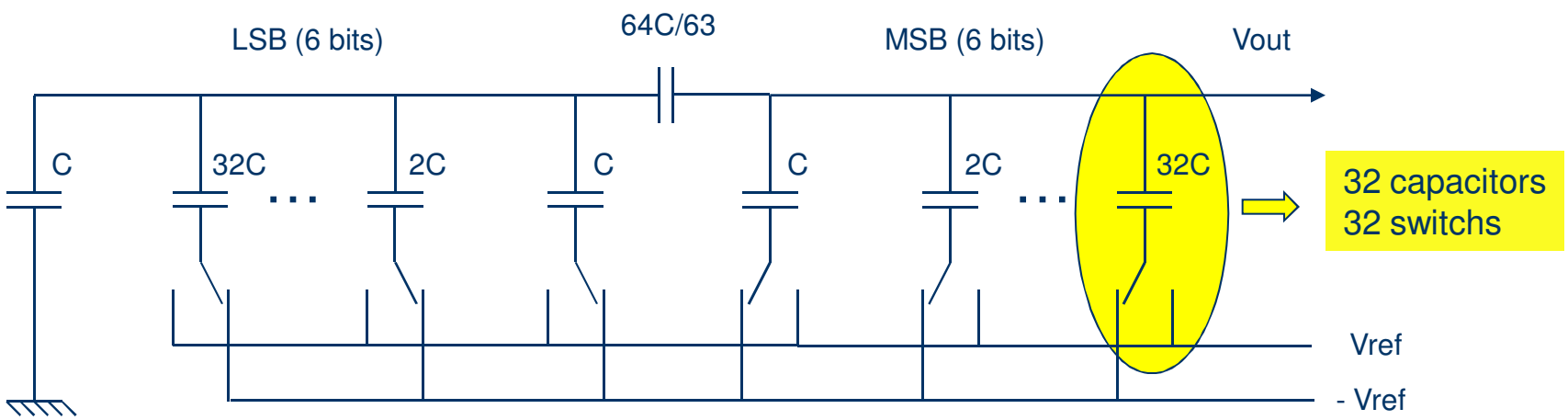
Segmented array of switched capacitors – Differential implementation



$$Vout = \frac{1}{64}\left(\frac{2l-63}{64} + 2m - 63\right)Vref$$

l = 6 bit LSB

m = 6 bit MSB

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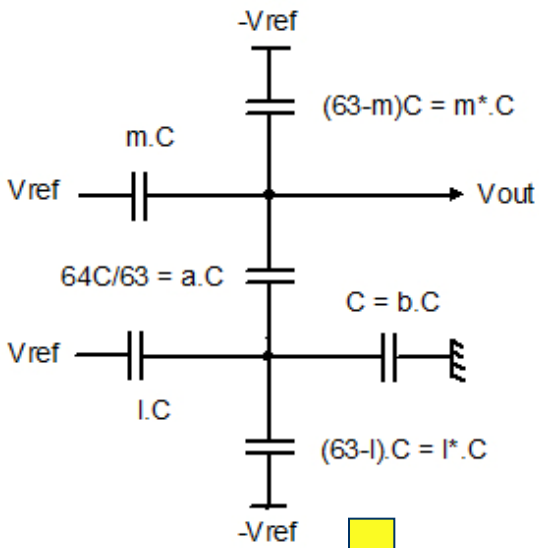
DAC modelling



Ideal capacitors

$$Vout = \frac{1}{64}\left(\frac{2l-63}{64} + 2m - 63\right)Vref$$

Capacitors with matching errors

$$Vout = \frac{B}{A}Vref = f(m,l,a,b)$$

$$A = \frac{m+m^{*}+b}{b} - \frac{b}{l+l^{*}+a+b}$$

$$B = \frac{2l-63}{l+l^{*}+a+b} + \frac{2m-63}{b}$$

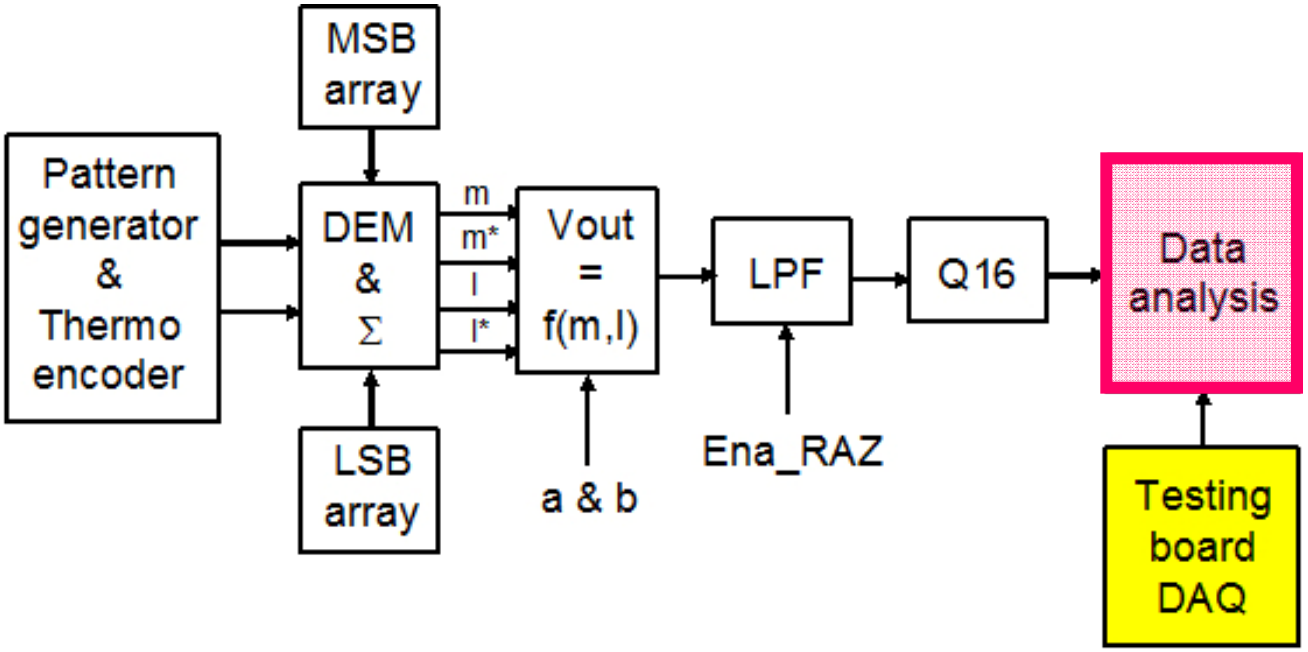
$$m = \sum_{1}^{m} C_i \qquad m^{*} = \sum_{m+1}^{63} C_i$$

Design of a 12 bit, 5 Msps Digital to Analog Converter

Simulation software

- **Labview** was used for the simulation and for the test bench control.

- Simulated and measured data are processed in the same way by the block labelled *Data Analysis*. This block computes the INL, DNL,THD, SNR, ... It also extracts the capacitors errors.



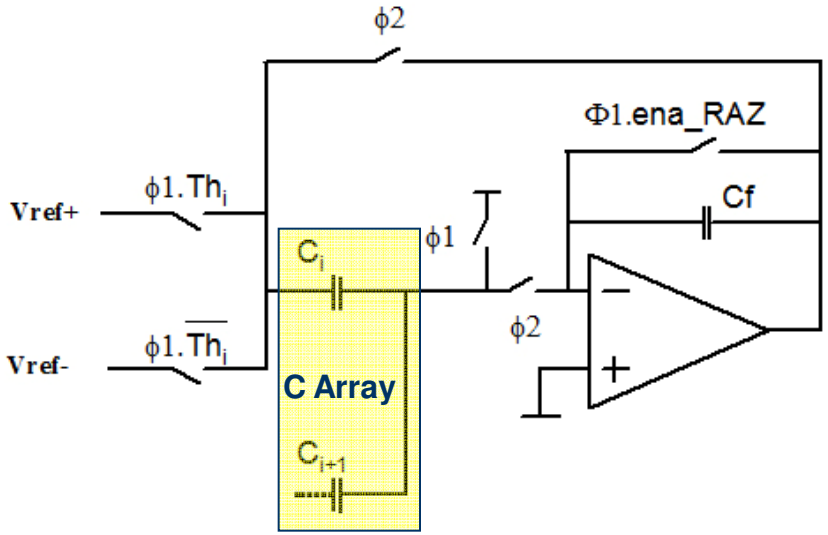
Design of a 12 bit, 5 Msps Digital to Analog Converter

Direct Charge Transfer

- $\Phi 1$: C_i capacitors are connected to Vref+ or Vref- , depending on Th_i.
  Cf can be discharged or not => **LPF if ena_RAZ=0.**

- $\Phi 2$: C_i capacitors are connected in parallel with Cf => charge sharing.

- **The amplifier does not charge Cf => low power even for large values of Cf.**



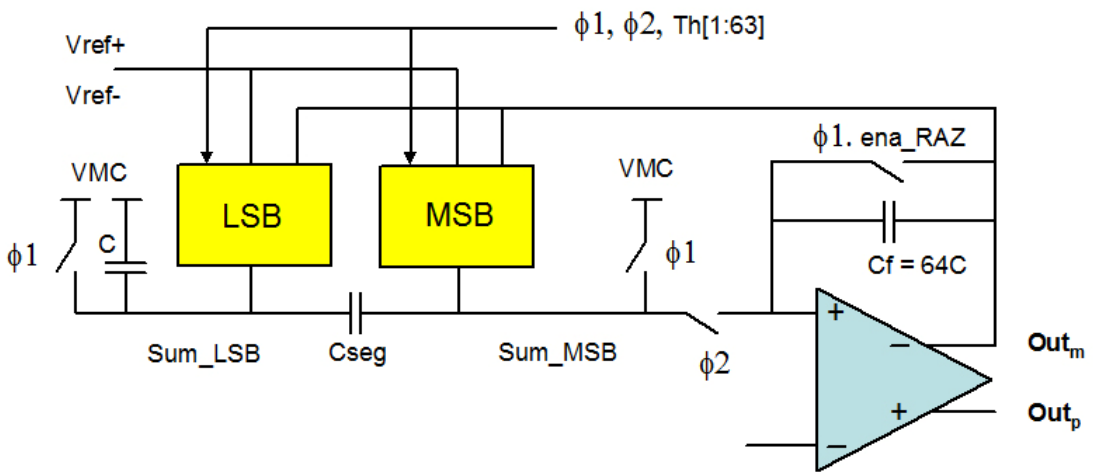
$$H(z) = \frac{1}{2 - z^{-1}}$$

$$f_{-3dB} = \frac{\ln 2}{2\pi . T_s} \approx 0.11 f_s$$

Design of a 12 bit, 5 Msps Digital to Analog Converter

Differential implementation

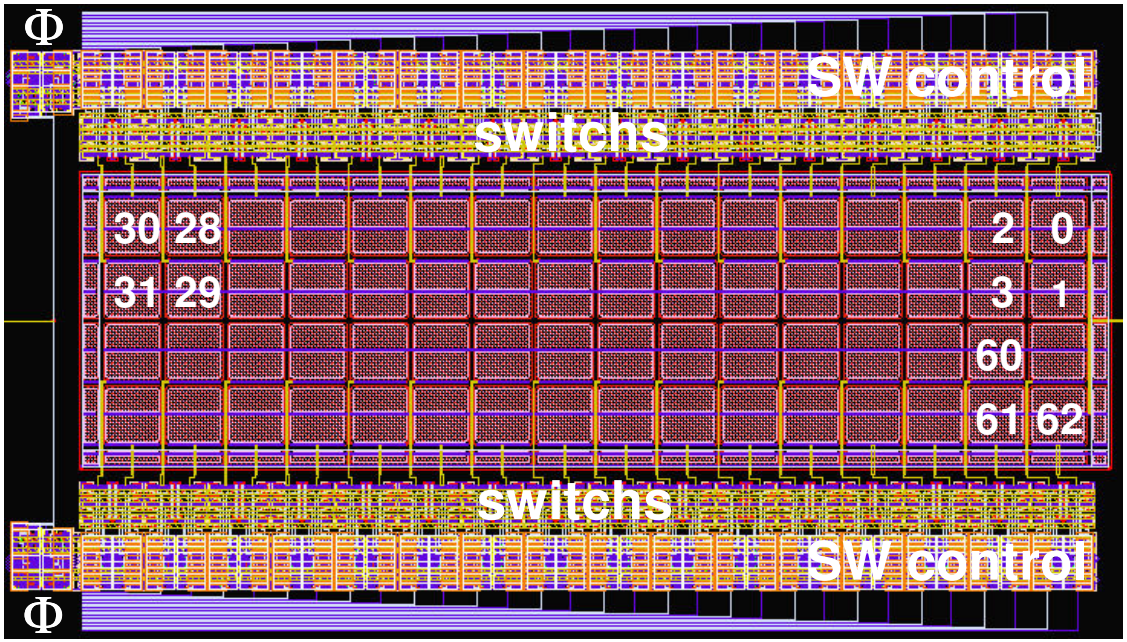
- Inherits the OTA designed at LPSC for a pipeline ADC (Dzahini, Rarbi).
- Low sensitivity to parasitic capacitors :
  - Sum_LSB : very low sensitivity on LSB side.
  - Sum_MSB : OTA 90dB open loop gain => $\Delta V=0$.
  - Parasitic capacitors in parallel with C_i => related layout considerations : matching.
- Sensitive component : Cseg, must match the MSB array mean value.



Design of a 12 bit, 5 Msps Digital to Analog Converter

Layout – 64 capacitor array : MSB array + Cseg

- 63 MSB capacitors + Cseg + dummies C_i = 500 fF => 25x25 µm^2.
  - 4x16 array.
  - Not a common centroid design.
  - Matching errors due to metallic interconnections : < 0.5 fF : 0.1% (AV_extracted view).
- 63 switchs + control logic.
- 2 clock generators.
- 500x300 µm^2



Design of a 12 bit, 5 Msps Digital to Analog Converter

Power consumption - Layout

Vdd = 3.3 V

DEM => 0.3 mW @ 5MHz

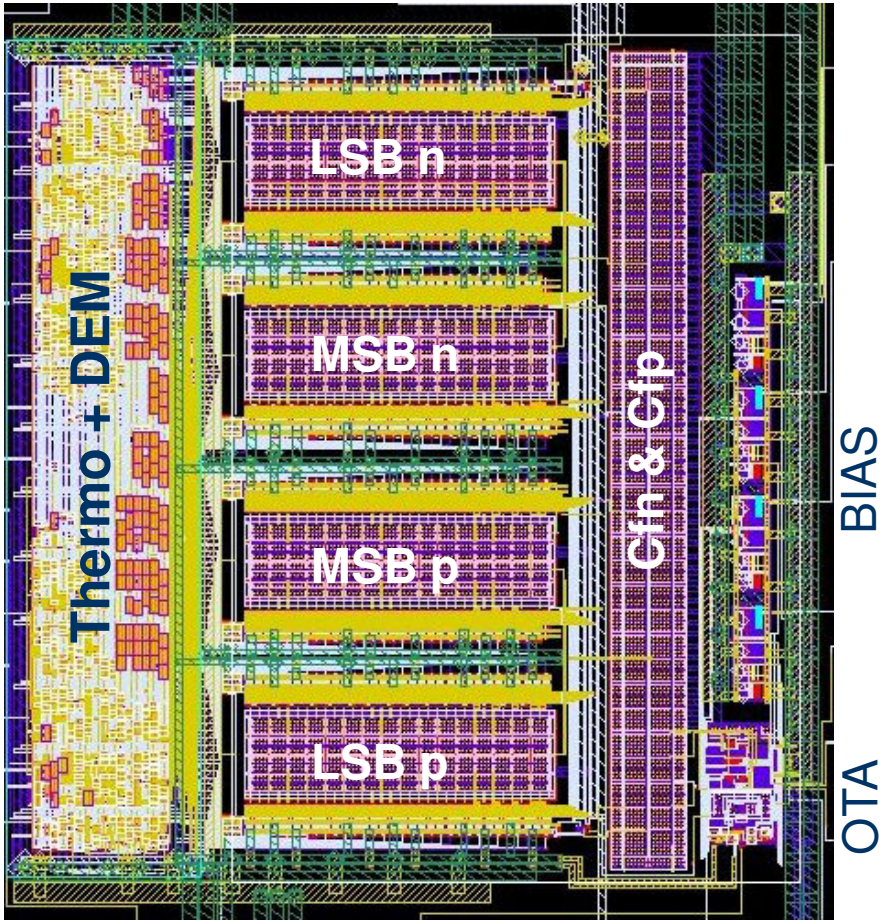
OTA => 2.2 mW

BIAS => 2.5 mW

DAC12 => 5 mW

Idle mode : < 1 µW

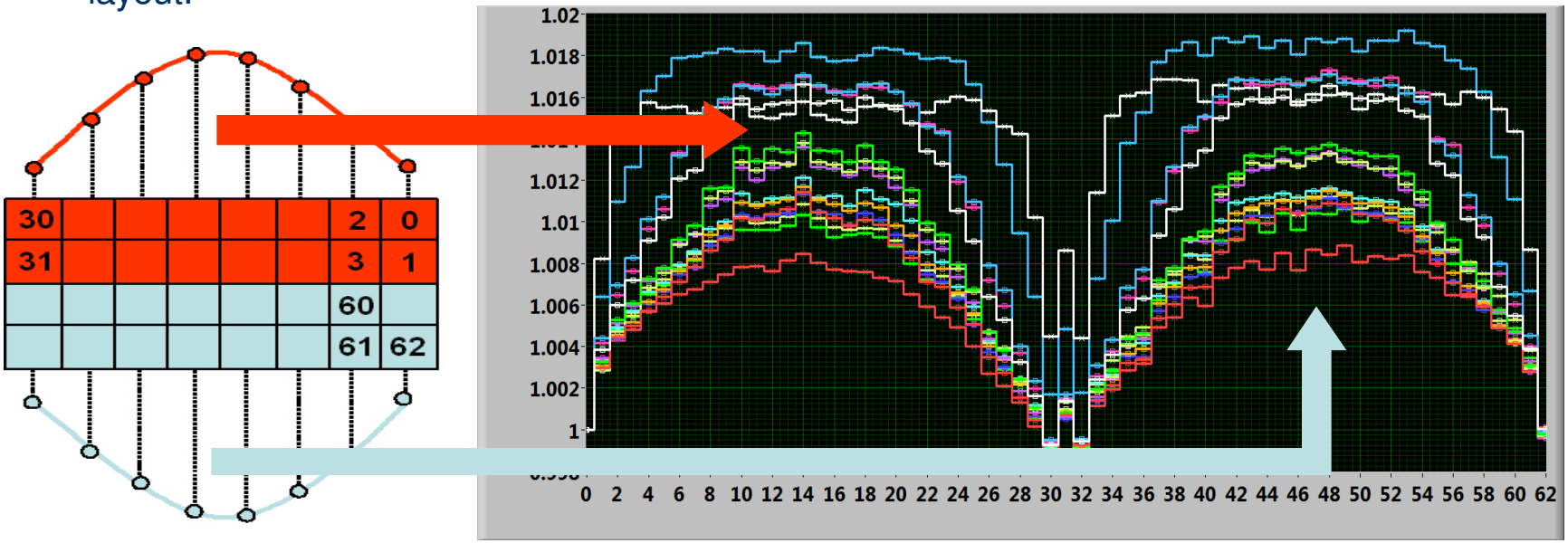
1300x1200 μm^2 = 1.6 mm^2



Design of a 12 bit, 5 Msps Digital to Analog Converter

Test results – Matching errors in a 63 capacitor array

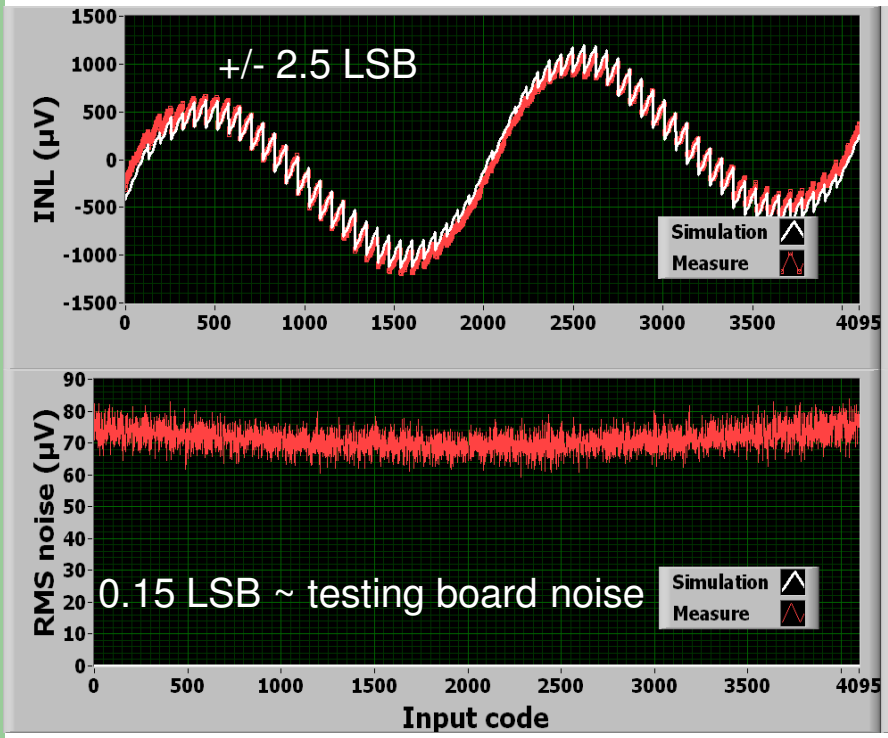
- 15 chips tested
- Systematic matching error : from 0.8% to 1.8%
- Gradient not constant over the array => effect not cancelled by a Common Centroid layout.



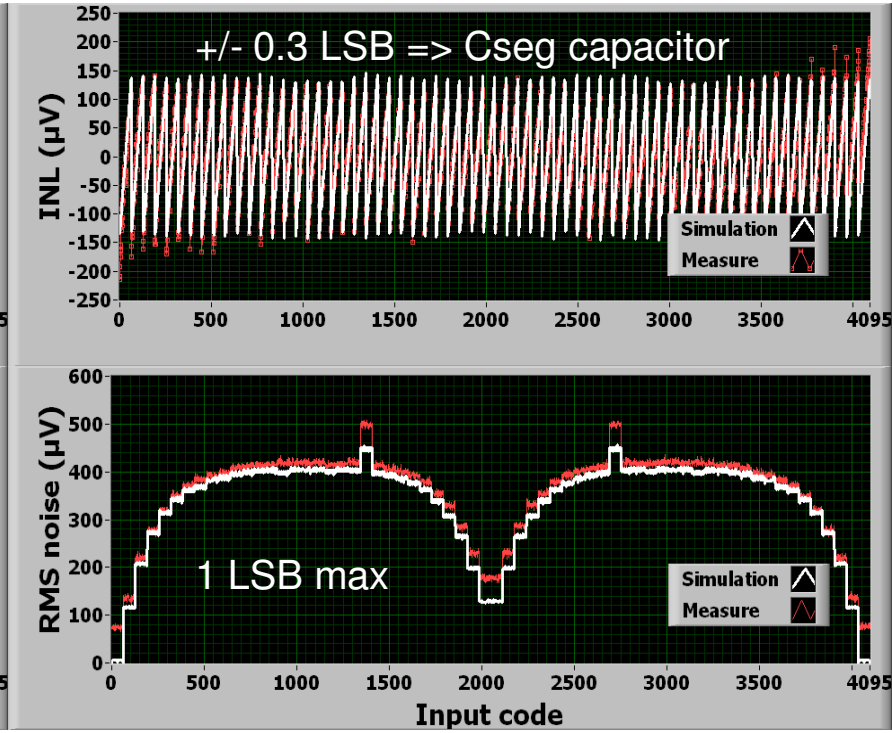
Design of a 12 bit, 5 Msps Digital to Analog Converter

High level simulation versus test results - INL and RMS noise

Without DEM



With DEM



Design of a 12 bit, 5 Msps Digital to Analog Converter

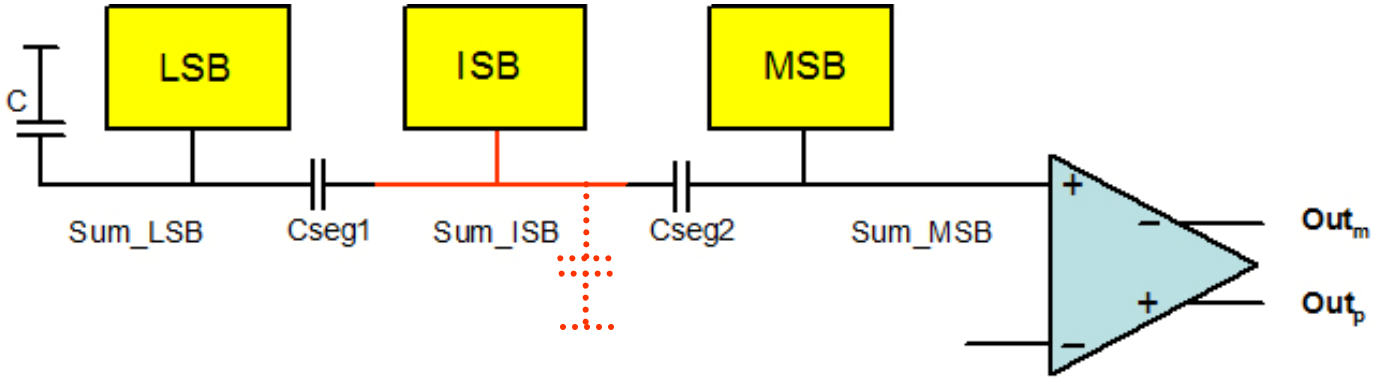
Conclusion for the 12 bit DAC

- The DAC **satisfies the constraints** of the MEMS sensor project.
  (Power consumption, Sampling rate, INL,THD, IBSNR).
- **The capacitors matching errors are larger than expected in a CMOS 0.35µ process.**
- **The DEM improves the INL by a factor of 8 (3 bits).**
- The noise induced by the DEM has to be reduced (for the ECAL FEE calibration).
- Our high level simulation is a fast and reliable tool.

Design of a 14 bit, 5 Msps Digital to Analog Converter

Capacitor arrays

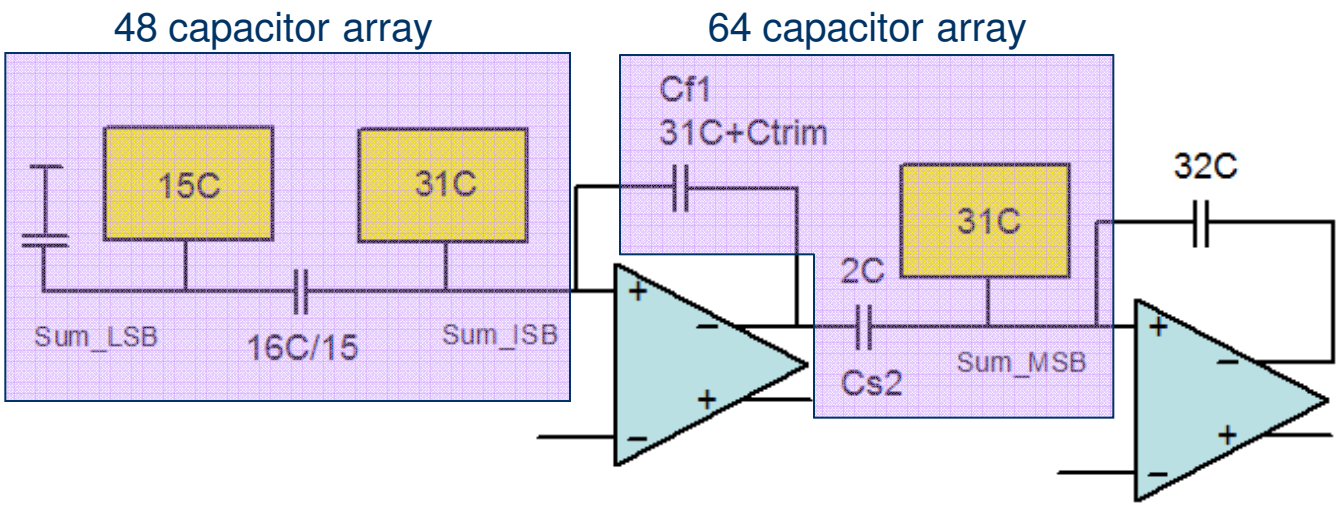
- **The experience from the 12 bit DAC helps to design a 14 bit version.**
- 3 segments to reduce the number of capacitors in each array (better matching).
- The net *Sum_ISB* is very sensitive to parasitic coupling with the bulk.
  - Metallic interconnections : 20 fF => INL=+/- 1 LSB.
- A solution : a second OTA.



Design of a 14 bit, 5 Msps Digital to Analog Converter

Block diagram

- Number of capacitors reduced compared to the 12 bit DAC (144/191).
- Very low sensitivity to parasitic capacitors.
- Cf_1, Cs_2, MSB array mean value : matching has to be better than 0.3%.
- Cf_1 : trimming capability for this first 14 bit prototype (0.1C step).



Design of a 14 bit, 5 Msps Digital to Analog Converter

Power consumption - Layout

Vdd = 3.3 V

DEM => 0.2 mW @ 5MHz

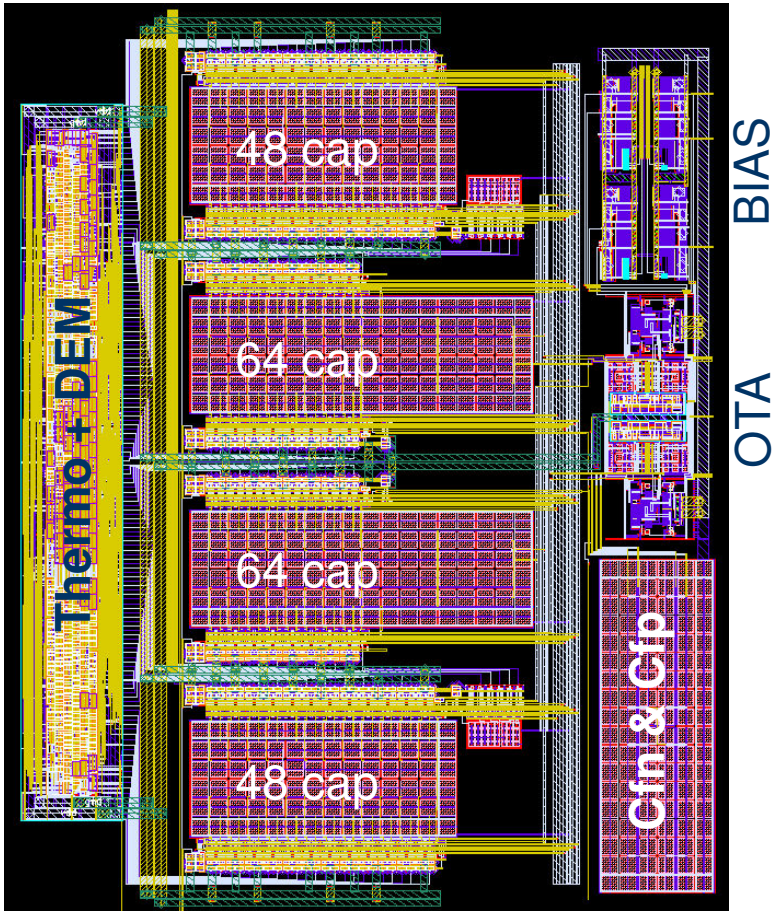
OTA => 2 x 2.2 mW

BIAS => 2.5 mW

DAC14 => 7.1 mW

Idle mode : < 1µW

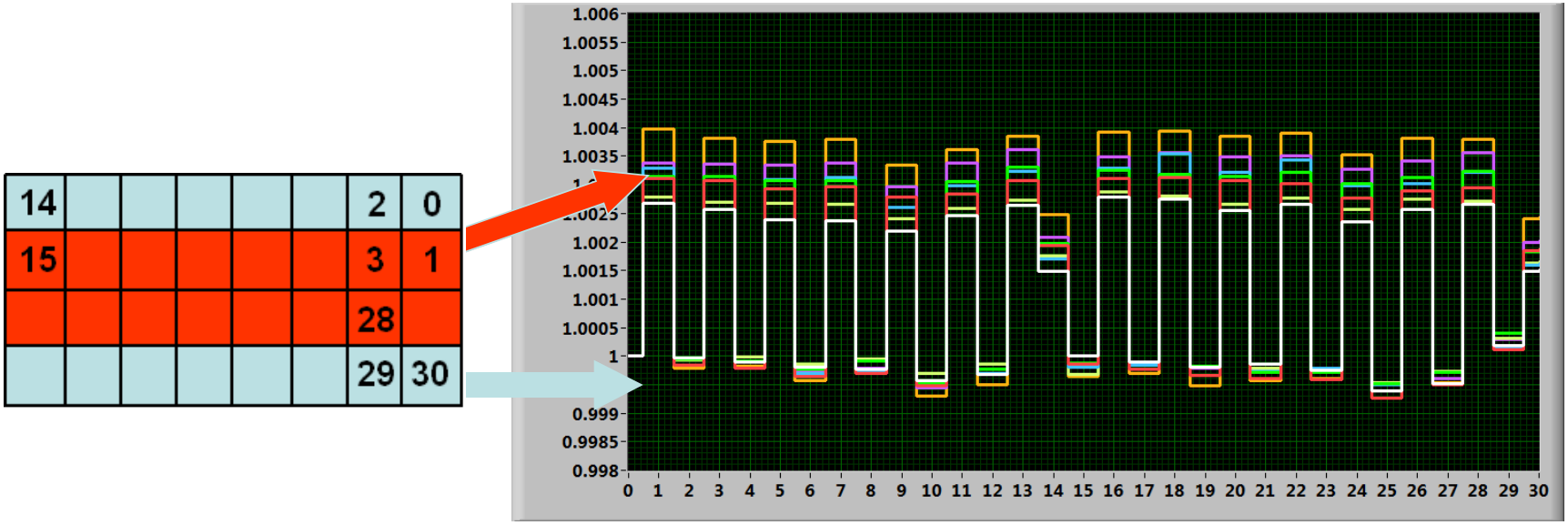
1300x1100 μm^2 = 1.4 mm^2



Design of a 14 bit, 5 Msps Digital to Analog Converter

Test results – Matching errors in a 31 capacitor array

- 9 chips tested.
- Systematic matching error : from 0.25% to 0.4%
- Mismatch due to metallic interconnections : < 0.1% (AV_extracted view).

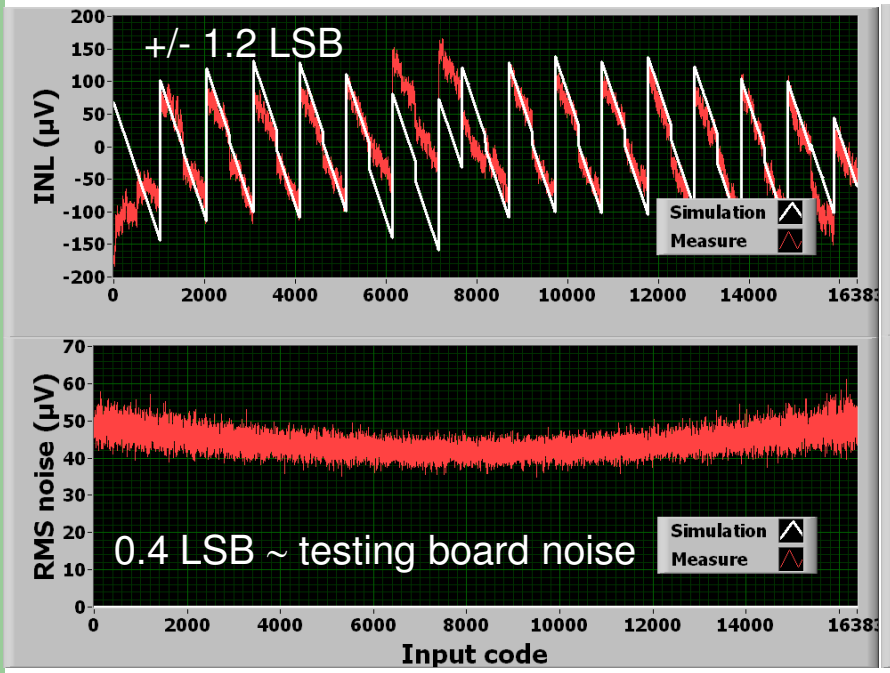


Design of a 14 bit, 5 Msps Digital to Analog Converter

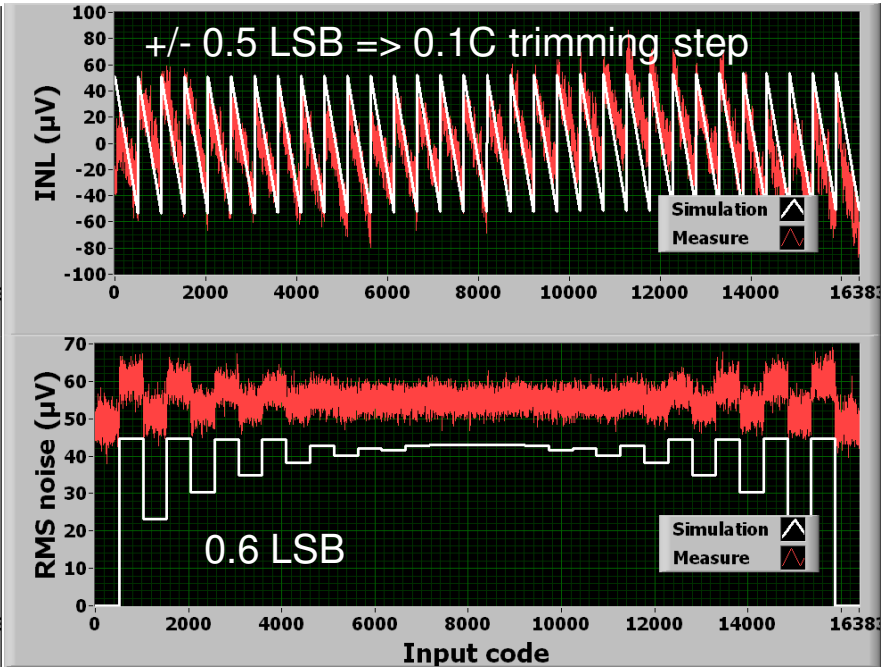
Test results – INL and RMS noise

- The DEM improves the INL by a factor of 2 (1bit) and its effect on the noise is small.

Without DEM



With DEM



Design of a 14 bit, 5 Msps Digital to Analog Converter

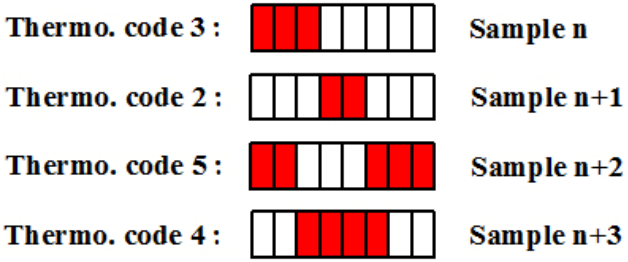
Conclusion : Process reliability – Trimming issue

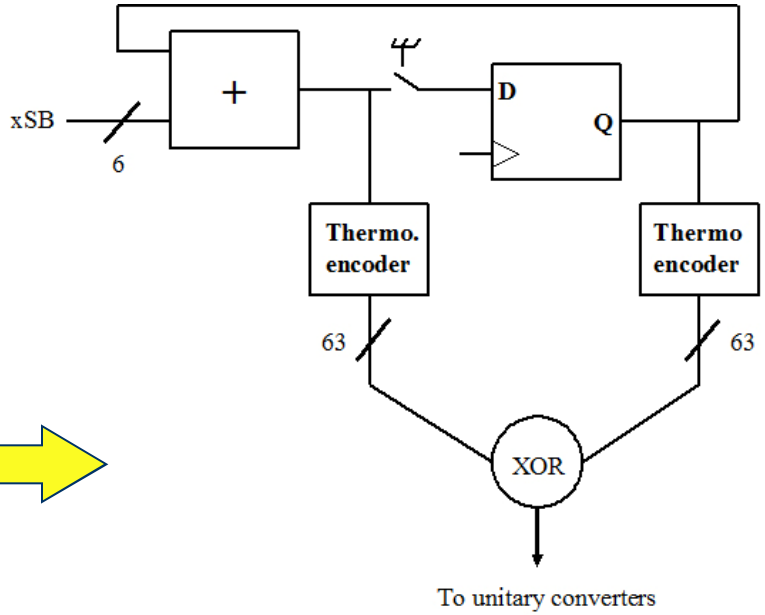
- The matching errors are much smaller in the 14 bit DAC compared to the 12 bit DAC, whereas the capacitor arrays are similar (larger dummies in the 14 bit DAC).
- The spread of the oxide thickness for the 12 bit DAC run is twice the spread for the 14 bit DAC run (and is the worst of the chips submitted by LPSC in 2008/2009 for this process).
- The optimal trimming value is the same for the 9 tested DAC. **The same value is also found with high level simulation.**
- For **this run,** the **DAC satisfies the constraints of a 14 bit design without trimming.** (since the optimal value can be predicted).
- It is not realistic to trim a sub-circuit dedicated to calibration.
- **A self calibrated 14 bit DAC will be submitted in 2010.**

Backup slide: Dynamic Element Matching

Data Weighted Averaging (DWA)

- Deterministic algorithm controlled entirely by the data sequence.
- Rotates elements with the maximum possible rate.
  - The average of the errors converges to zero quickly.
- The noise is shifted to higher frequencies.
- Easy to implement in VHDL.





Backup slide: Self calibration principle

Block diagram

- The 9 bit sub DAC has to match the MSB array mean value (5 bit sub DAC).
- The DCT mode of 5 bit sub DAC is turned in Charge Injection mode.
  - Conversion results can be accumulated in the Cf_2 capacitor (pileup).
  - The DNL is concentrated in the 511/512 transition, modulo 512.
- The output voltage error is amplified and can be easily minimized using a basic comparator.