SPIROC with SiPMs: Status of the Characterisation Measurements

Riccardo Fabbri [DESY]

Benjamin Lutz [DESY]

Wei Shen [Heidelberg]

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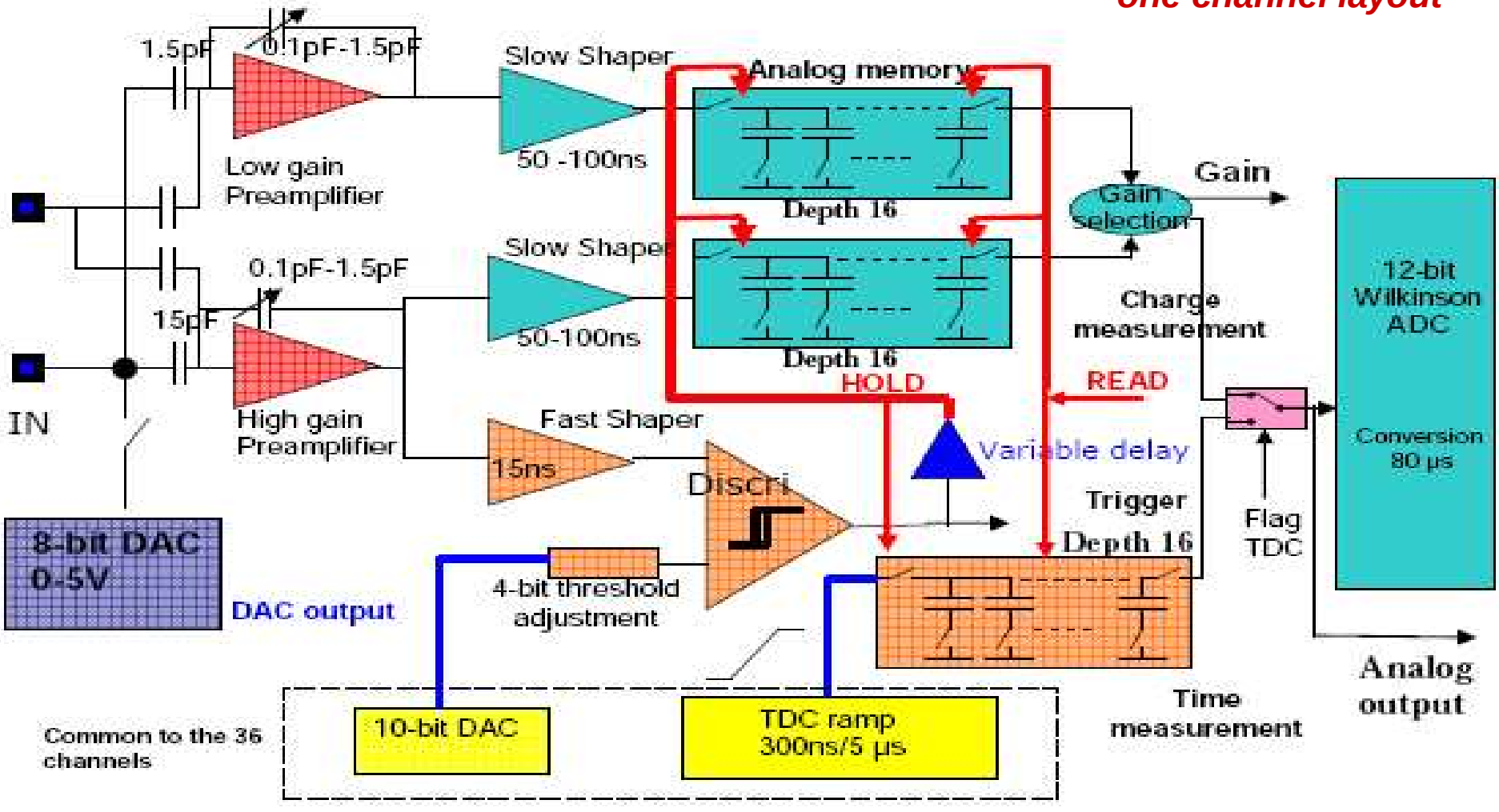
SPIROC ASIC Description and Properties

- **Dedicated front-end electronics for ILC analogue HCAL (AHCAL)**
- **Replacement of ILC-SiPM ASIC currently used in AHCAL prototype**
- **It embeds cutting edge features to fullfil ILC final requirements:**
  - **— low noise**
  - **— low power dissipation (should sit inside the detector)**
  - **— large number of readout (SiPM) channel: 38**
  - **— auto-trigger (according to preselected threshold level)**
  - **— input signals internally processed (pre-amplification, shaping, ADC)**
  - **— large dynamic range (should allow calibration & cover SiPM range)**
- **Developed by LAL/OMEGA Paris**
- **Commisioning performed (and on-going) mainly at DESY**
- **Measurements presented here concern SPIROC I version (no digital part)**

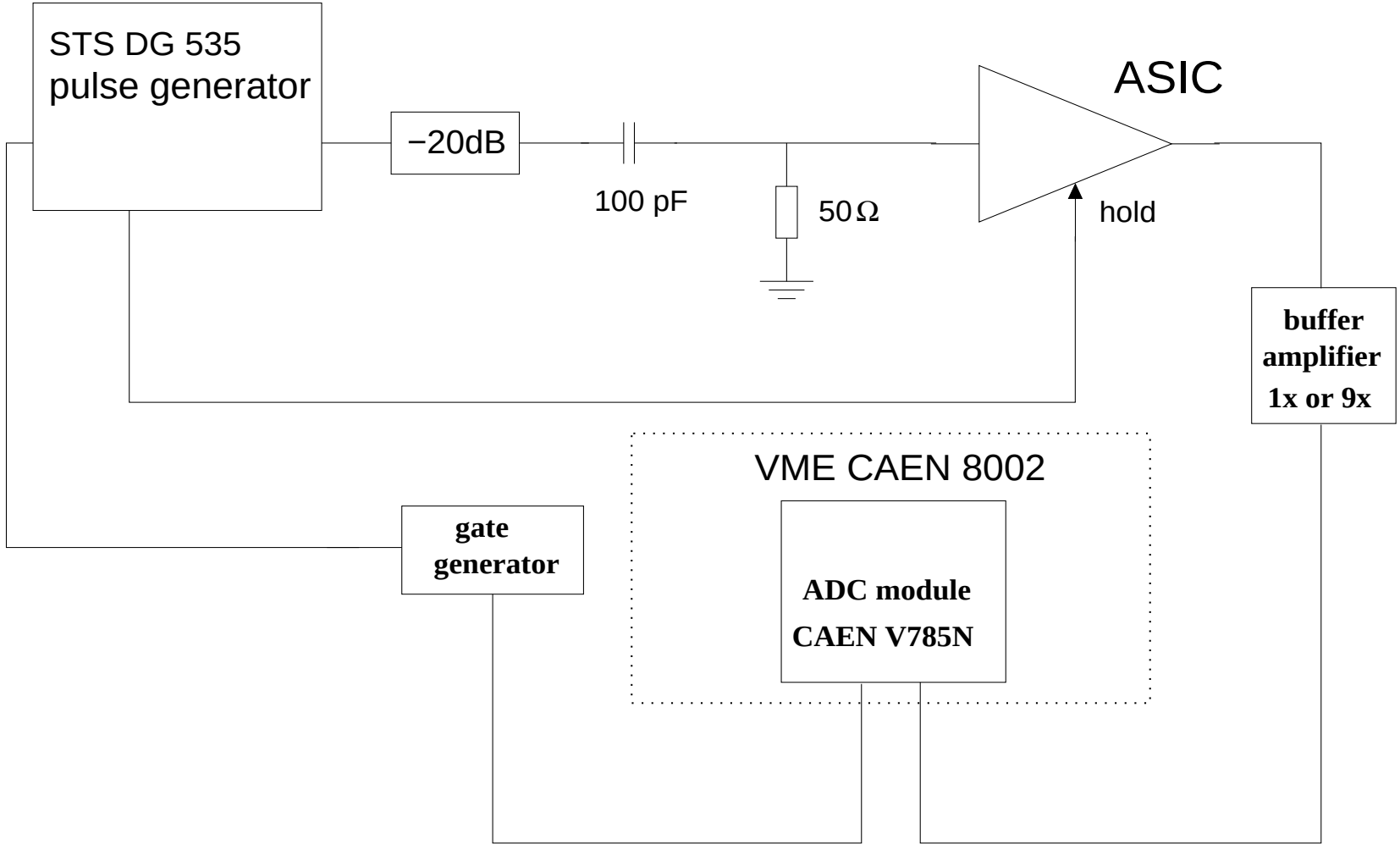
SPIROC ASIC Description and Properties

Analogue part:

one channel layout



Test-Bench Description

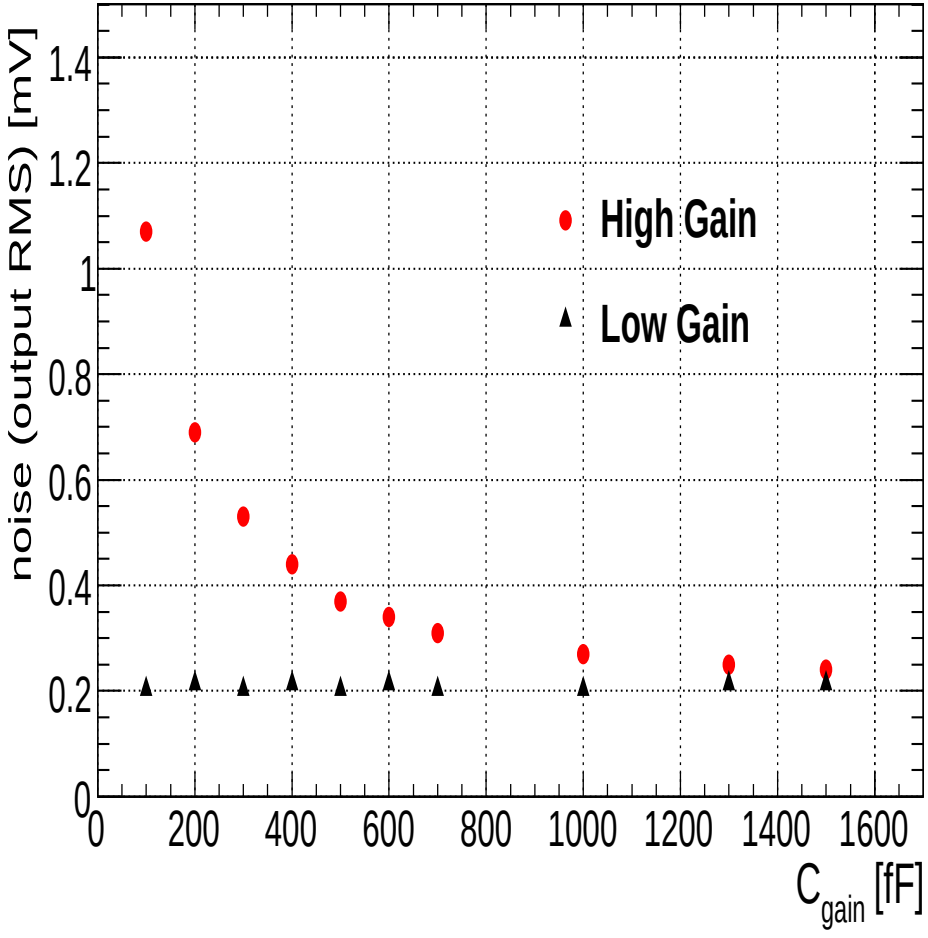


Noise Studies

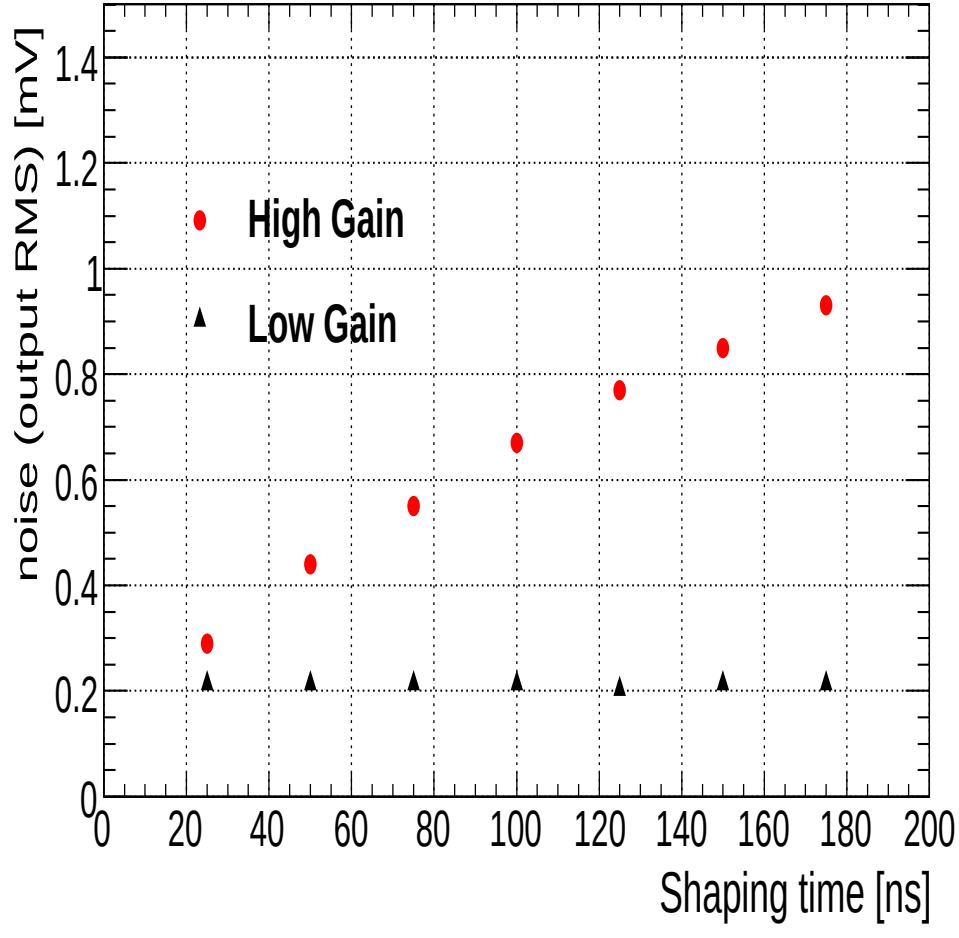
Electrical Noise Investigation

- **Noise affecting processed signal was measured at different working conditions of the chip (no input line connected)**

Channel by channel spread negligible



⇑ **for** 50 **ns shaping time** ⇑



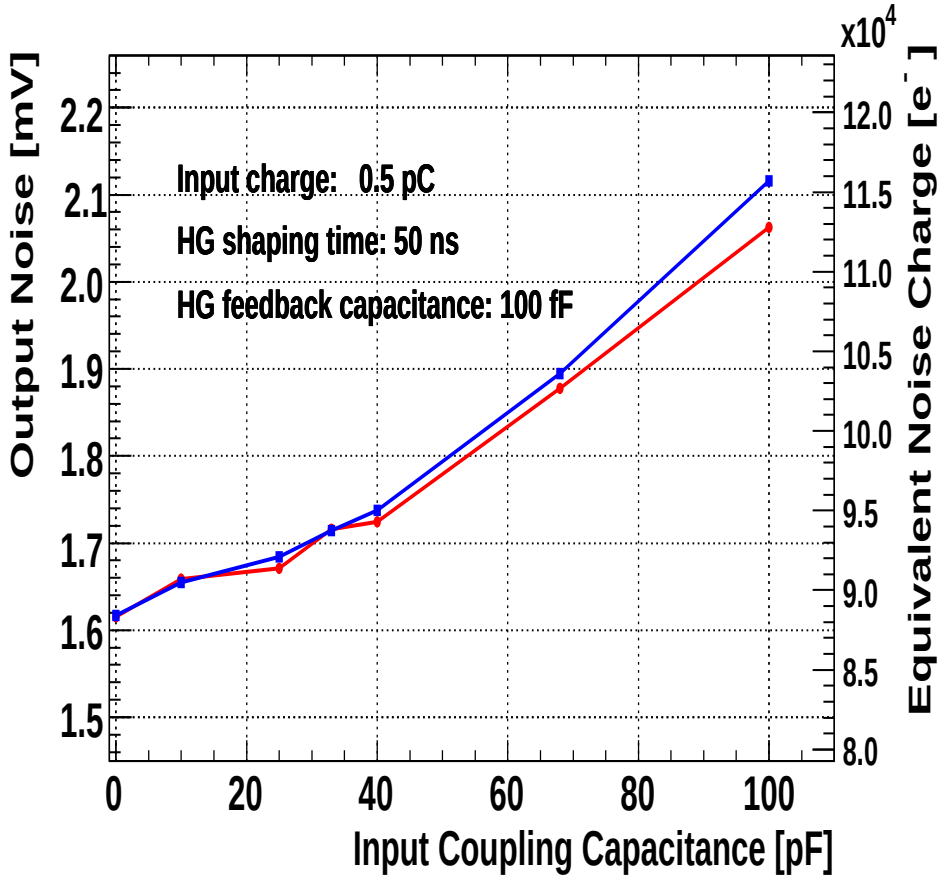
⇑ **for** 400 **fF variable capacitance** ⇑

Additional sizable effect ($\approx 3X$) **from Track and Hold switch**

ENC and Input Detector Capacitance

- **Connecting a SiPM expected to increase noise depending on coupling capacitance (CC**

  — crucial to quantify noise sensitivity to external variable capacitance (SiPM)



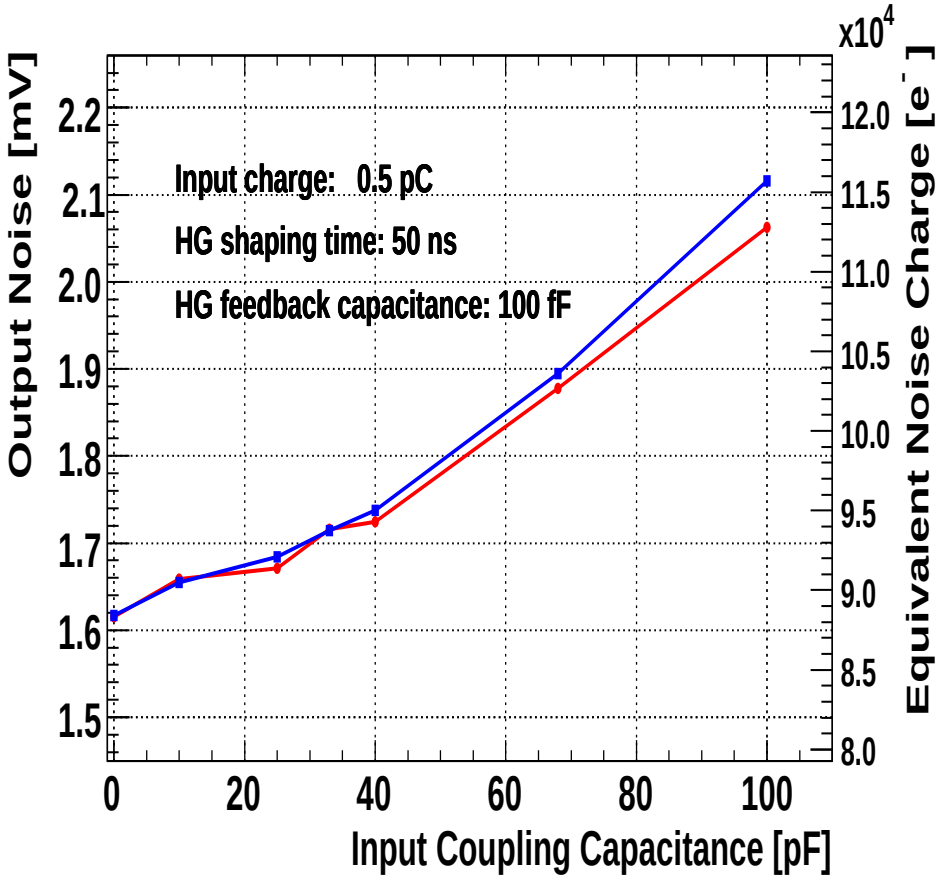
20% effects in the 0-100 pF range

observed non-reproducibility

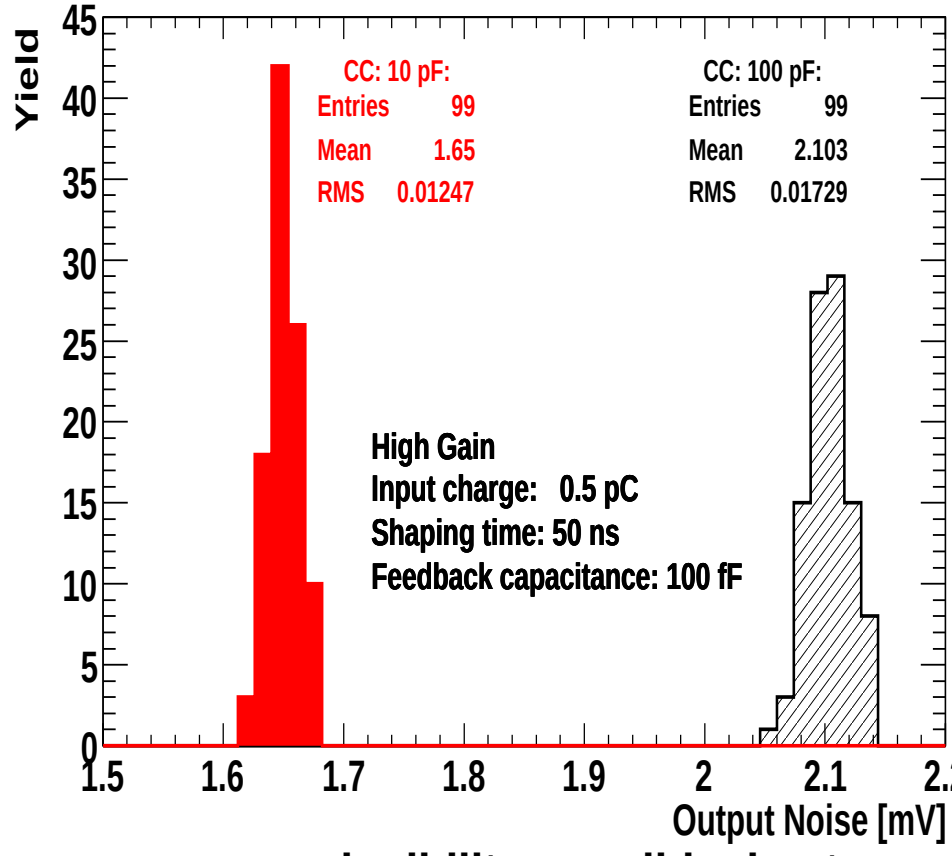
ENC and Input Detector Capacitance

- **Connecting a SiPM expected to increase noise depending on coupling capacitance (CC**

— crucial to quantify noise sensitivity to external variable capacitance (SiPM)



Reiterate measurements:



20% **effects in the** 0-100 **pF range**

observed non-reproducibility

non-reproducibility possibly due to

experimental setup

Trigger Studies

Auto-Trigger Mode Operation Principles

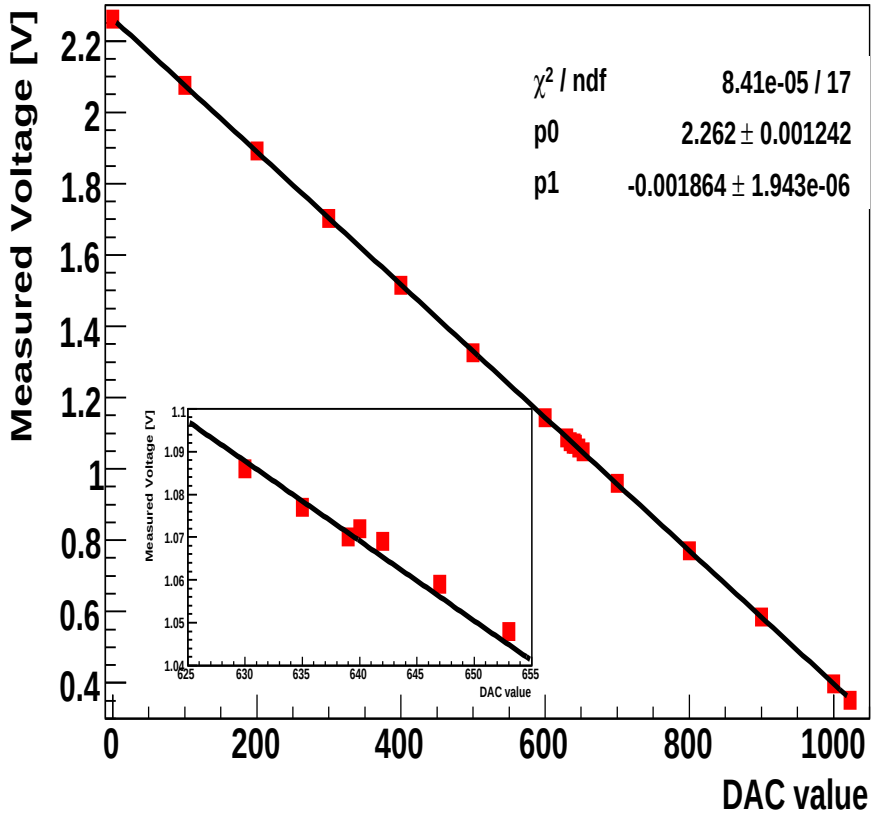
- **Chip designed to operate in 'auto-trigger' mode**
- **Signal from 15 ns fast shaping enters a adjustable discriminator**
  - **— 10 bits DAC common to all channels**
  - **— Threshold for each channel individually adjustable by 4 bits DAC**
- **If signal overshoots threshold, trigger is generated to hold signal at its peaking amplitude and store in analogue memory**
- **Crucial to investigate trigger efficiency and homogeneity for 36 channels**
- **Uncertainty on trigger timing should be studied**

Common Threshold Level (10 bits DAC)

Calibration:

— Change DAC via LabView GUI:

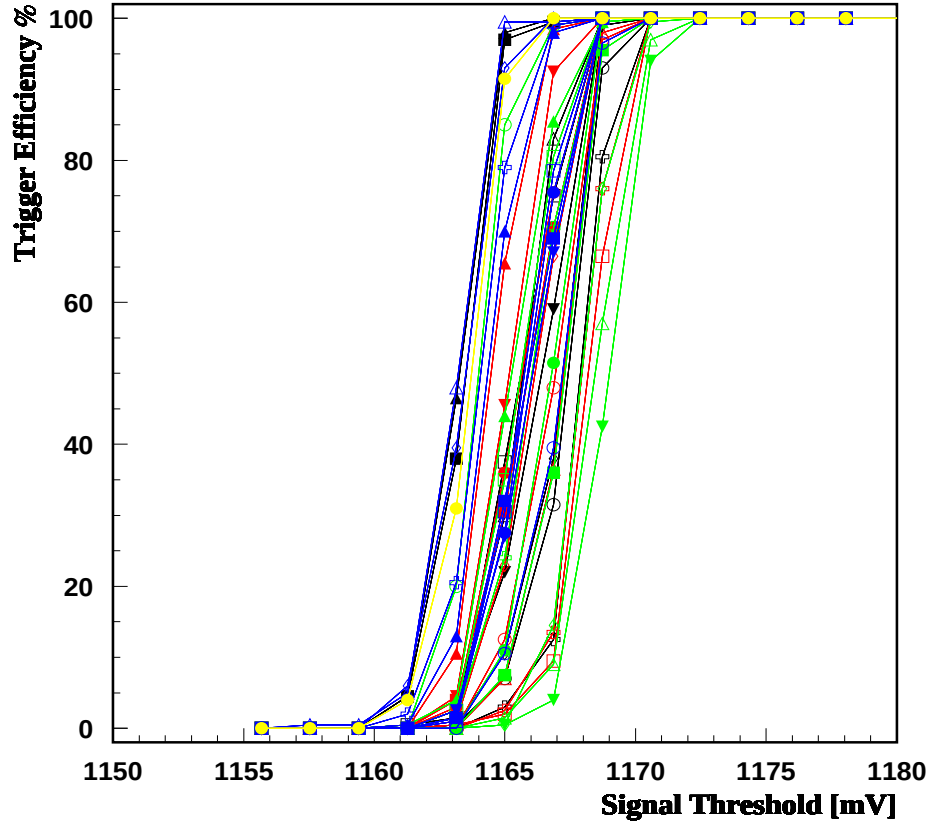
— Measure voltage on board with voltmeter



Trigger Efficiency (for pedestal):

— Increase DAC via LabView GUI:

— Count generated triggers



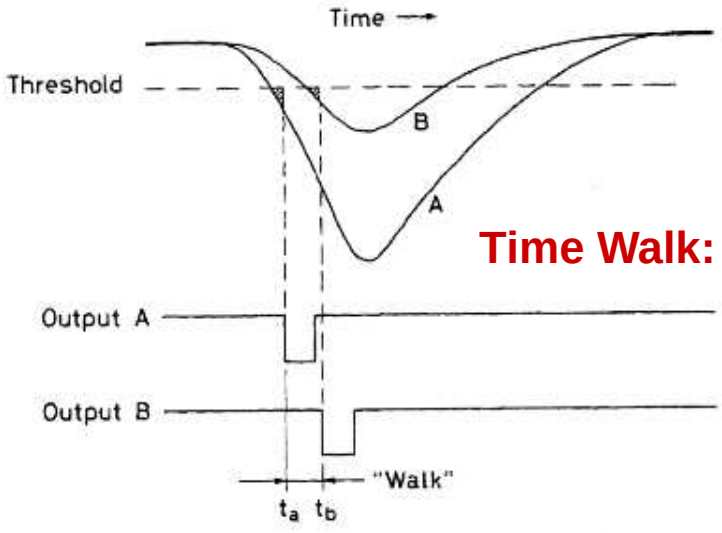
⇑ **measured noise:** ≈ 2-3 **mV** ⇑

channel to channel spread: 8 **mV**

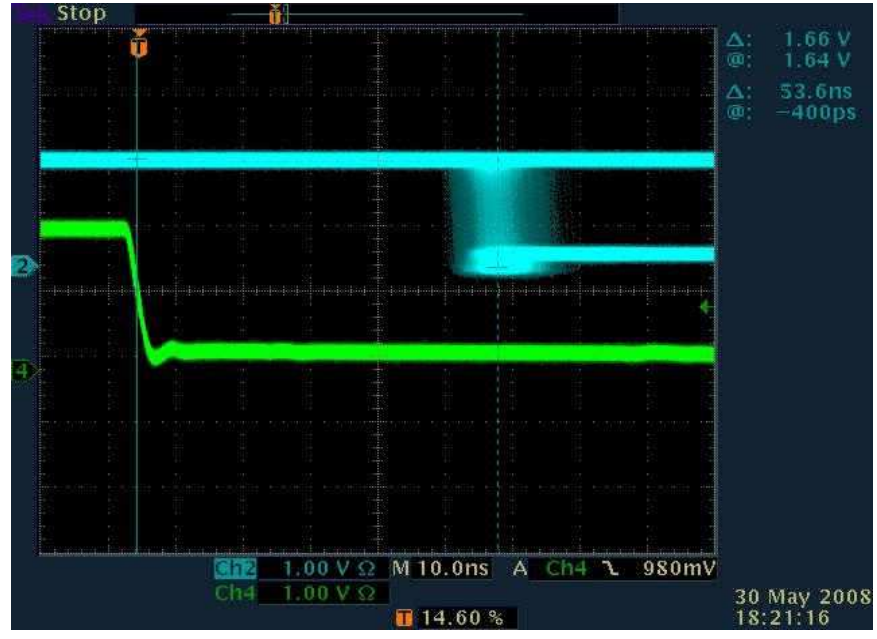
Trigger Time Walk and Jitter

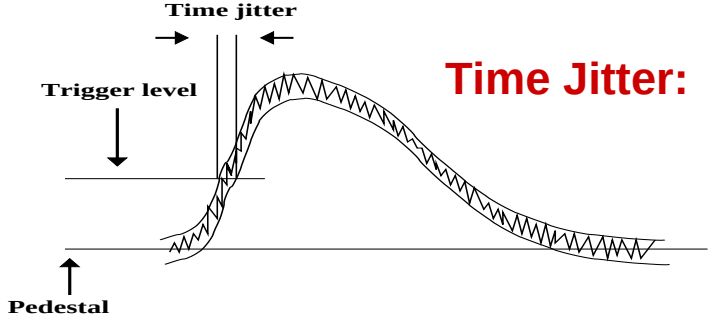
- **Main uncertainty of trigger timing:**

  amplitude dependence



Time Walk: ⇒ **Mean**





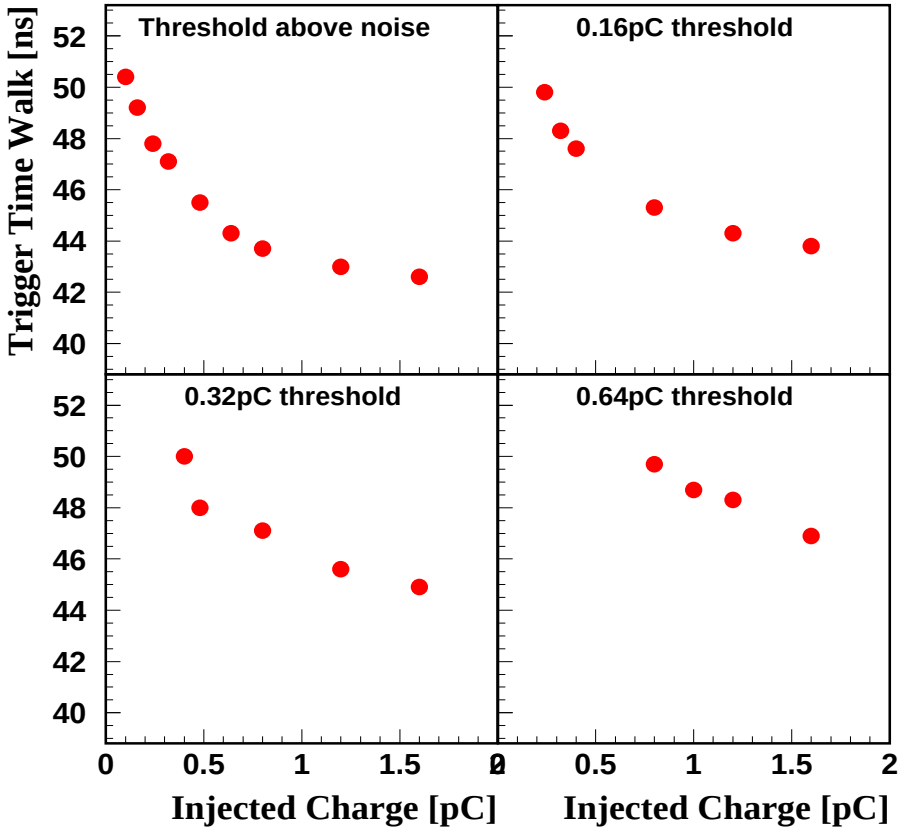
Time Jitter: ⇒ **RMS**

noise dependence

Trigger Time Walk and Jitter

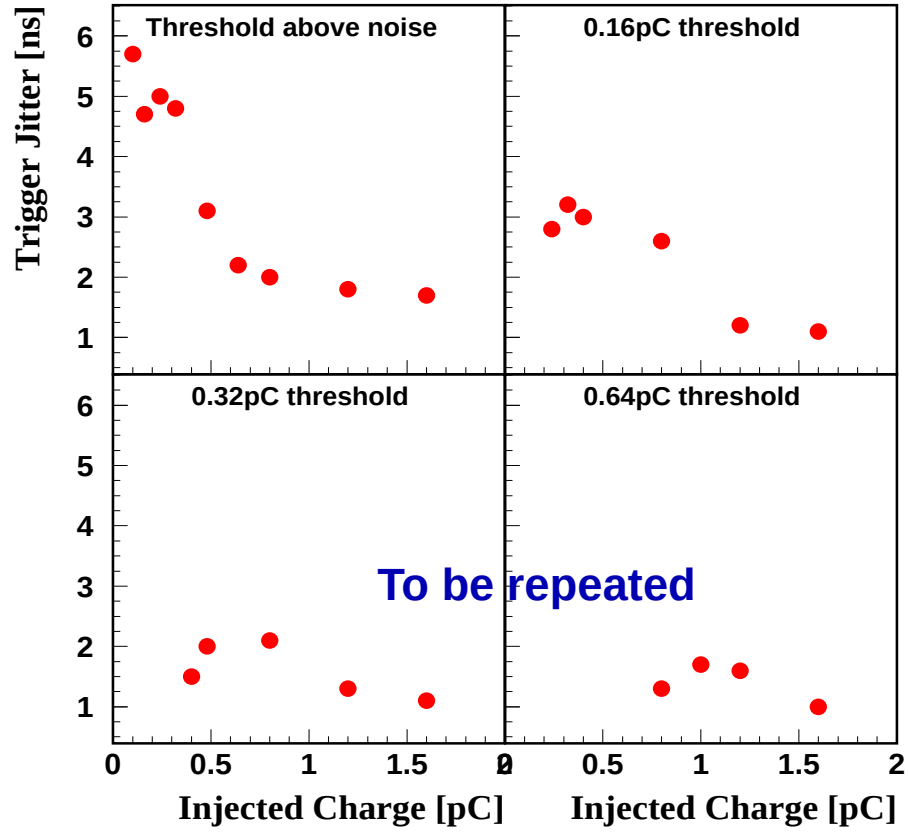
Time Walk:

[Consistent with Orsay]



Jitter:

[$3X$ larger than Orsay]



Large time walk at small injected charge and threshold level

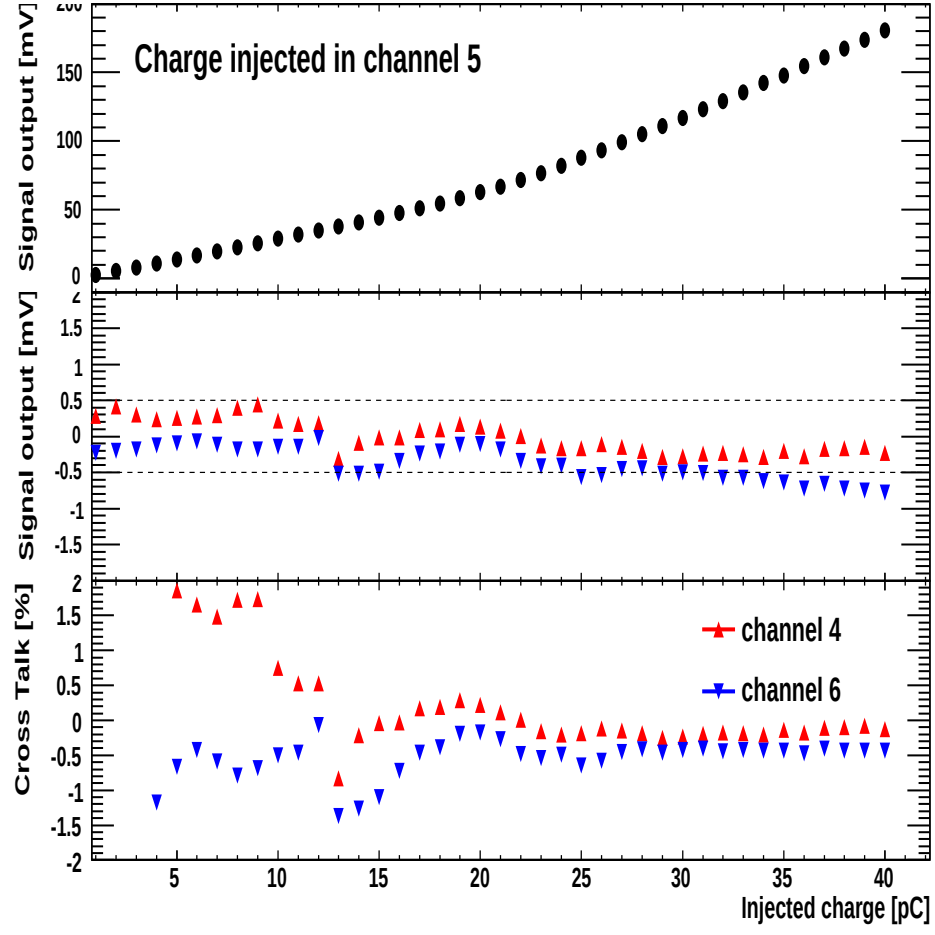
$\Rightarrow$ **Auto-trigger operation for calibration problematic (it was not forseen!)**

$\Rightarrow$ **No problems for physics mode (threshold at $1/2$ mip)**

Cross-Talk

Cross-Talk between Input Channels

- **ASIC should handle 36 input lines**
- **Orsay measurements presented for low injected charge values**
  - **— estimated cross-talk: $\approx 0.3\%$ at $Q_{inj} = 15$ pC**
- **Extend measurements to wider input charge range (up to ≈ 33 mips)**



⇒ Pedestal variation within $\approx \pm 0.5\%$ mV

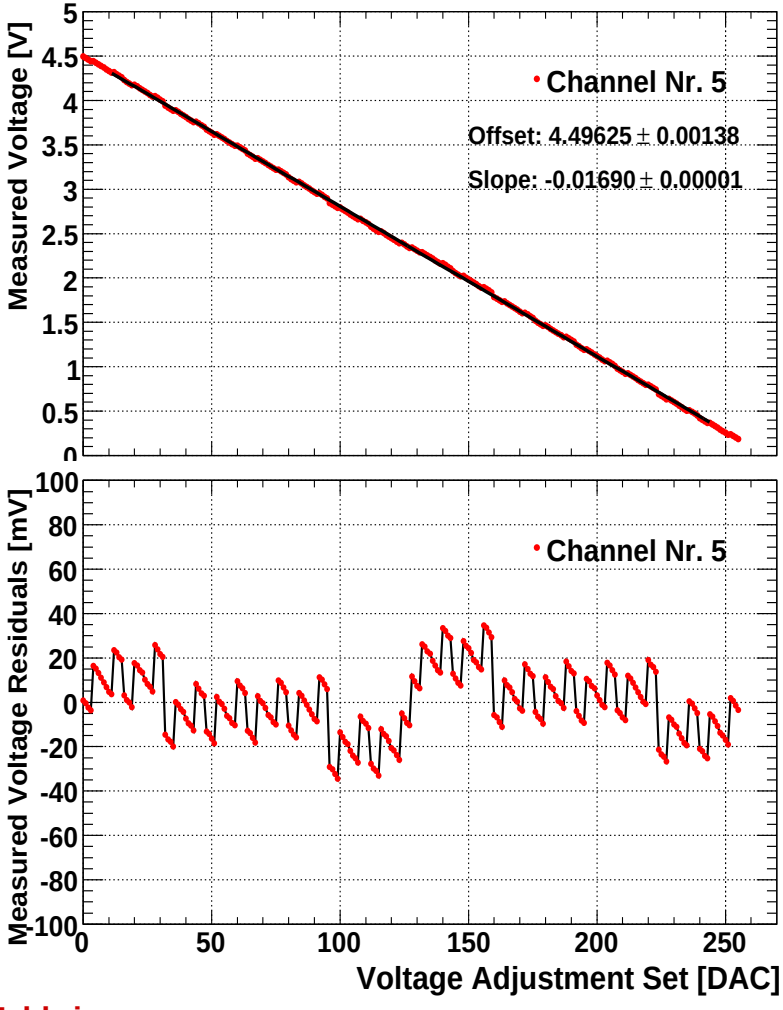
⇒ Result close to previous measurement

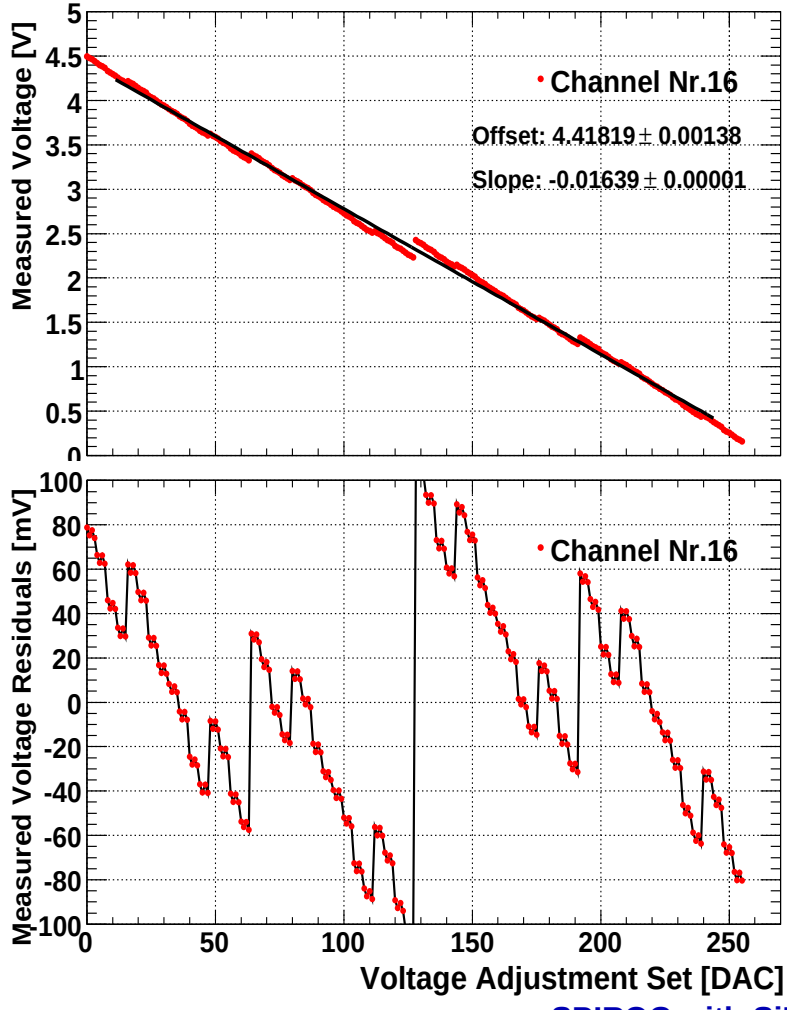
- **— within systematics (fluctuations)**
- **— fluctuations given by setup/analysis ?**

SiPM Voltage Adjustment

SiPM Voltage Adjustment

- ASIC forseen to provide common forward voltage to 36 connected SiPMs
- Single channel voltage tuning provided by dedicated 8 bit DAC adjustment
- Calibration of DAC to HV performed via dedicated LabView routines



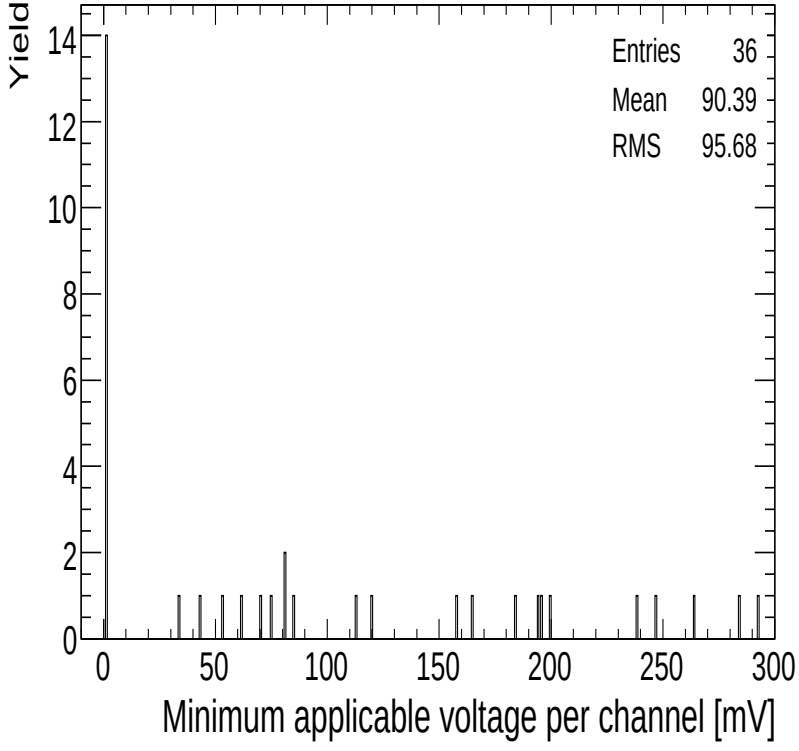


SiPM Voltage Adjustment

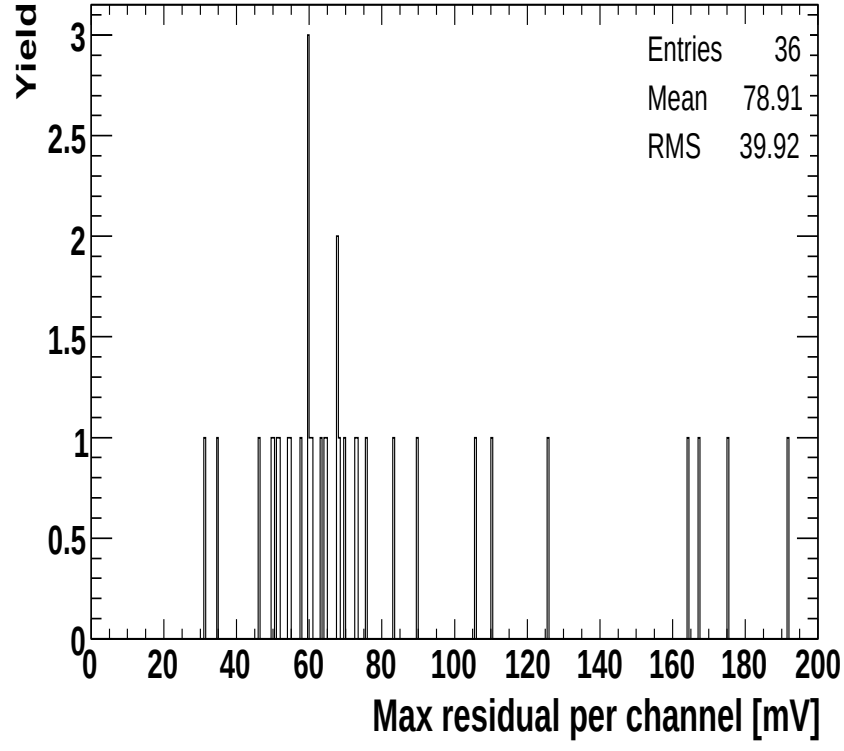
Applied voltage ranges approximately between 0.0 and 4.5 V

- **Possible Problems:**

Ranges differ channel by channel



Residuals up to 200 mV



$\Rightarrow$ **Relative gain change of $\approx 5.2\%$ due to large residuals ($\frac{\Delta G}{G \Delta V} \approx \frac{2.6\%}{100mV}$)?**

$\Rightarrow$ **Systematical uncertainty to energy calibration?**

Dynamic Range, Linearity, and Gain of the ASIC

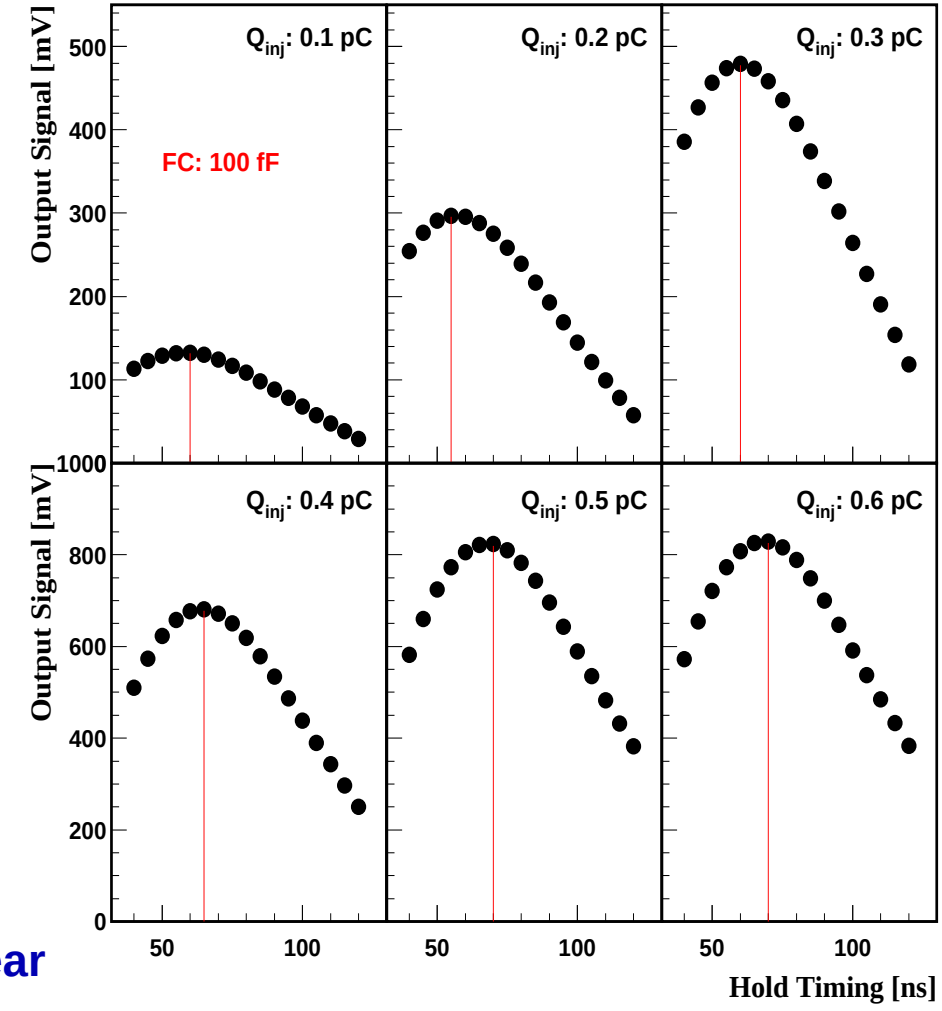
Track and Hold Switch

- Processed signal forseen to be held at peaking amplitude by track and hold switch
- Peaking amplitude reconstructed using

  T&H found to be:

  — charge dependent

  — larger than w/o using T&H



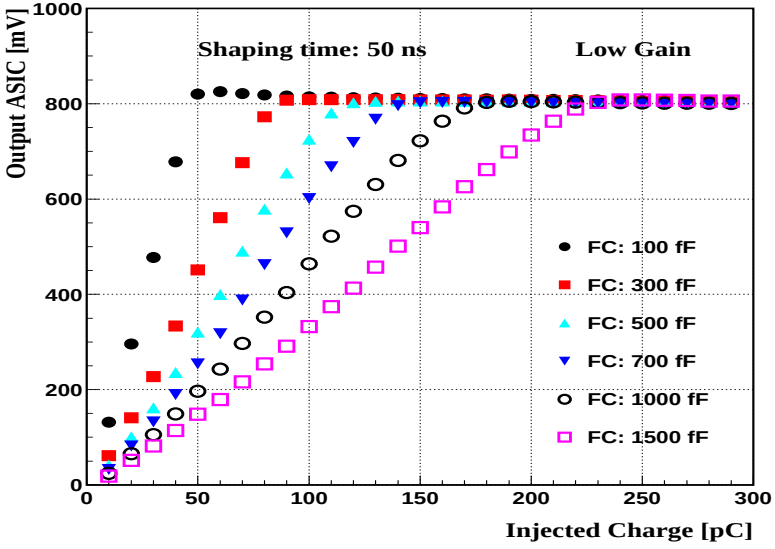
- Using T&H switch is necessary for

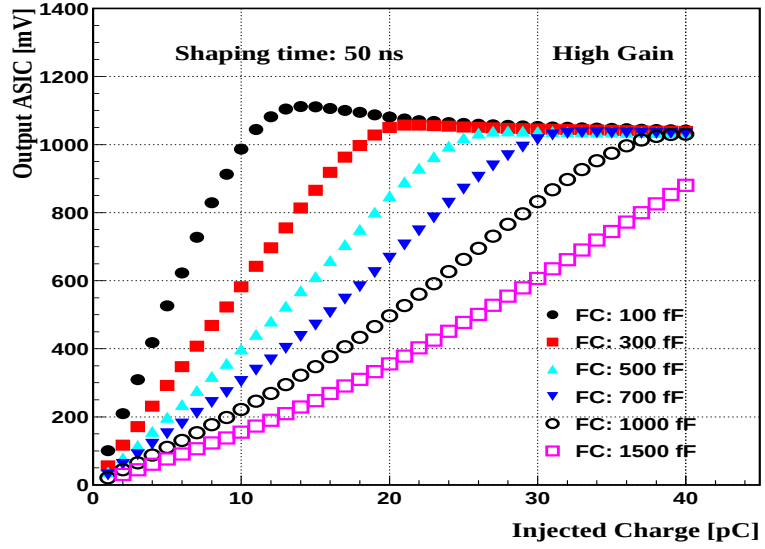
  extensive systematical measurements
- T&H switch forseen in ILC data taking

  ⇒ used for presented measurements

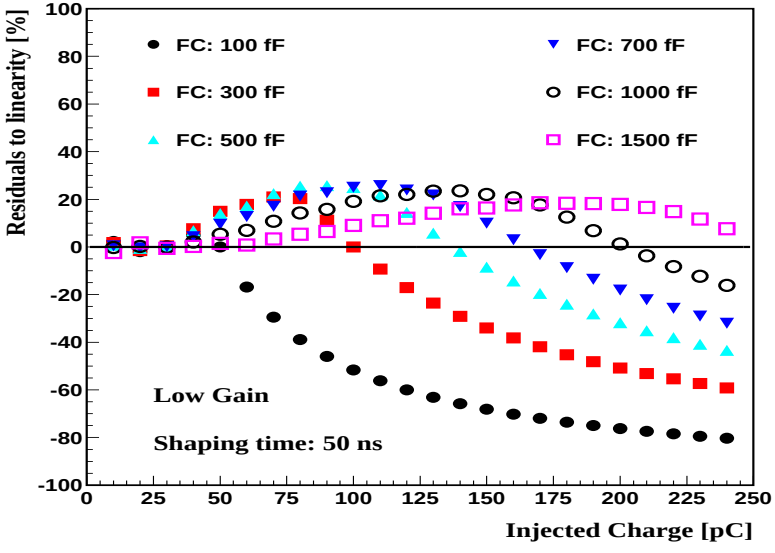
  ⇒ possible effects on measurements
- W/O T&H peaking amplitude appears linear

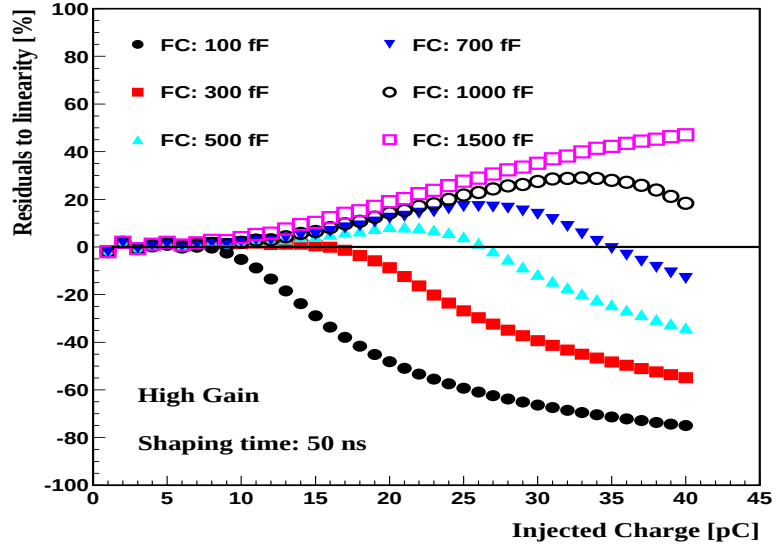
Linearity Measurements





1 pxl = $5 \cdot 10^5$ e $\approx$ 0.08 pC





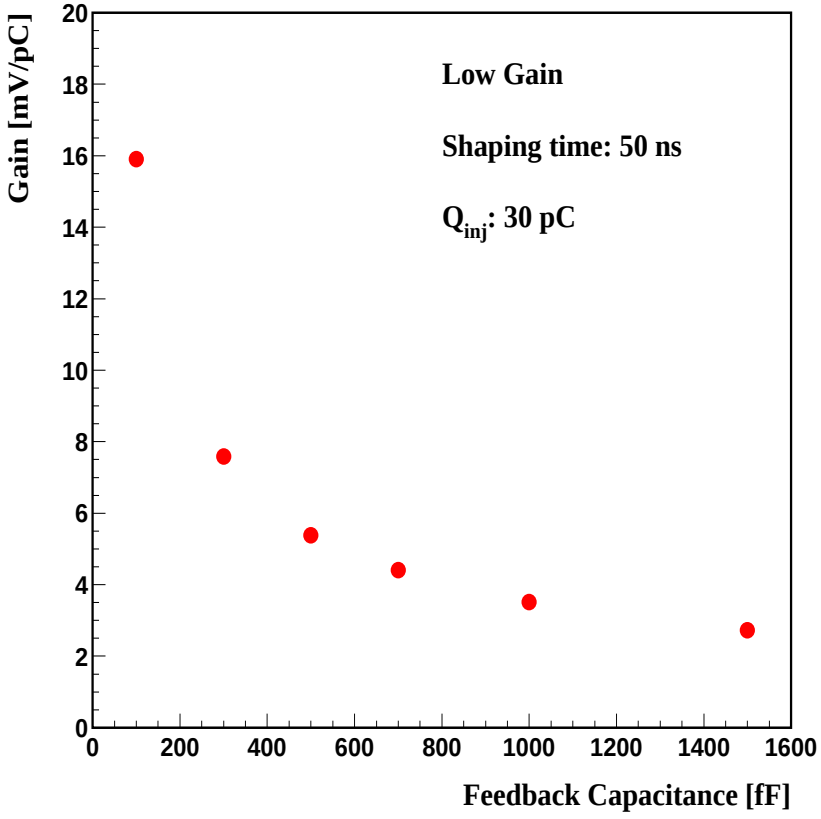
- **SiPM dynamic range: ≈ 77 mips (1156 pxl / 15 pxl per mip) ≈ 92 pC**

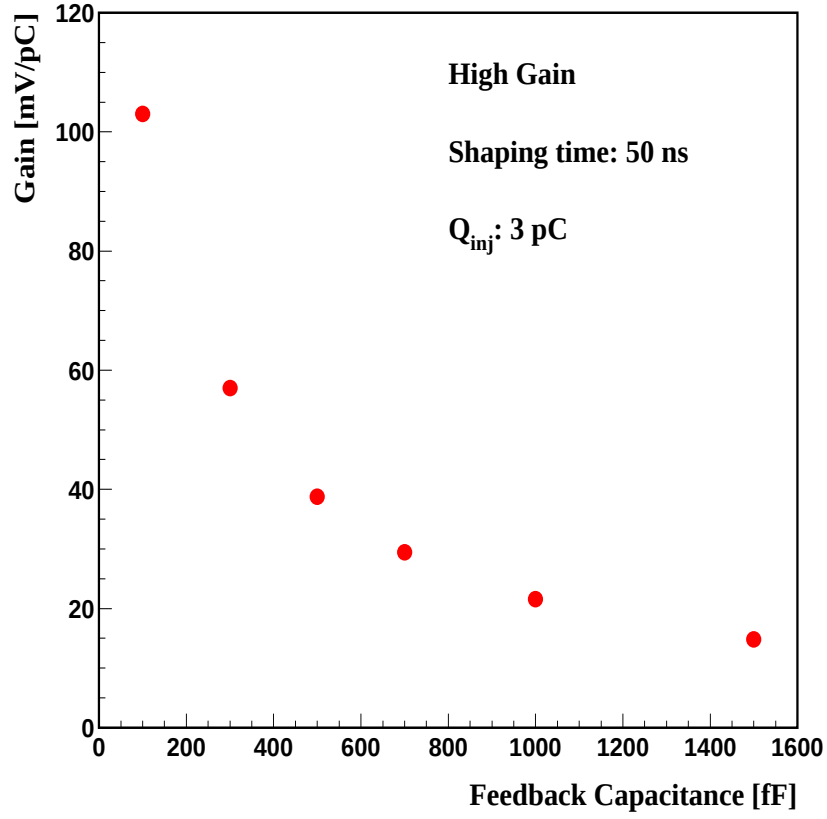
  $\Rightarrow$ covered for FC ≥ 300 fF (physics mode) [calibration OK for > 100 fF] at $5 \cdot 10^5$ gain

  $\Rightarrow$ Strong non-linearity due to T&H switch (possibly understood by Orsay group)

Gain Measurements

- **Gain calculated as** $G_{ASIC} = \frac{V_{output}}{Q_{input}} [\frac{mV}{pC}]$





$\Rightarrow$ **Expected behaviour** $1/C_{FC}$ **observed**

$\Rightarrow$ **Qualitative agreement with Orsay measurements**

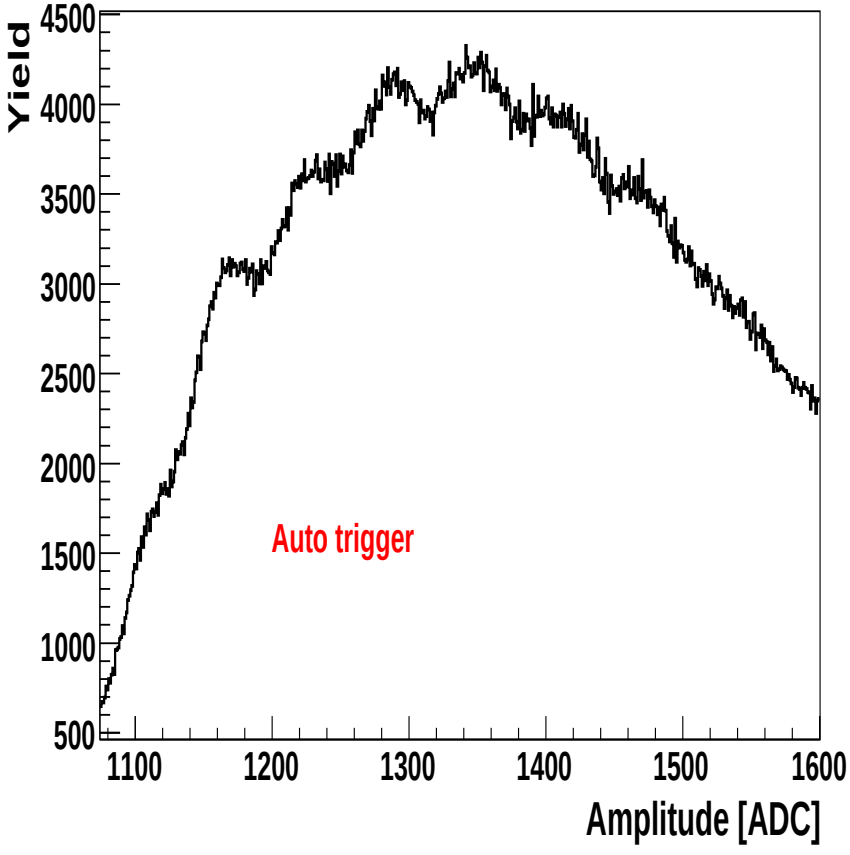
Simulating Real Data Taking Conditions

Single-Pixel Spectra

How to perform SiPM calibrations?

- Process signal from SiPM fired by LED (synchronised with opening of ADC gate)

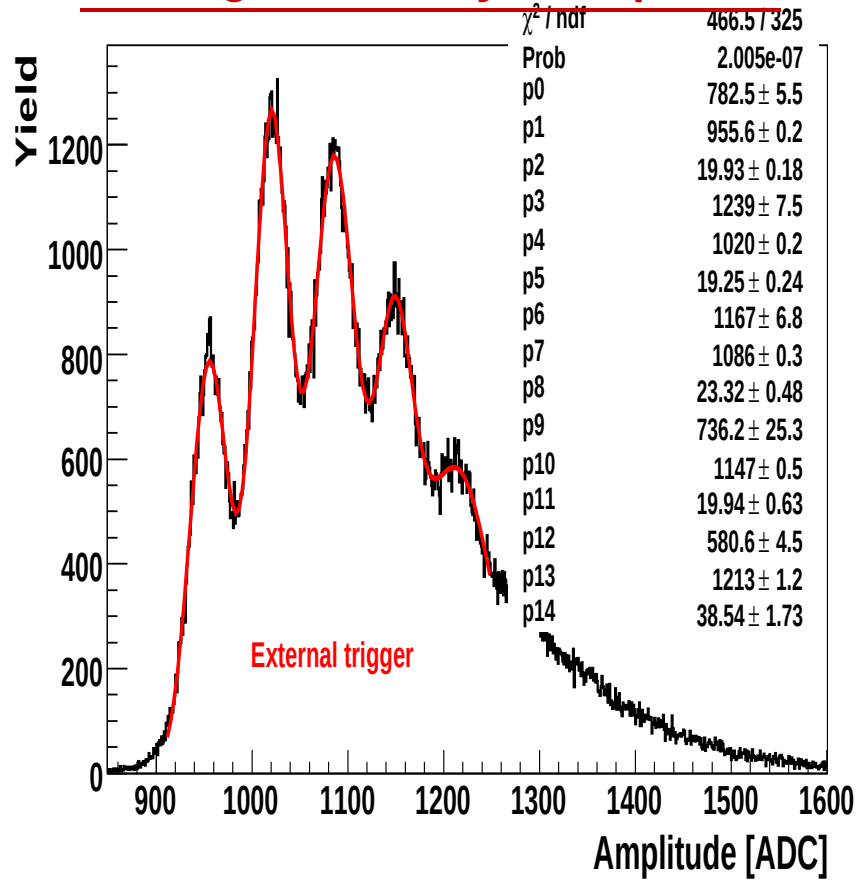
ASIC auto-trigger mode



⇒ Calibration not feasable in this mode

As expected, and NOT forseen

HOLD generated by main pulser



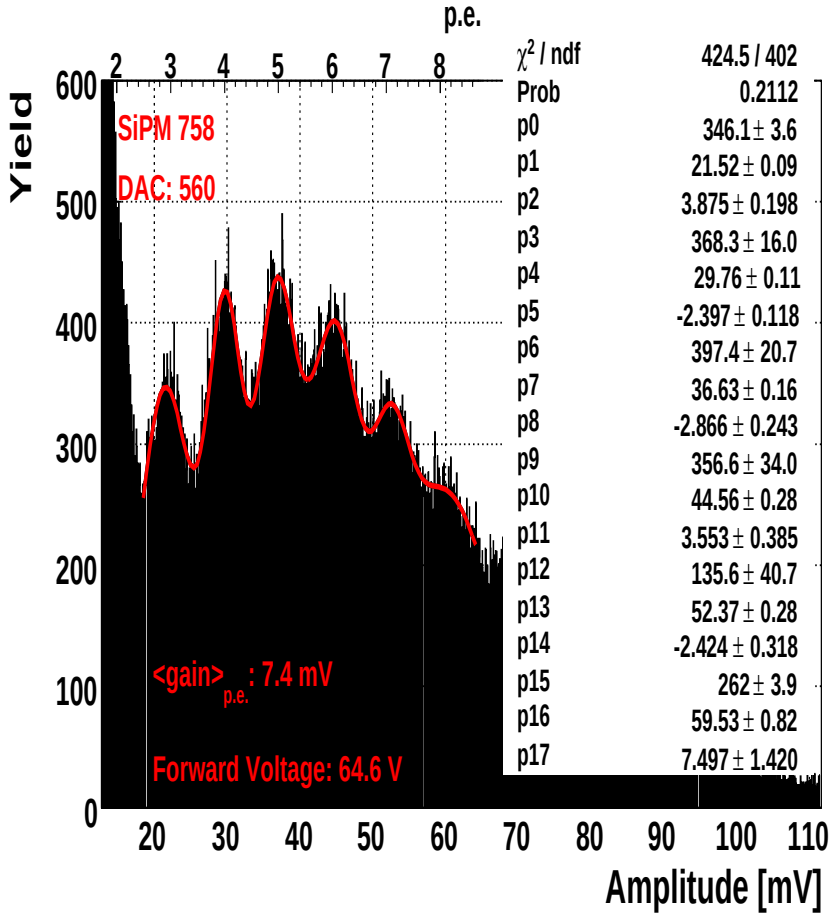
⇒ Reliable fit can be obtained

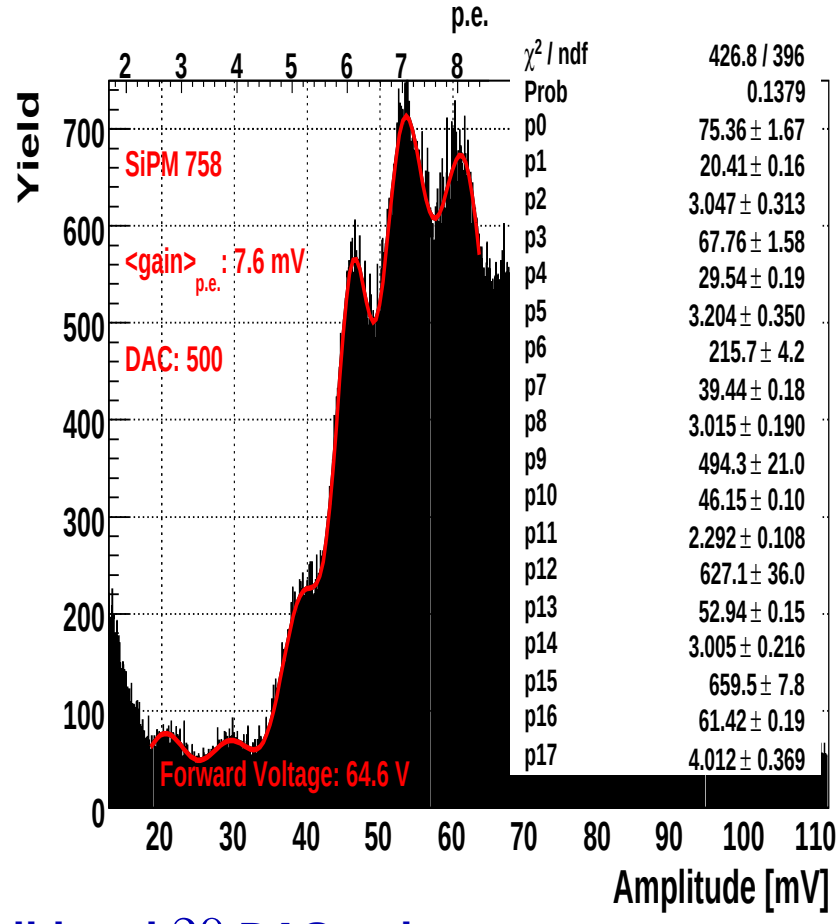
Data Taking in Physics Mode

- **We want a proof of principle that chip can operate in auto-trigger mode (1/2 mip cut)**

  — need to know where is applied threshold / mip amplitude

- **Process signal from SiPM (LED fired) at different threshold values**



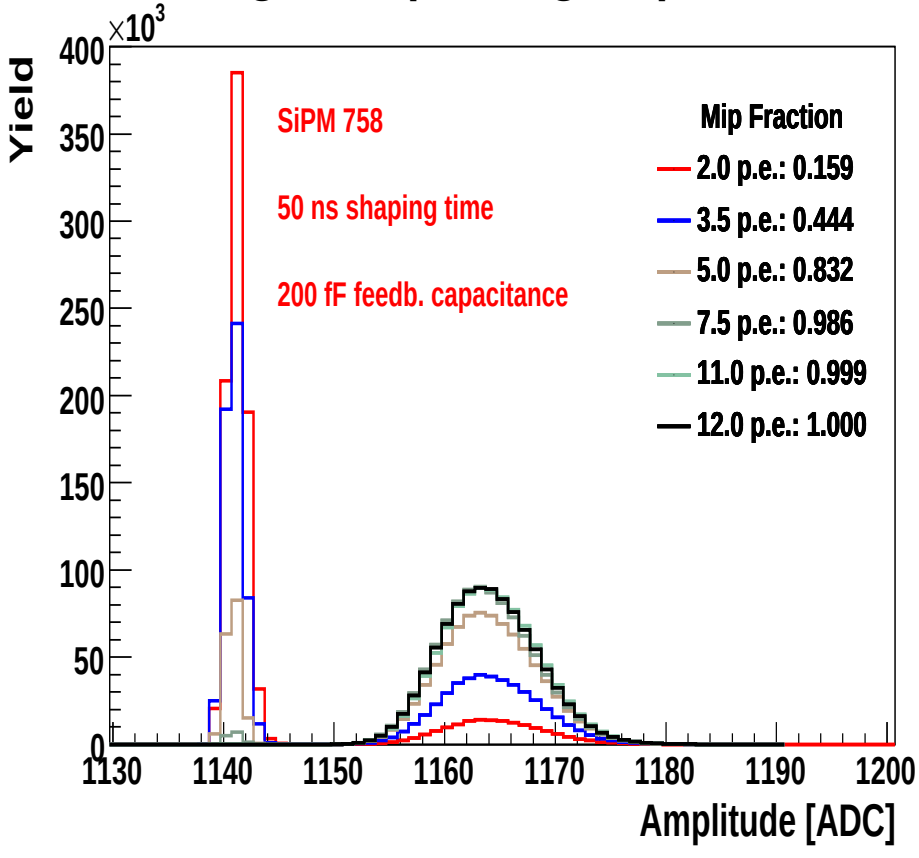


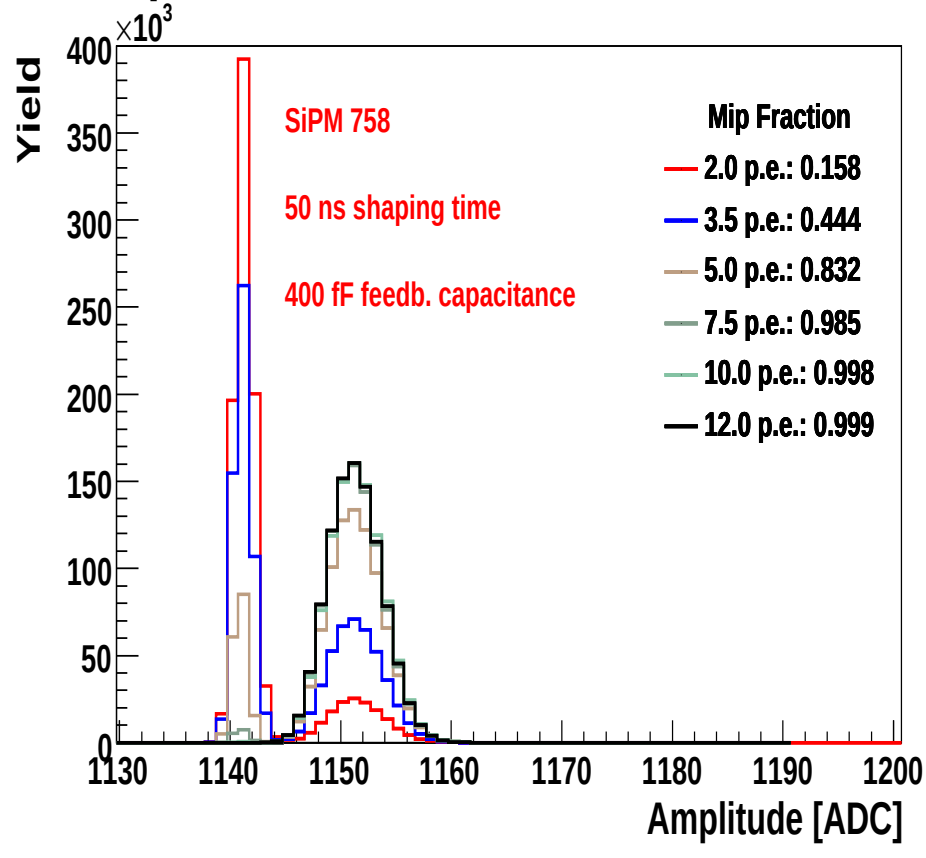
$\Rightarrow$ **Considering entire DAC scan, on average additional 20 DAC units suppress one peak**

$\Rightarrow$ **LED amplitude tuned to generate one mip signal (maximum around 15 pxls)**

Data Taking in Physics Mode

- **Knowing what a DAC value corresponds to, process mip-like signal in low gain**
- **REMINDER: autotrigger does not work in SPIROC I**
  - **— use generated trigger to open ADC gate**
  - **— hold signal at peaking amplitude with external pulser**





$\Rightarrow$ **Almost 100% signal induced triggers at $1/2$ mip threshold cut (proof of principle)**

Summary and Outlook

- Analogue component of SPIROC ASIC extensively investigated
  - — Measurements presented for SPIROC I chip version
- Dynamic range for physics/calibration modes possibly covered (depends on gain)
- ASIC can operate in auto-trigger mode (in low gain)
- Low noise measured
- Low cross-talk
- Gain as expected
- Calibration feasable w ext trigger
- Residuals to linearity of DAC HV adjustment sizable
  - — might affect sizably the energy calibration
- Track and Hold switch strongly affects (linearity) the measurements

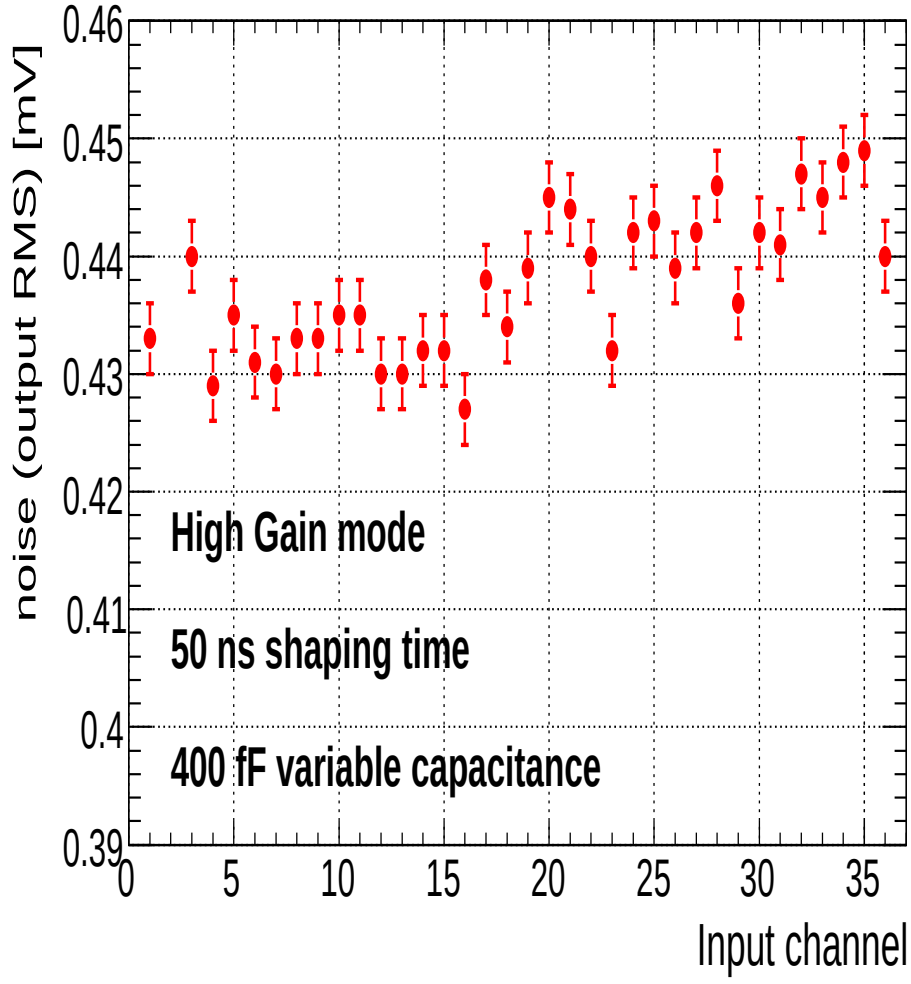
- As further steps:
  - ☞ proceed with SPIROC II
  - ☞ test auto-trigger mode feautures of new chip version (radioactive source?)
  - ☞ timing measurements
  - ☞ power pulsing

Internal Report almost ready

Backup Slides

Noise Uniformity

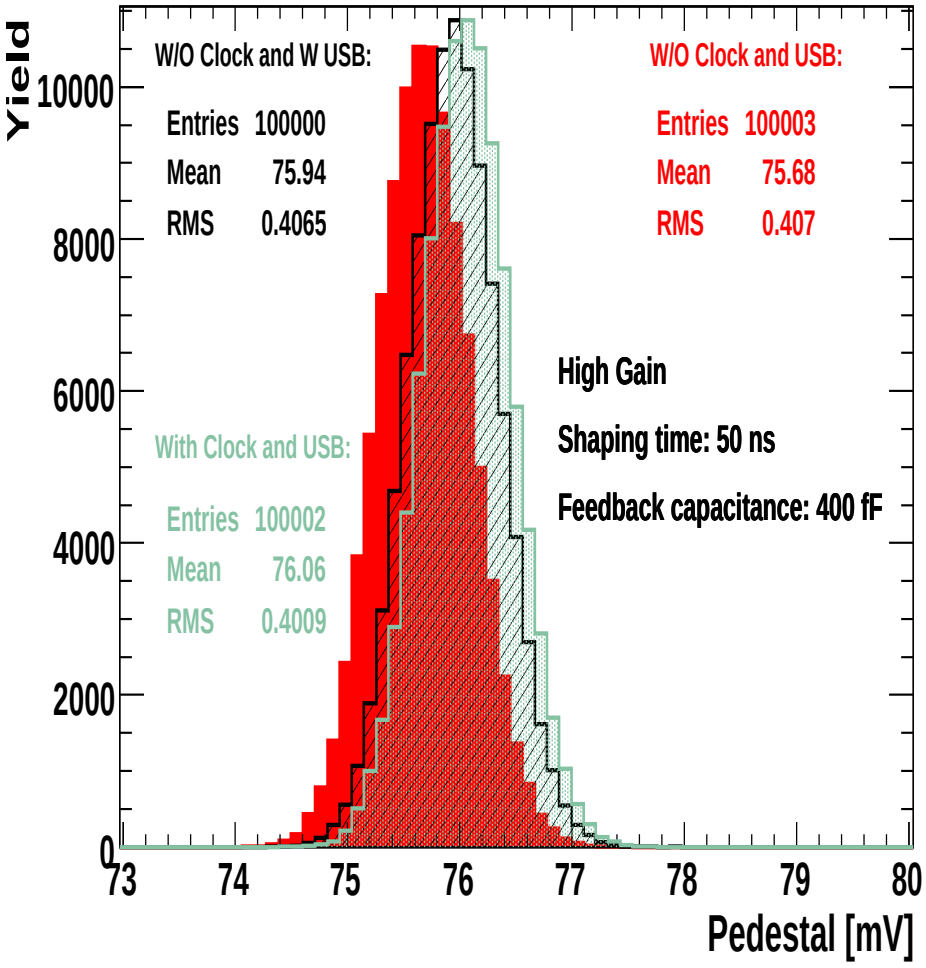
- **Noise measured for all 36 channels (no input line connected)**

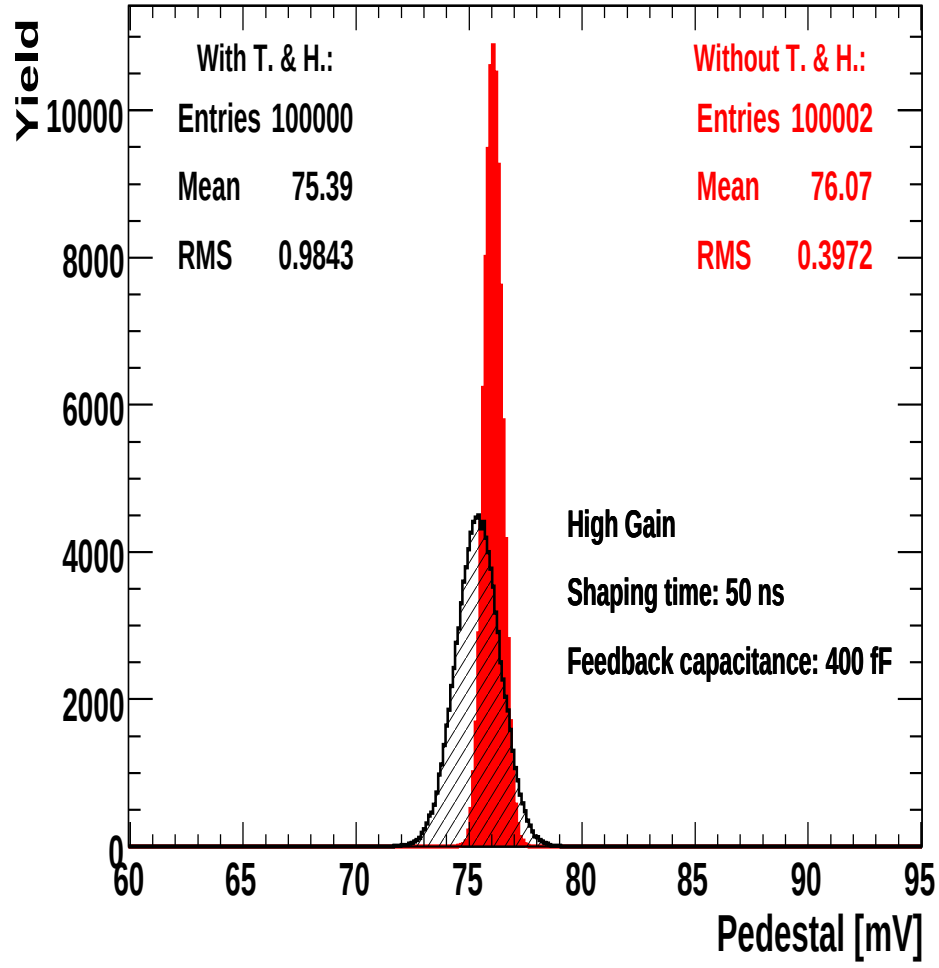


Non uniformity is negligible

Additional Sources to Noise

- **Additional source can affect signal (no input line connected)**



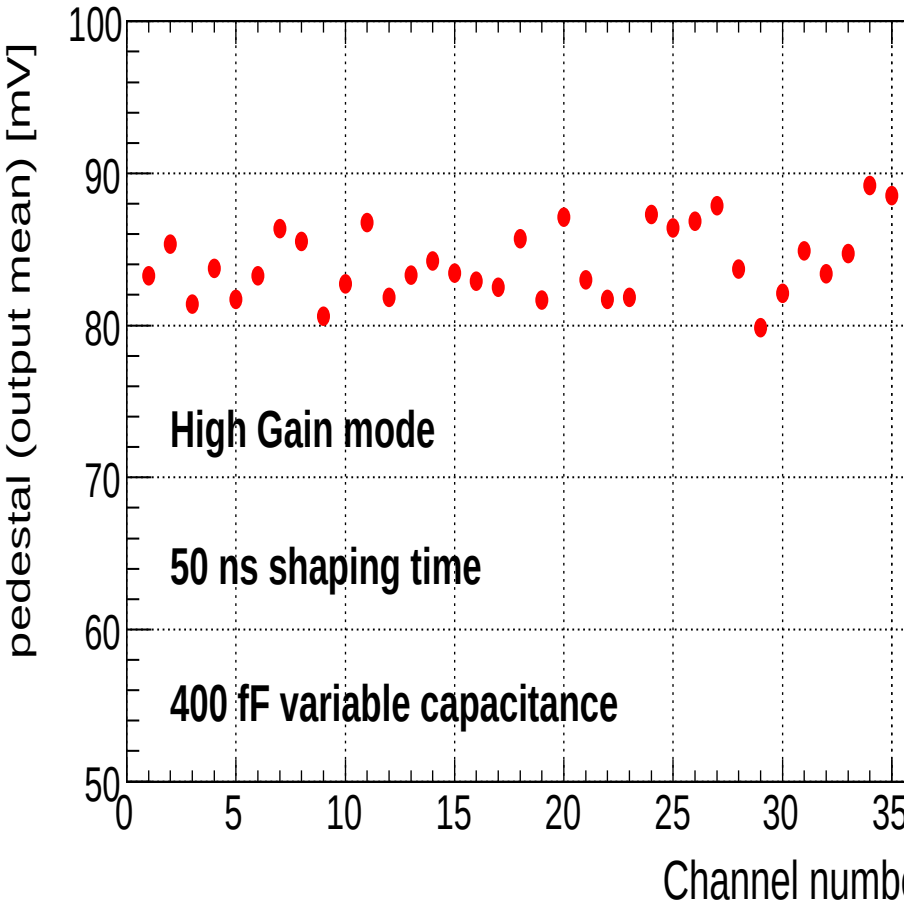


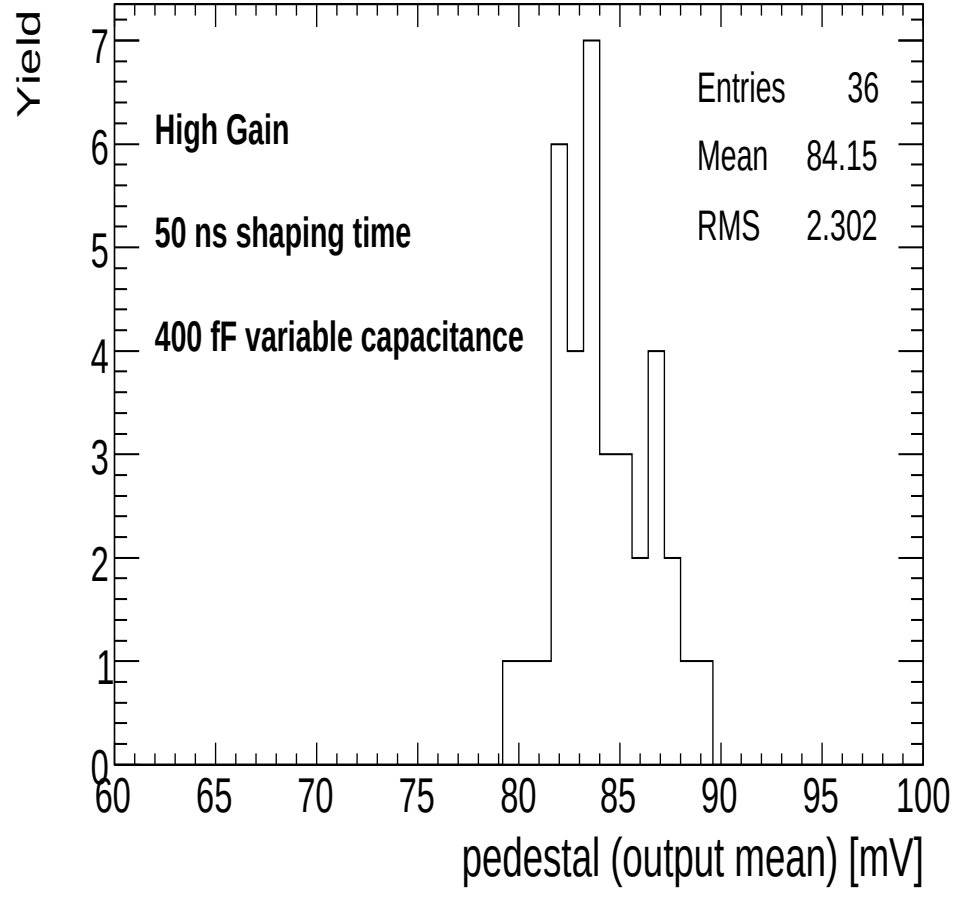
Negligible effect from swithing on clock and plugging in USB

Sizable effect from Track and Hold switch

Pedestals Uniformity

- **Pedestal measured in all 36 channels (input lines not connected)**

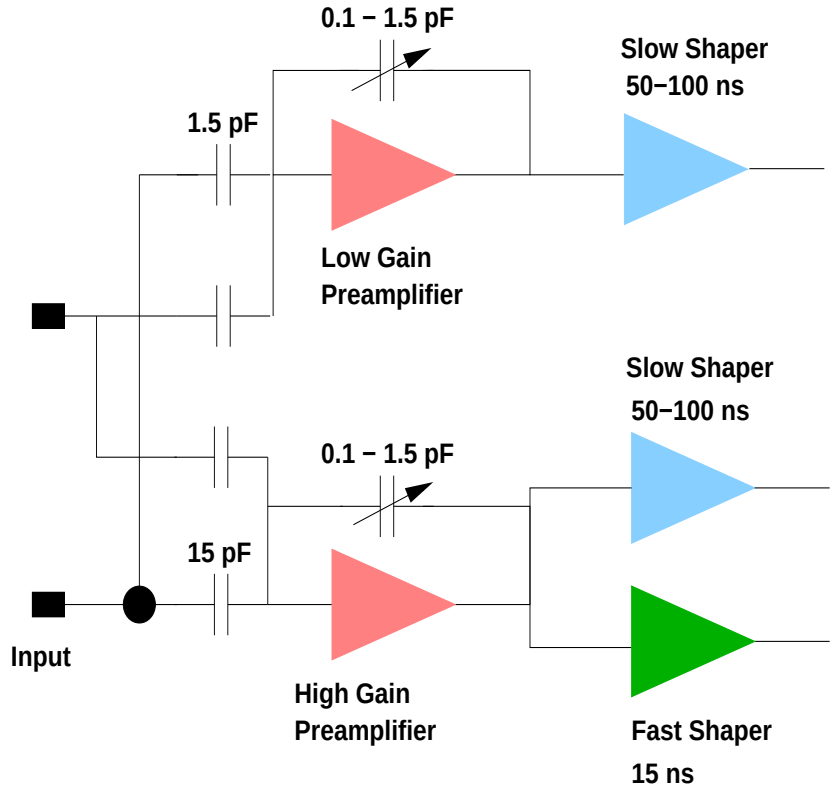




Spread slightly larger than what reported by Orsay group

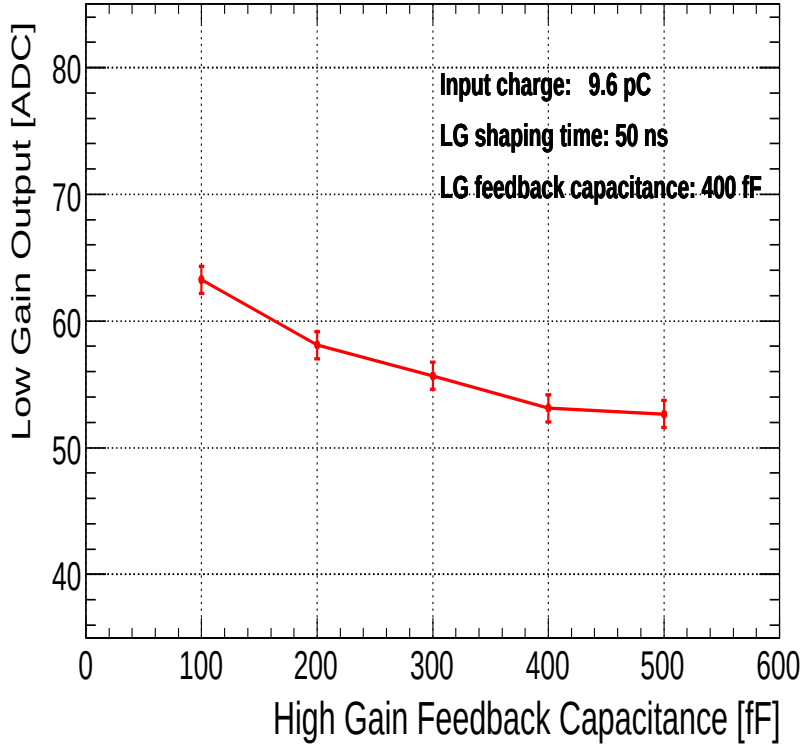
Low Gain - High Gain Coupling

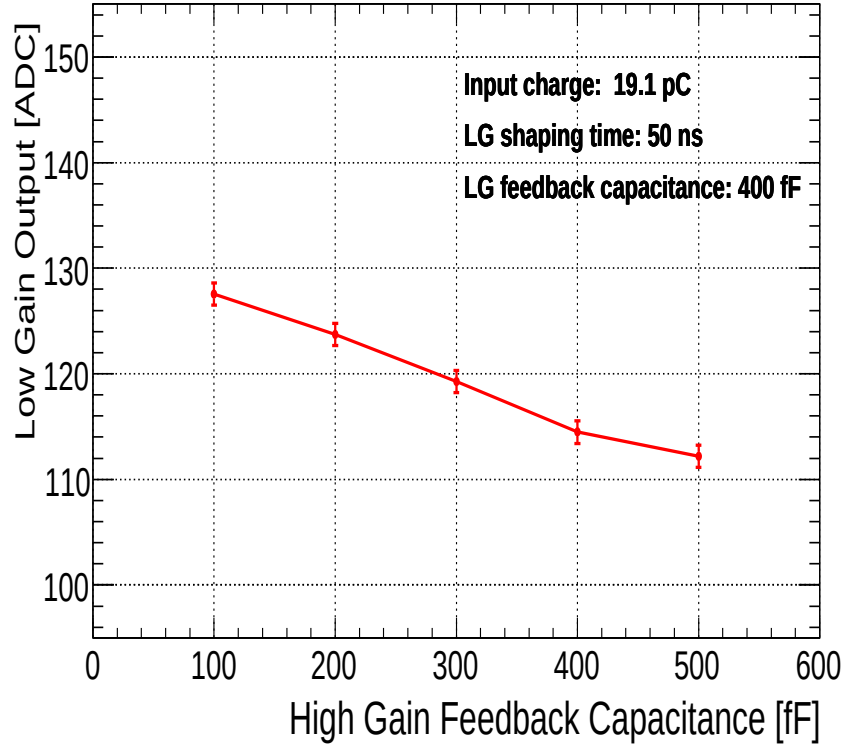
- **Low and high gain paths are electrically coupled**
  - **— charge sharing between paths influenced by preamplifier gain**



Low Gain - High Gain Coupling

- Low and high gain paths are electrically coupled
  — charge sharing between paths influenced by preamplifier gain
- Negligible effect in high gain path by LG preamplification

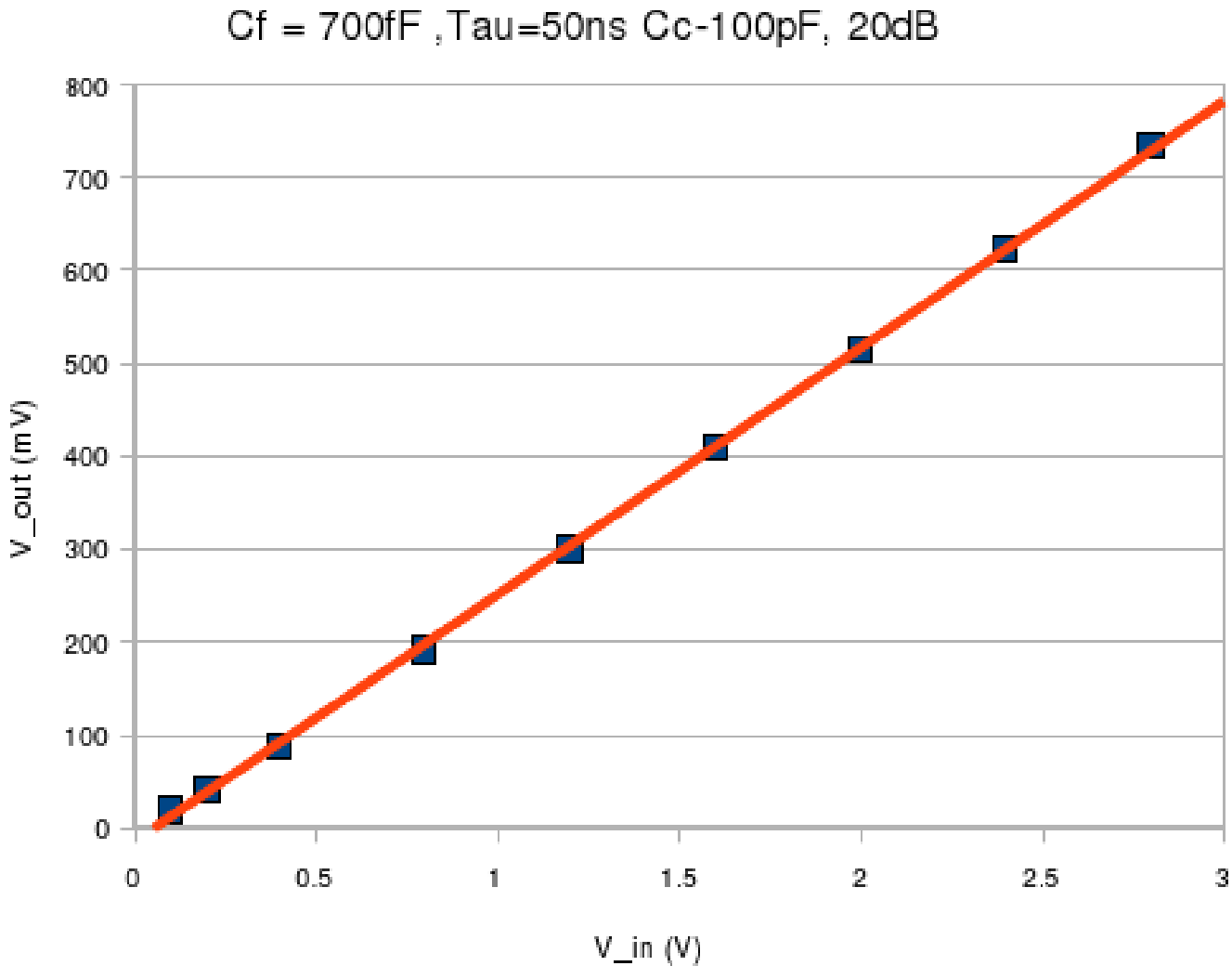




- Up to 10% effect in low gain path by HG preamplification

Peaking Amplitude Linearity W/O T&H

- **The peaking amplitude was measured at the oscilloscope (w/o track and hold switch)**

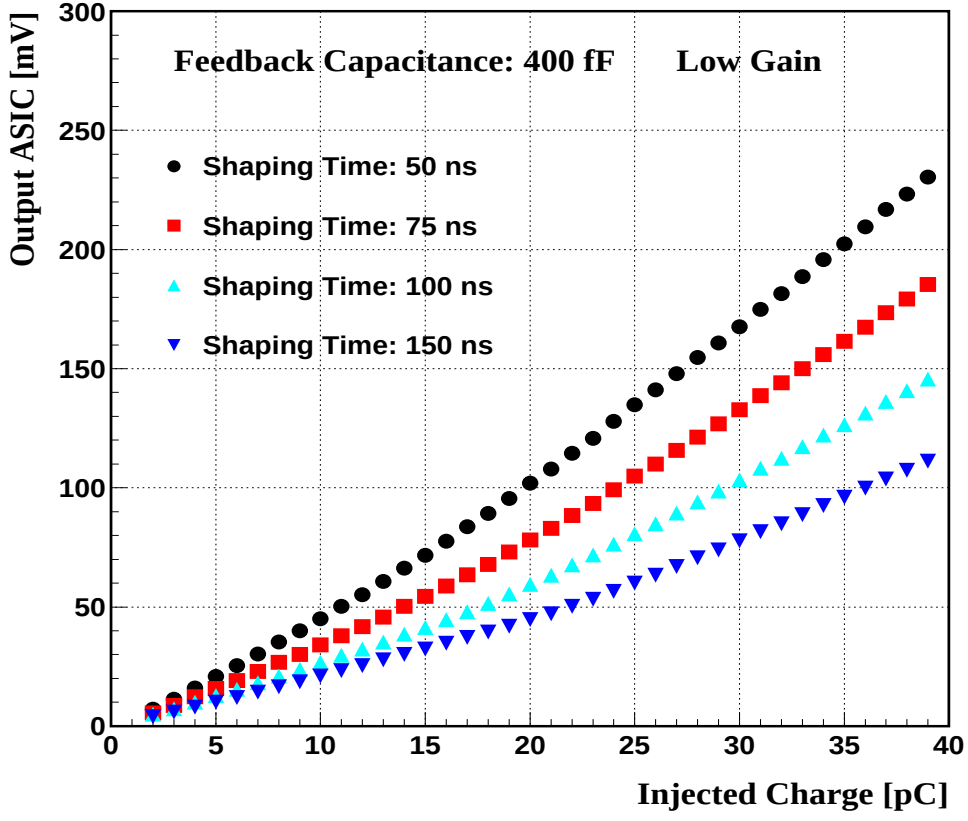


Dependence on Shaping Time

- **Hold signal timing kept fixed during input charge scan**

  — take mean peaking time during scan

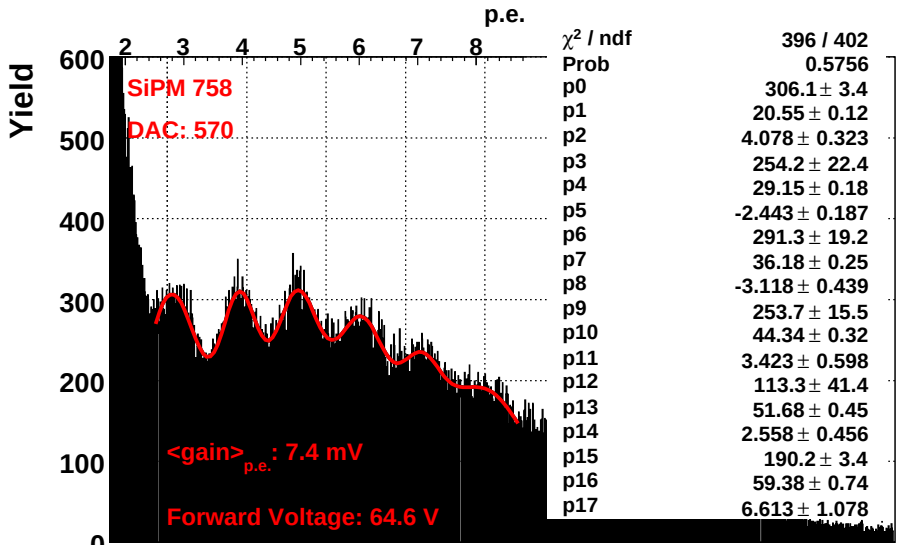
- **Hold signal timing changed according to shaping time**

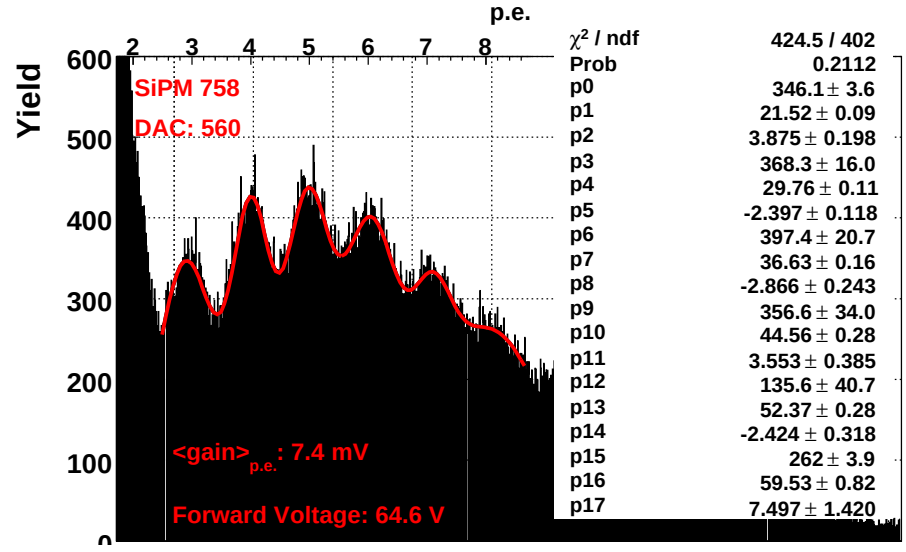


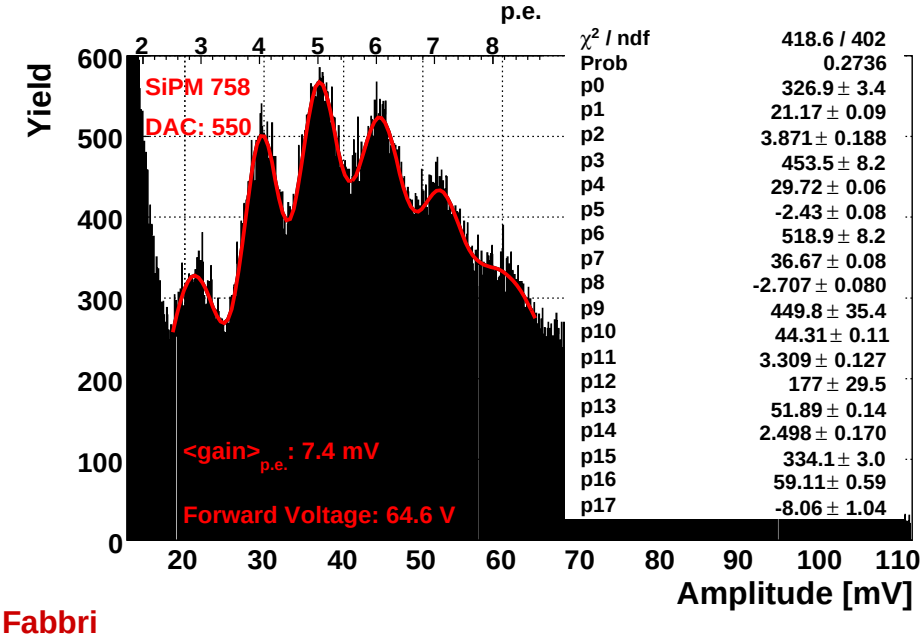
⇒ **To be understood**

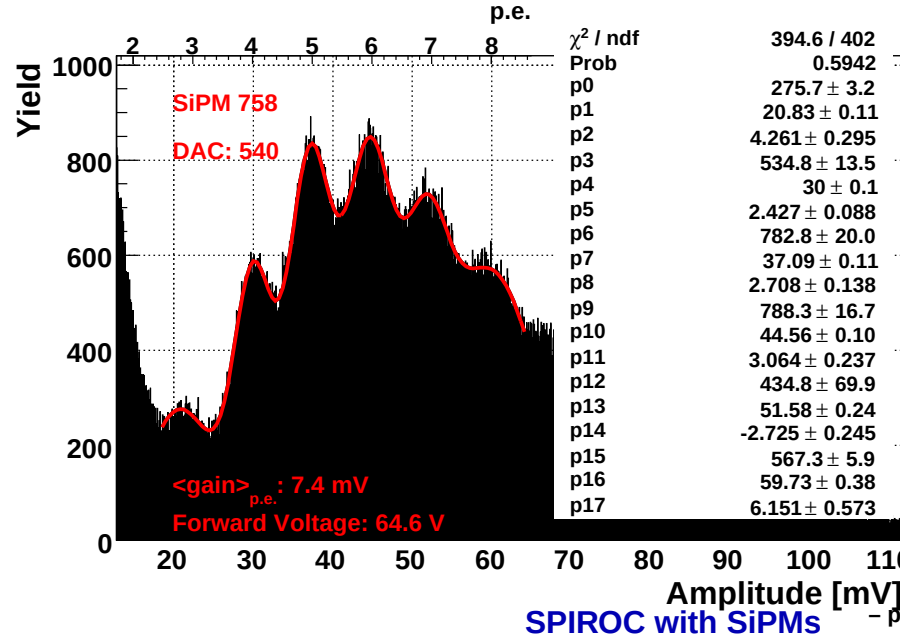
Determination of Trigger Threshold and SiPM Gain

SiPM signal for increasing values of DAC threshold



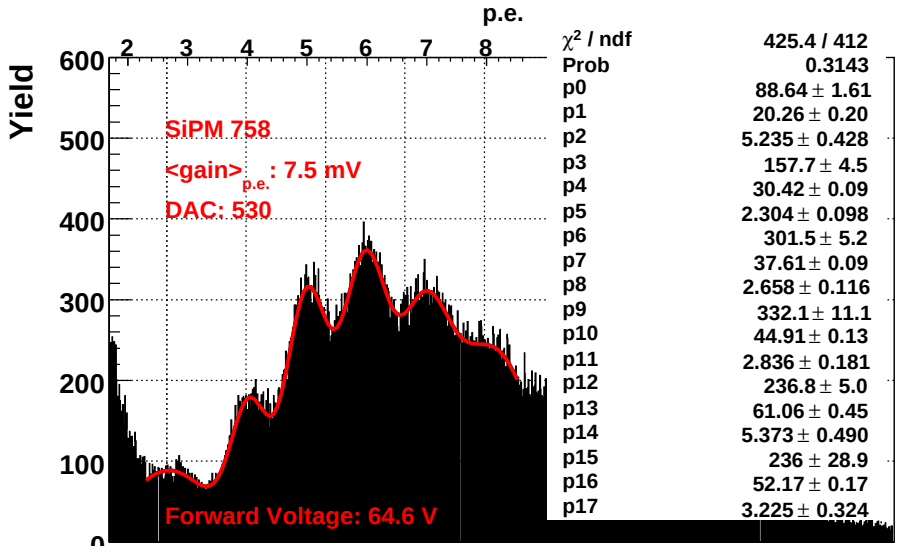


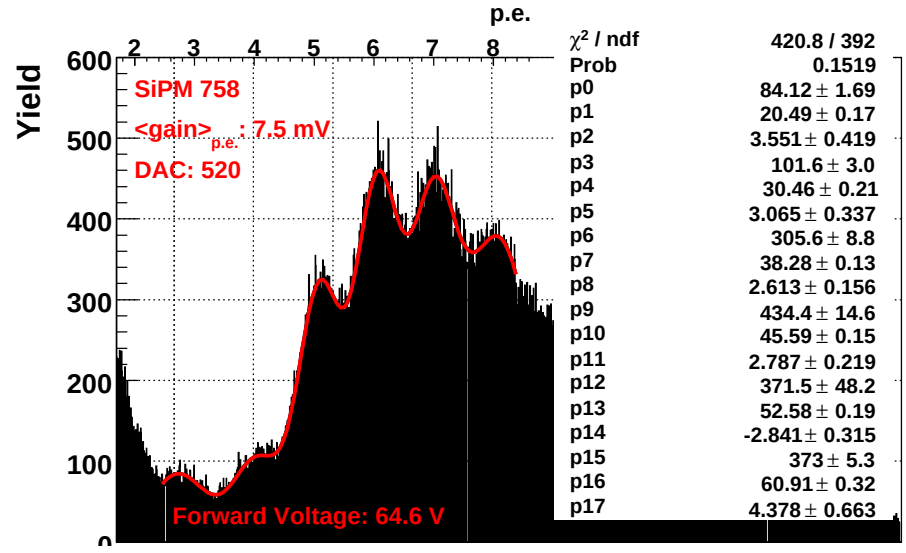


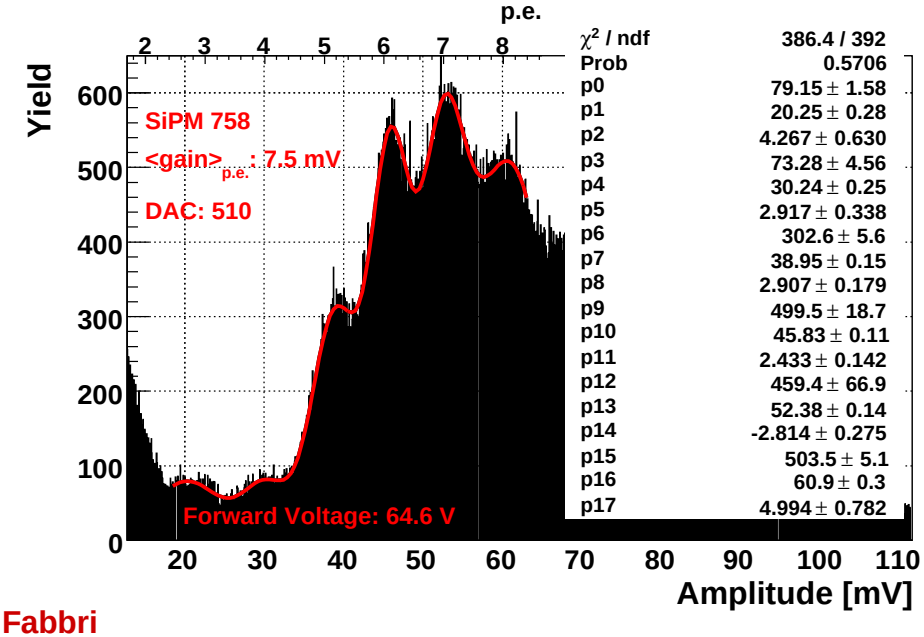


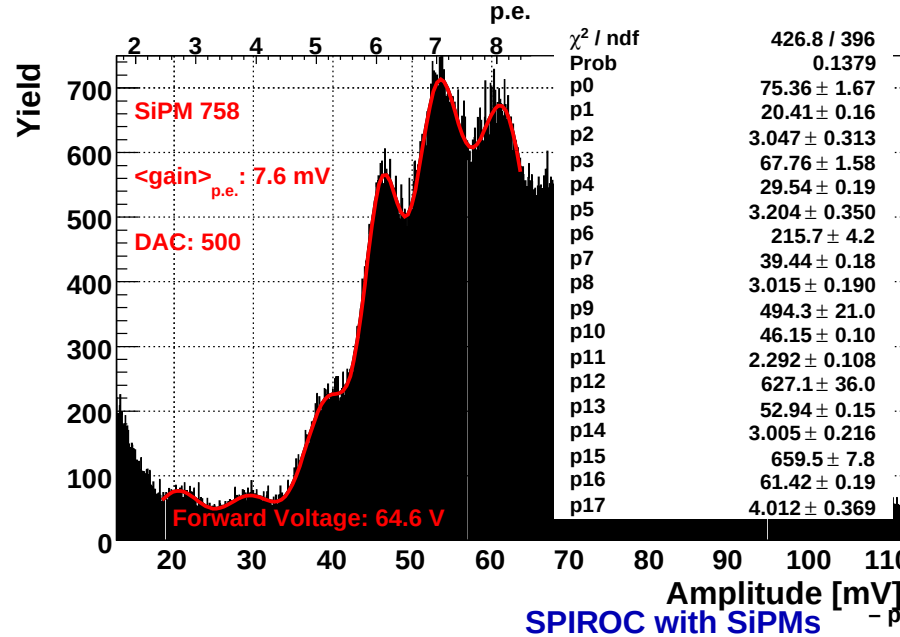
Determination of Trigger Threshold and SiPM Gain

SiPM signal for increasing values of DAC threshold



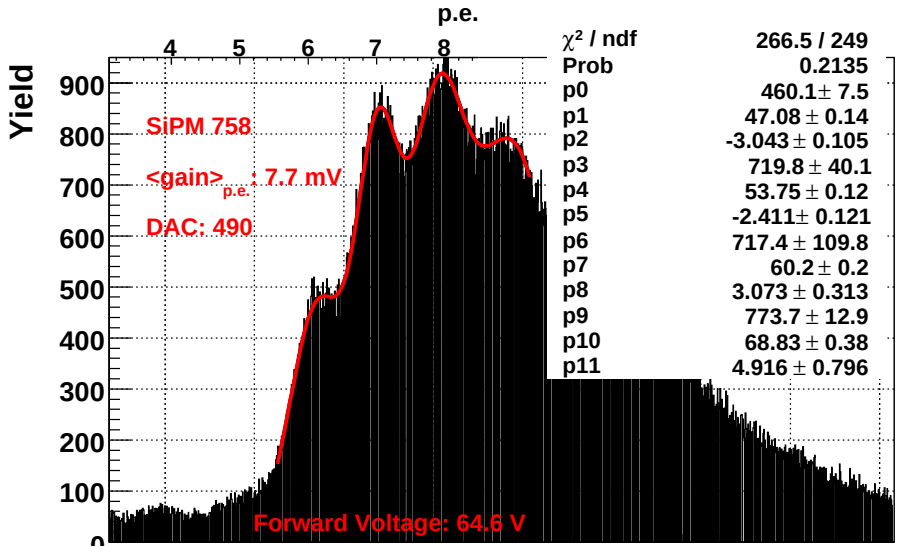


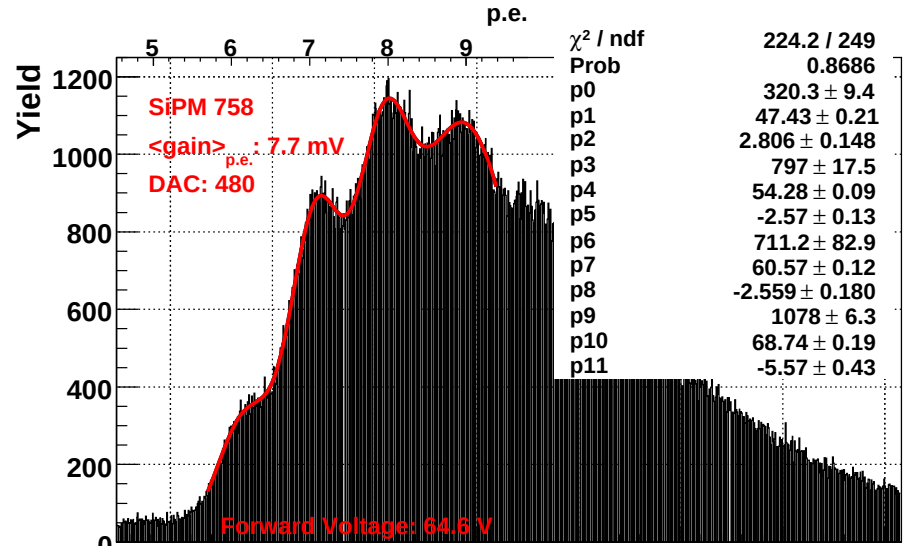


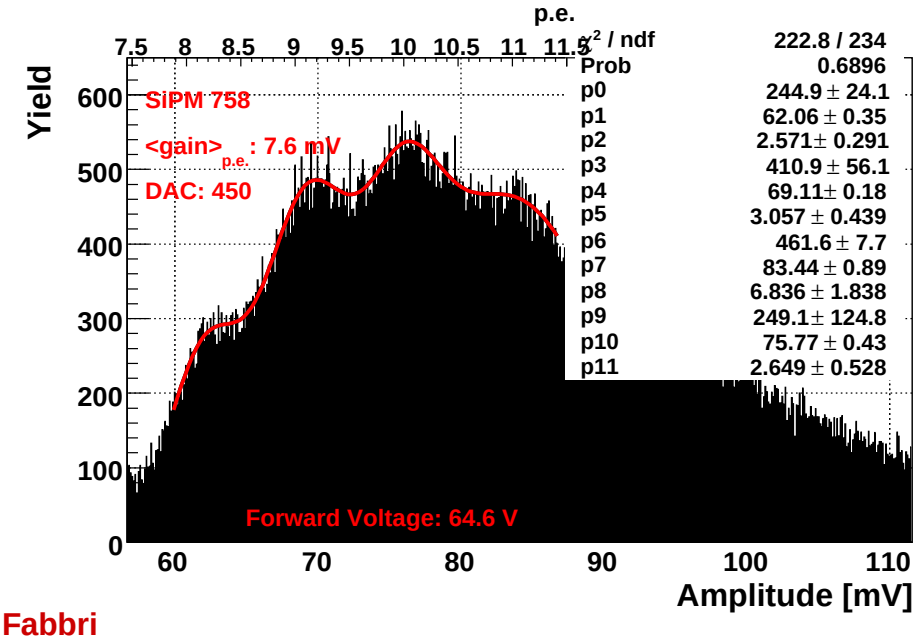


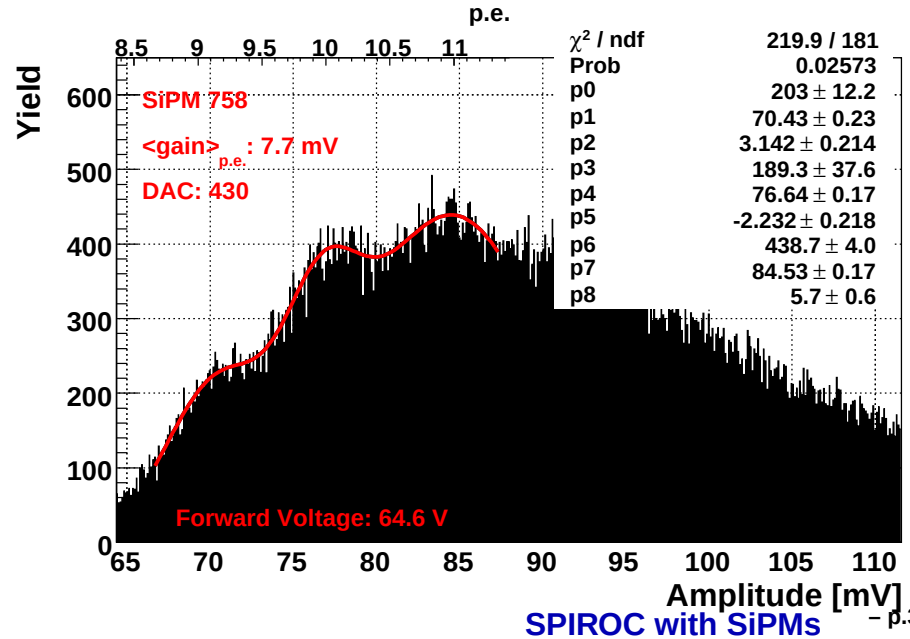
Determination of Trigger Threshold and SiPM Gain

SiPM signal for increasing values of DAC threshold



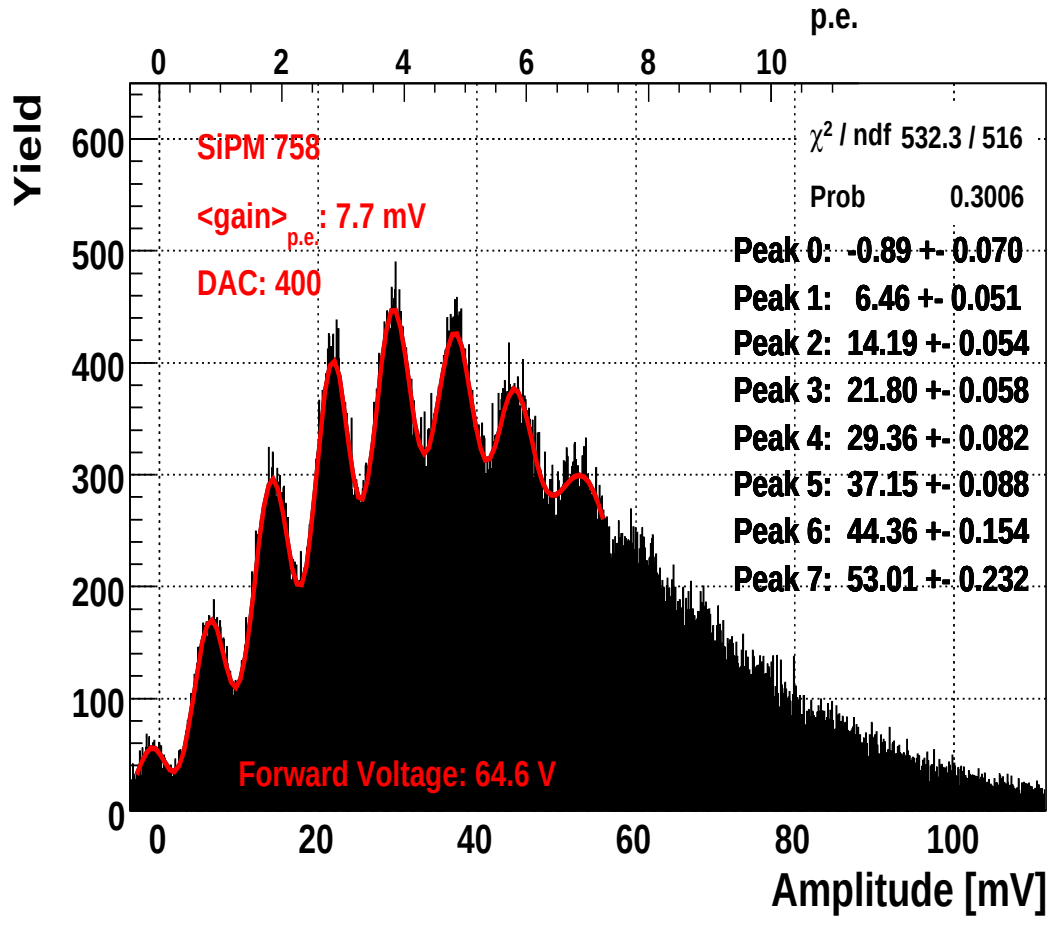






Determination of Trigger Threshold and SiPM Gain

- **SiPM signal with external trigger (for ADC gate and HOLD)**



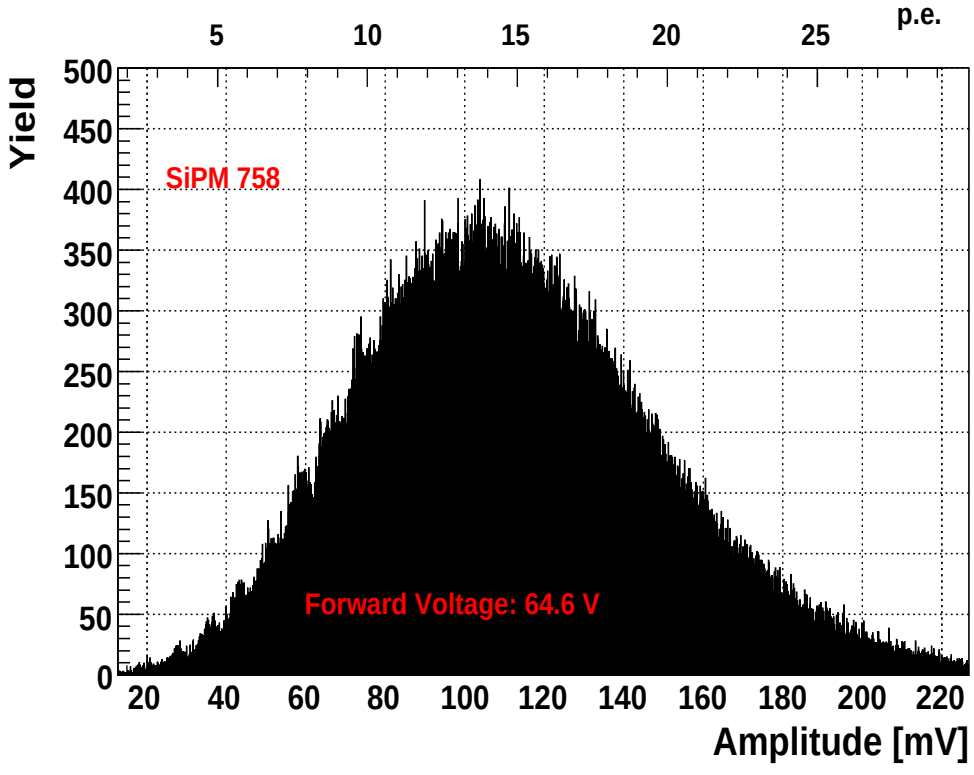
DAC Threshold and SiPM Pixel Suppression

DAC value	Suppressed peak number
530	3
510	4
490	5
470	6
450	7
430	8
410	9
390	10

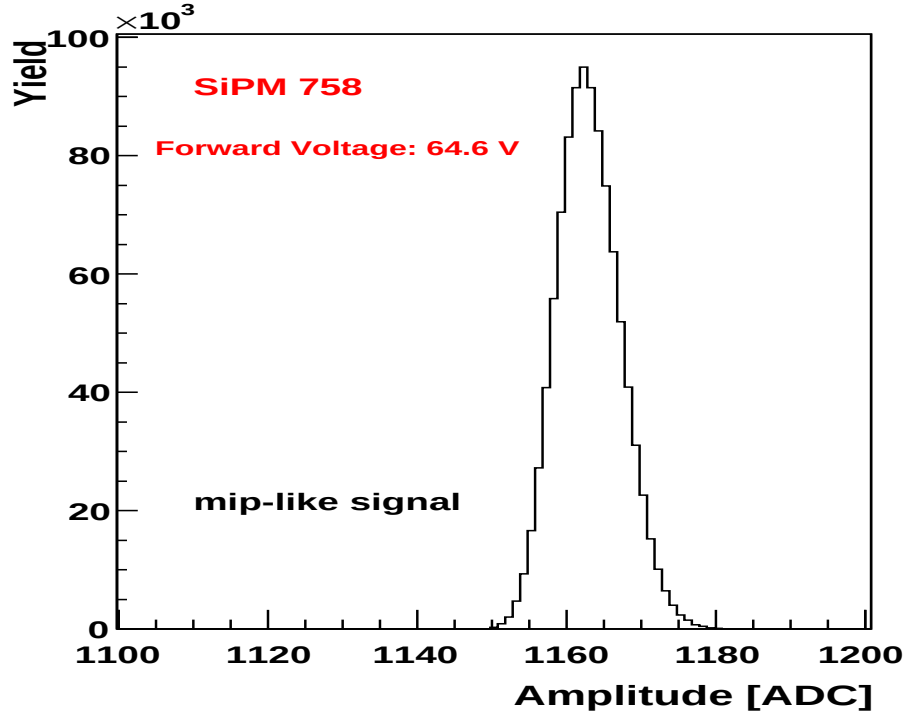
Mip SiPM Signal in High and Low Gain Modes

- **SiPM signal with external trigger (for ADC gate and HOLD)**

High Gain



Low Gain



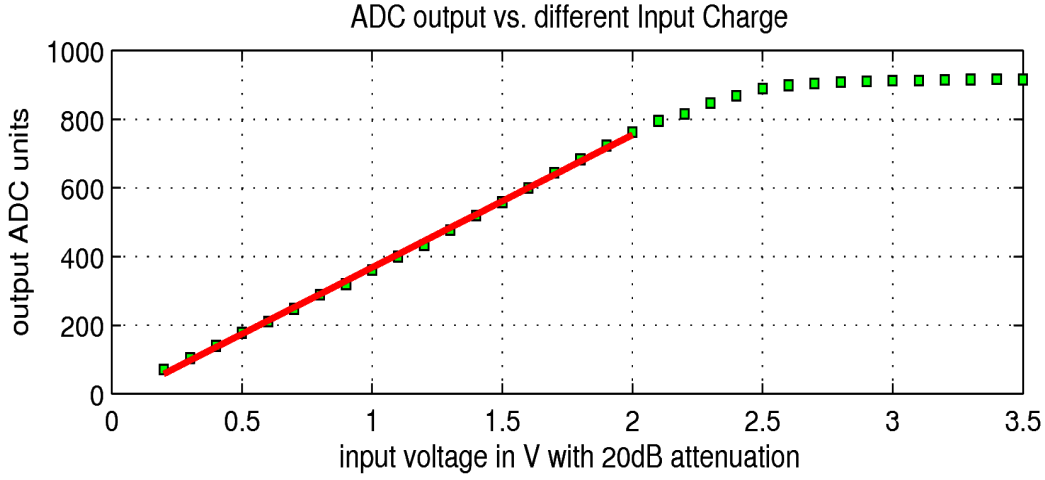
SPIROC II: Outlook

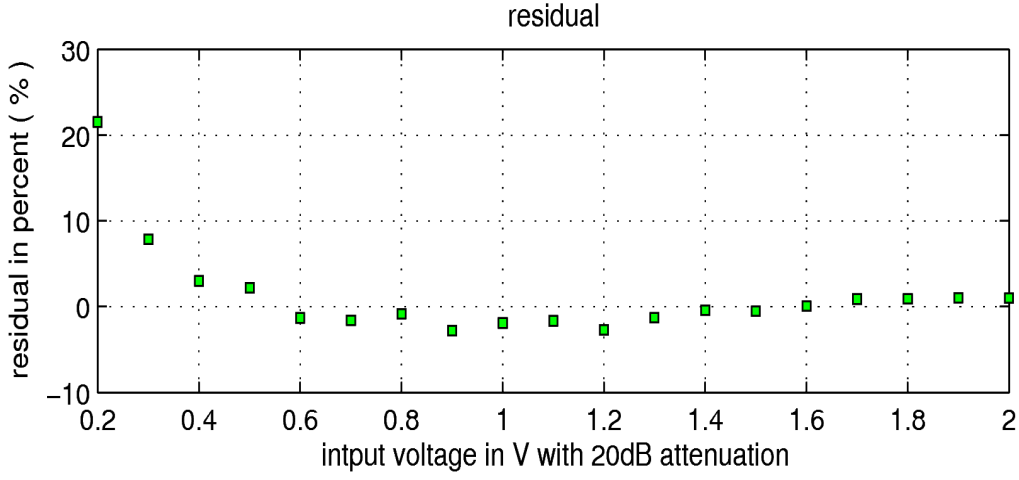
Analysis on going

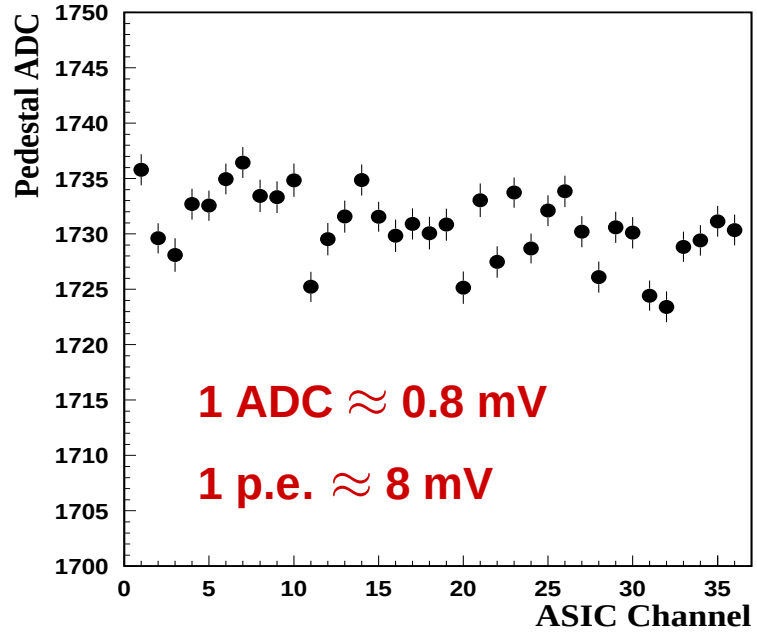
- **Digital part (Internal ADC) not usable in SPIROC I**

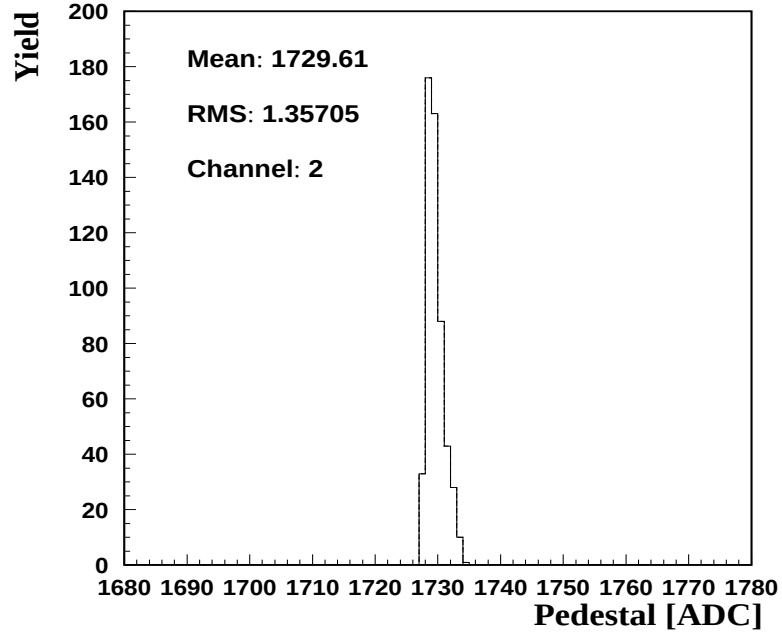
  — now fixed in SPIROC II (delivered this winter)

- **Linearity of Wilkinson ADC can be investigated**









⇒ **Similar behaviour observed with ext ADC**