

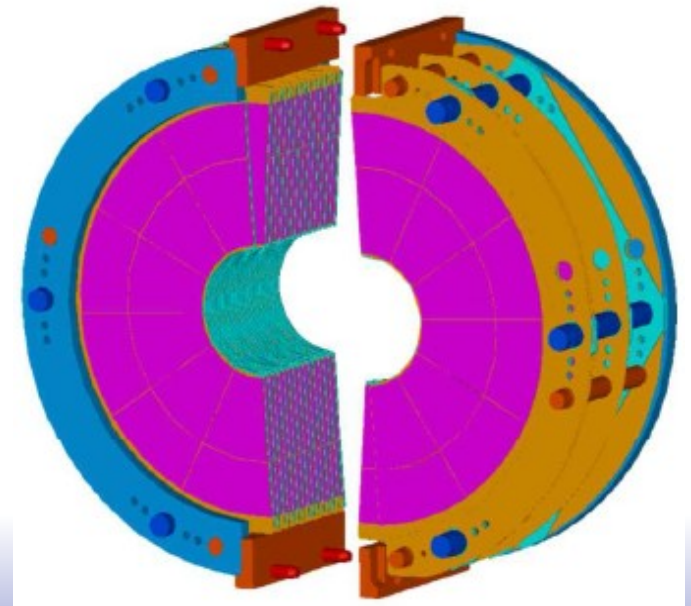
# ***FCAL testbeam preparation***

**Szymon Kulis\*** on behalf of **FCAL** Collaboration

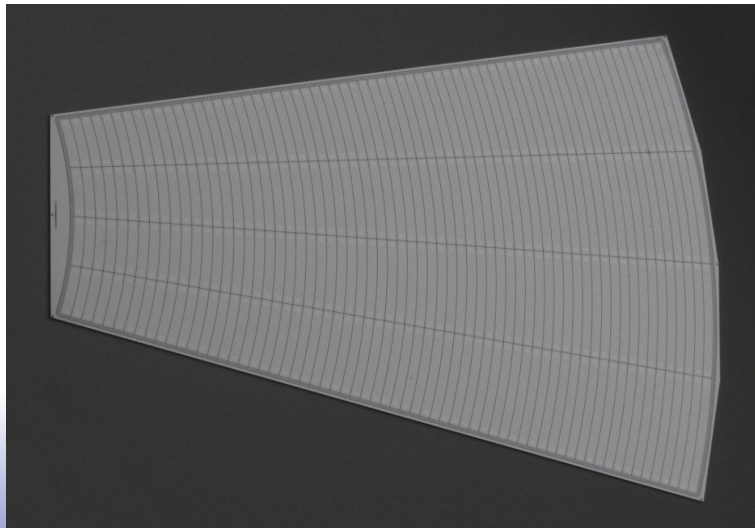
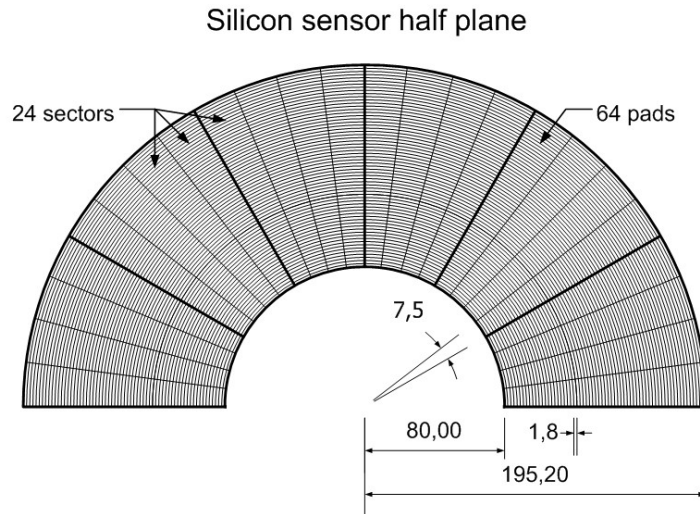
**\*) AGH-UST Kraków**

# Outline

- ❑ Development status
- ❑ Preparation of test setup of the whole readout chain
- ❑ Testbeam plans
- ❑ Summary & plans



# ***Silicon sensors***



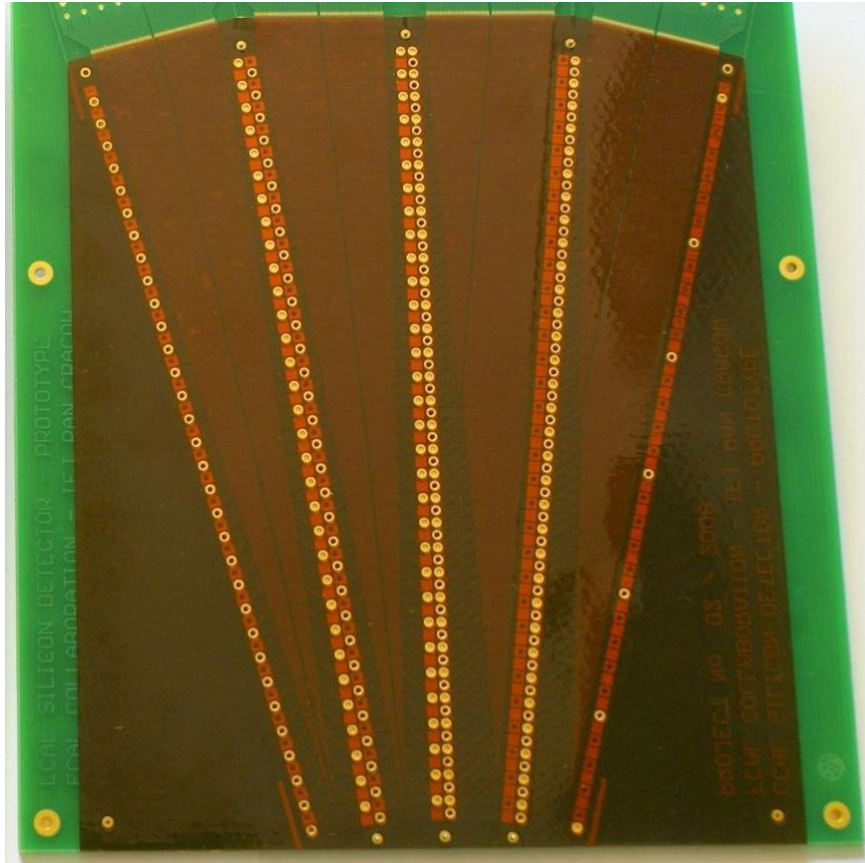
- 48 azimuthal sectors
- 64 radial pads in sector
- Prototypes ( $30^\circ \leftrightarrow 4$  sectors each) from Hamamatsu
- High resistivity n-type Si bulk 320um thick
- P+ pads with Al-metalizaion (DC coupled)

Prototypes produced

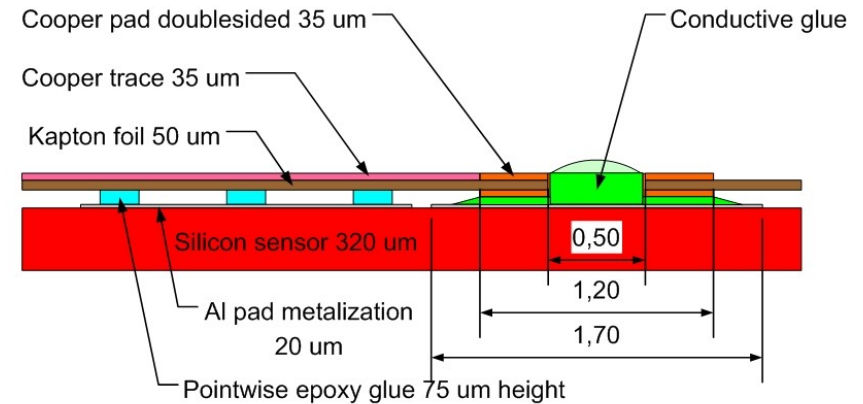
Electrical parameters checked

Tests with particles needed

# *Captan fanout*

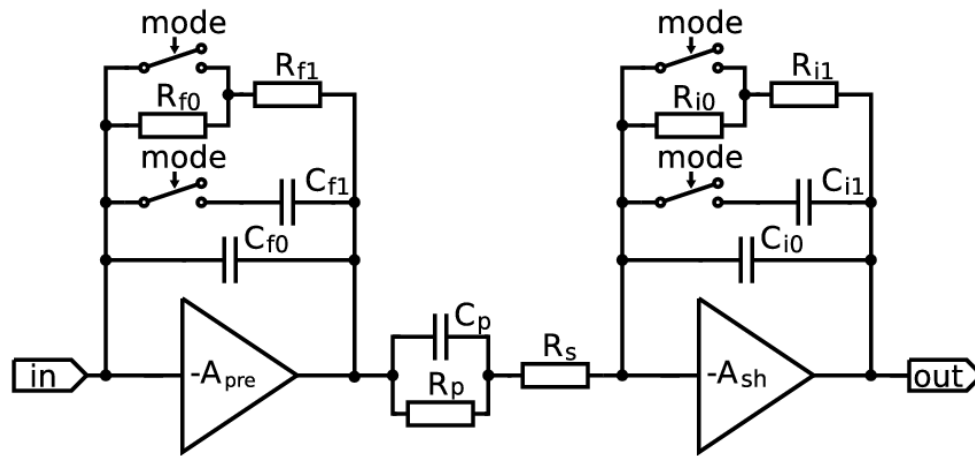


- 50um thick
- Two slightly different types of fanout produced
- Will be glued to sensors

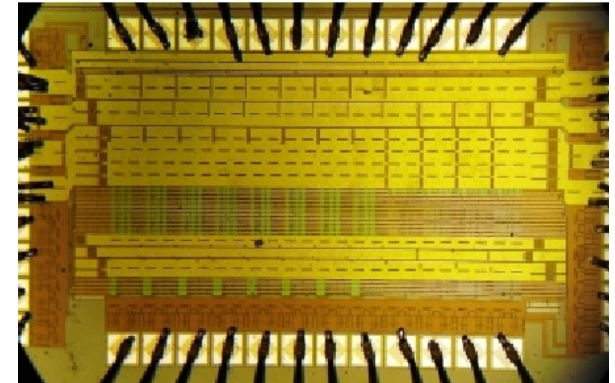


First prototypes produced

# Front-end electronics



- ❑ Charge amplifier
- ❑ Pole zero cancellation
- ❑ 1<sup>st</sup> order shaping
- ❑ Fabricated in AMS 0.35μm



## Specifications:

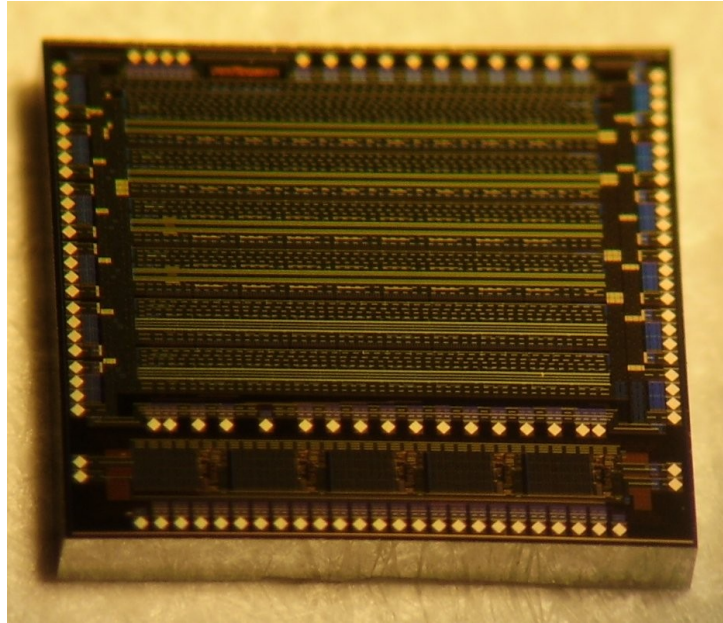
- $C_{det} = 10 - 100 \text{ pF}$
- $T_{peak} \sim 60 \text{ ns}$
- Variable gain:  
physics and calibration mode
- $Q_{max} \sim 10 \text{ pC}$
- Calibration mode:  $S/N > 10$  for MIP

8 channels prototype produced  
measurements agree with simulations

Tests with sensor needed



# ***10 bit pipeline ADC***



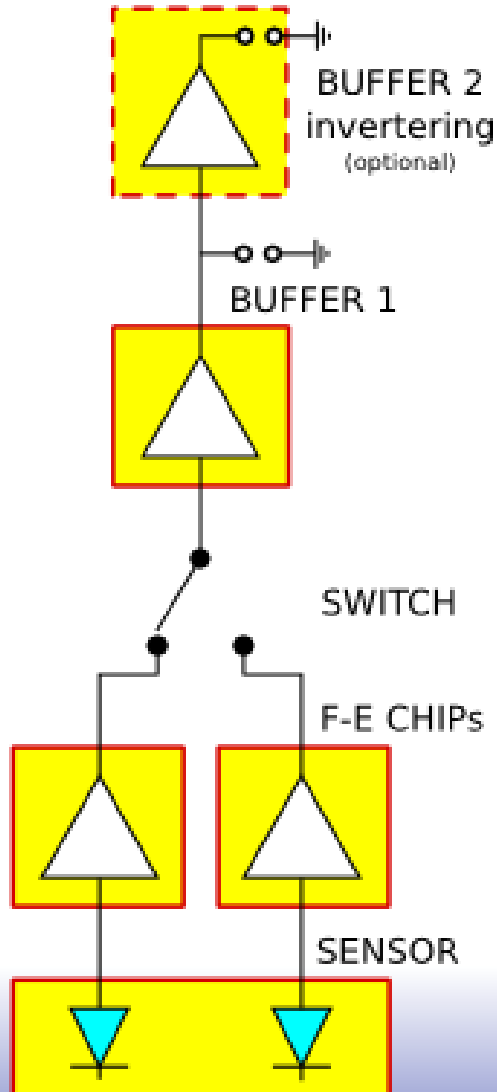
Prototype ADC channels with  
and without S/H fabricated in  
AMS 0.35  $\mu\text{m}$  technology

- ❑ Pipeline architecture (fully differential)  
power efficient & small area
- ❑ 10 bits resolution (1.5 bit per stage)
- ❑ Input dynamic range 2 V
- ❑ Maximum sampling rate  $\sim 30$  MHz
- ❑  $\text{DNL} < 0.5 \text{ LSB}$ ,  $\text{INL} < 1 \text{ LSB}$
- ❑ Multi channel version should be ready  
in few months (beginning of 2010)

single channel prototypes produced  
measurements agree with simulations

More measurements needed

# ***Preparation of sensor-readout electronics test-setup chain***



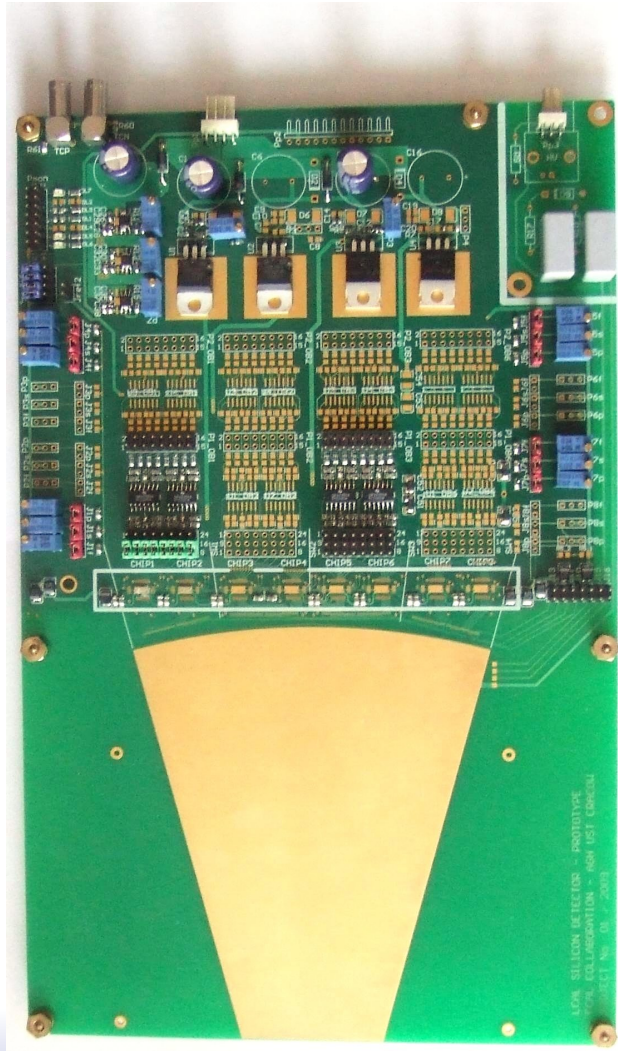
## □ Setup includes:

- Sensor
- Capton fanout
- Dedicated PCB
- Front-end ASICs
- Output buffers  
(to drive long wires)

## □ No ADC on board

(NO multichannel ADC yet)

# ***Readout chain test setup***



- ❑ Up to 8 front-end ASIC (64 channels)
- ❑ Two types of fanout can be tested
- ❑ All needed biasing and power supply included
- ❑ Buffered analogue outputs

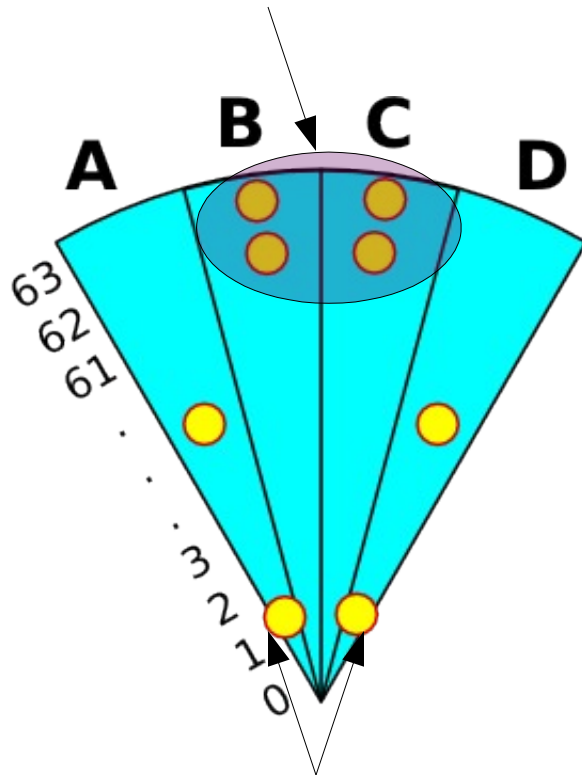
PCB produced and partially assembled

Assembly needs to be completed...  
Readout chain needs to be tested...



# ***Preparation of testbeam***

testbeam area ?

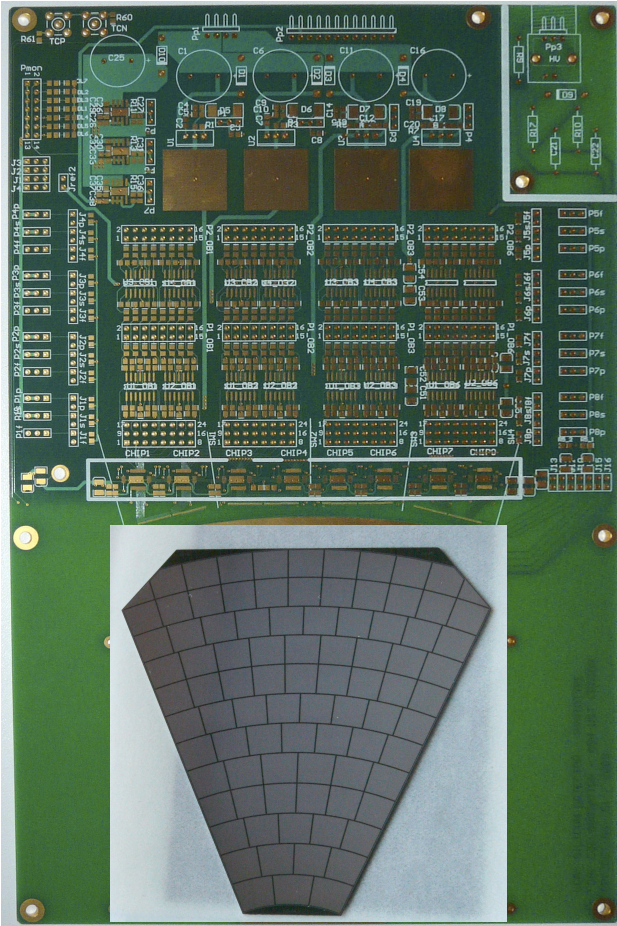


Each yellow dot means :  
1 ASIC (8 channels)

- ❑ Same setup is going to be used for testbeam – PCB board designed to be used also in testbeam
- ❑ Up to 32 readout channels can be read at the same time
- ❑ External multichannel ADC has to be used
  - VME – V1740 will be used
  - Work on software has started
- ❑ External trigger (Eudet telescope ?)

The whole readout chain needs to be checked first...

# ***Preparation of testbeam...***



# *Status & Plans*

- |   |            |                        |
|---|------------|------------------------|
| ❑ Sensors                                       | READY      |                        |
| ❑ Capton fanout                                 | READY      |                        |
| ❑ 8 channel front-end ASIC                      | READY      |                        |
| ❑ Single channel ADC ASIC                       | READY      |                        |
| ❑ Dedicated PCB                                 | READY      |                        |
| ❑ Parametrization of setup                      | IN ROGRESS | ~ Jan.2010             |
| ❑ Multichannel ADC ASIC                         | IN ROGRESS | ~ Dec.2009(submission) |
| ❑ <b>Test beam planed in the middle of 2010</b> |            |                        |