

# SPIDER CHERWELL

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- ◇ Future plans
- ◇ Wishlist

J.J. Velthuis  
for the

**SPIDER collaboration**

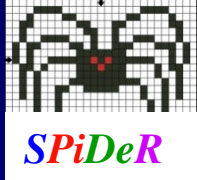
Jaap Velthuis, University of Bristol



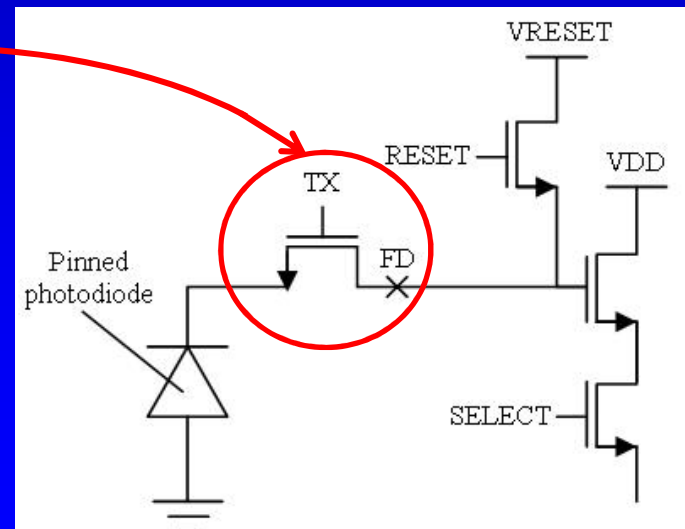
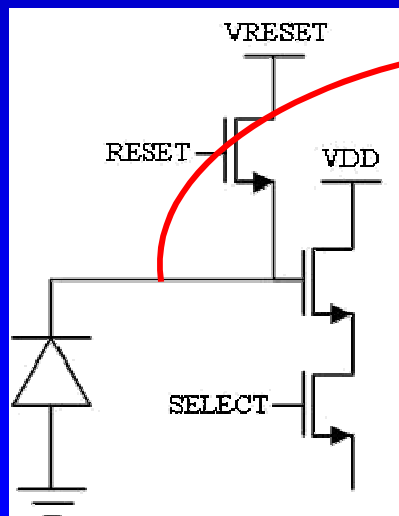
# SPIDER

- ♦ UK Collaboration working on Silicon Pixel R&D for future colliders.
  - Demonstrate a new improved technique for calorimetry
  - Develop a MAPS sensor with in-pixel data processing for tracking applications
- ♦ In principle funded until end of 2012

# FORTIS



- ♦ FORTIS is the first 4T MAPS for Particle Physics
  - 3T CMOS
    - ♦ Simple architecture
    - ♦ Readout and charge collection area are the same
  - 4T CMOS
    - ♦ Three additional elements
    - ♦ Readout and charge collection area are at different points



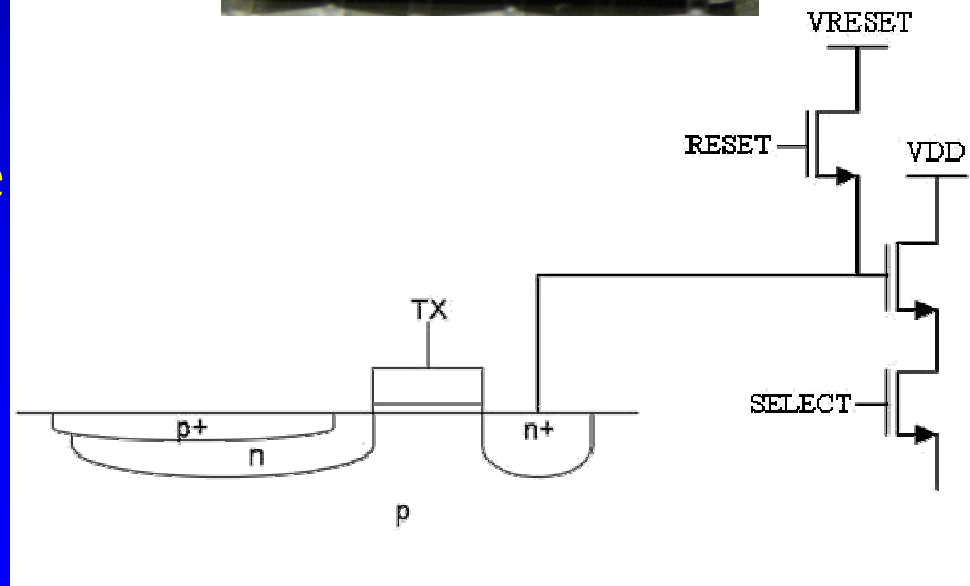
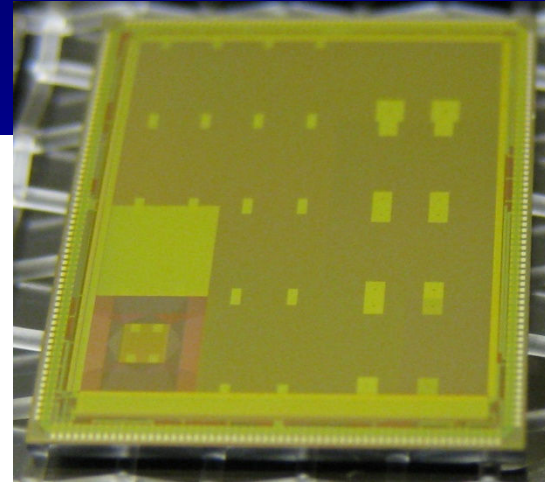
# 4T Pixel Advantages

## ♦ Low Noise

- readout node separated from charge collection area
- The reset noise and fixed pattern noise (FPN) can be removed by in-pixel correlated double sampling (CDS)

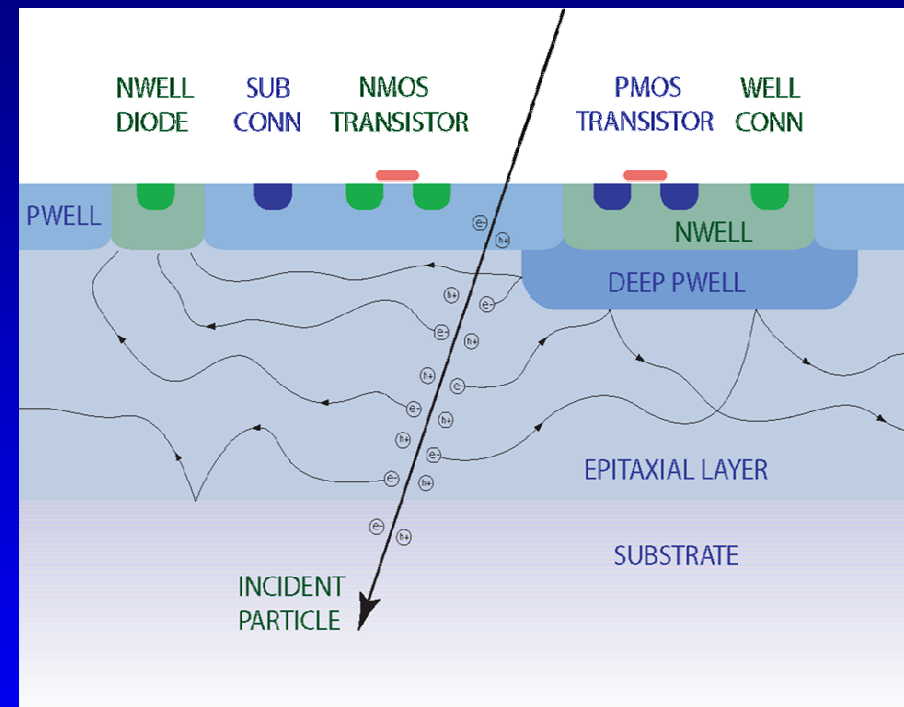
## ♦ High Conversion Gain

- Charge is collected on large diode then transferred to the floating diffusion
- Large  $C$  gives fast and complete charge collection
- Small  $C$  yields large gain

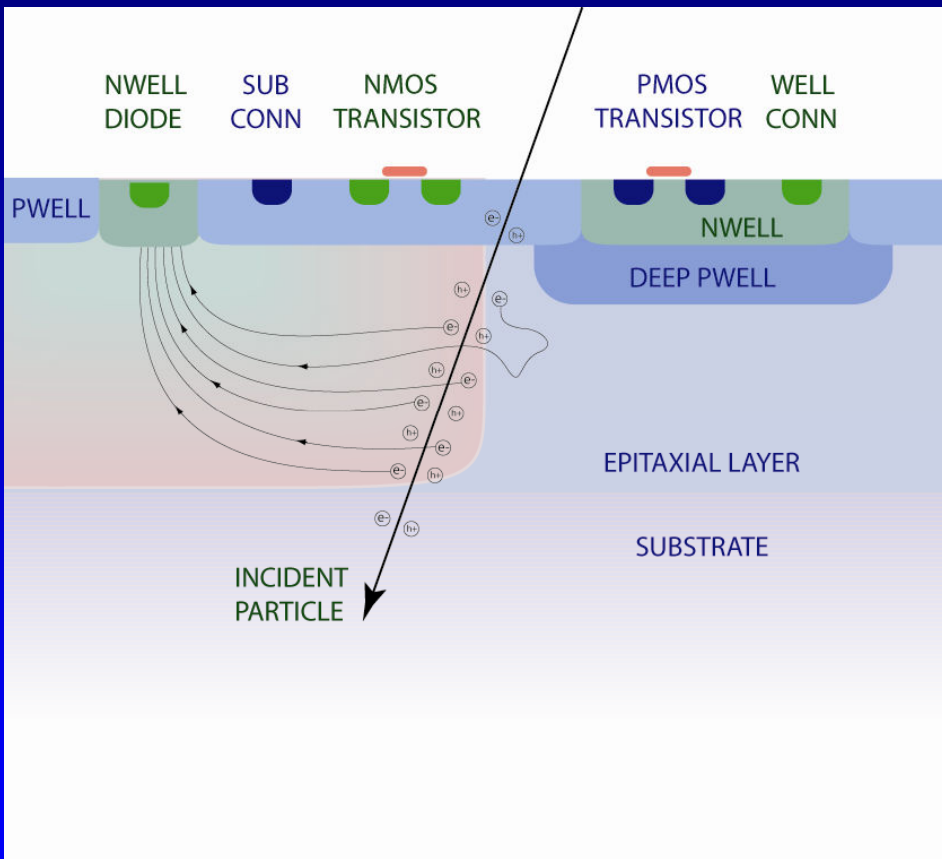


# Deep Pwell

- ♦ Problem in MAPS:
  - PMOS electronics need Nwell
  - Nwell acts as charge collection diode
  - So can't make PMOS without losing huge amount of  $Q$
- ♦ New development: make deep pwell with Nwell inside
  - can do CMOS
  - Road to data processing in pixel
- ♦ Some FORTIS have empty deep pwell to test effect of  $Q$  collection

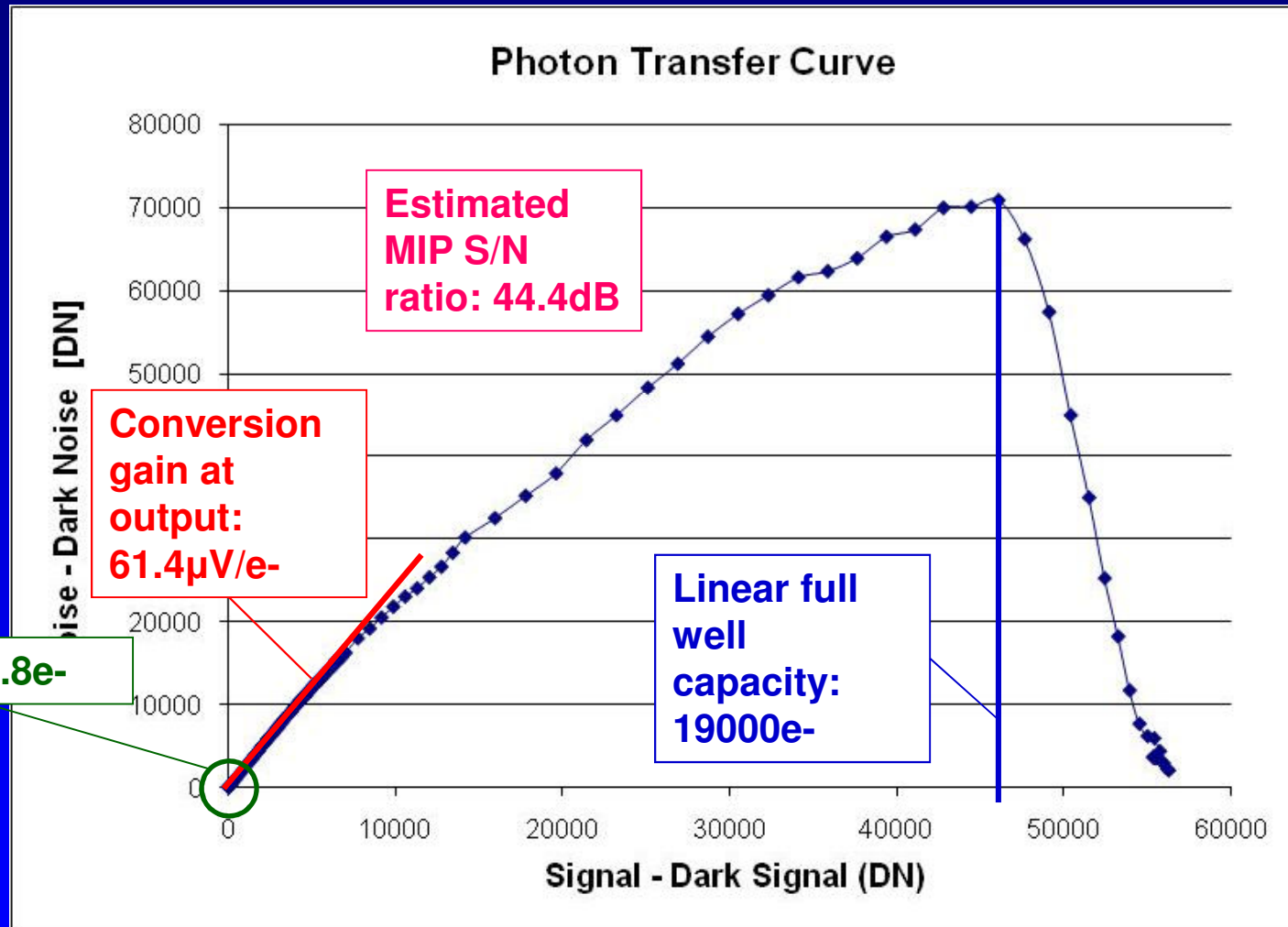


# Substrate Resistivity

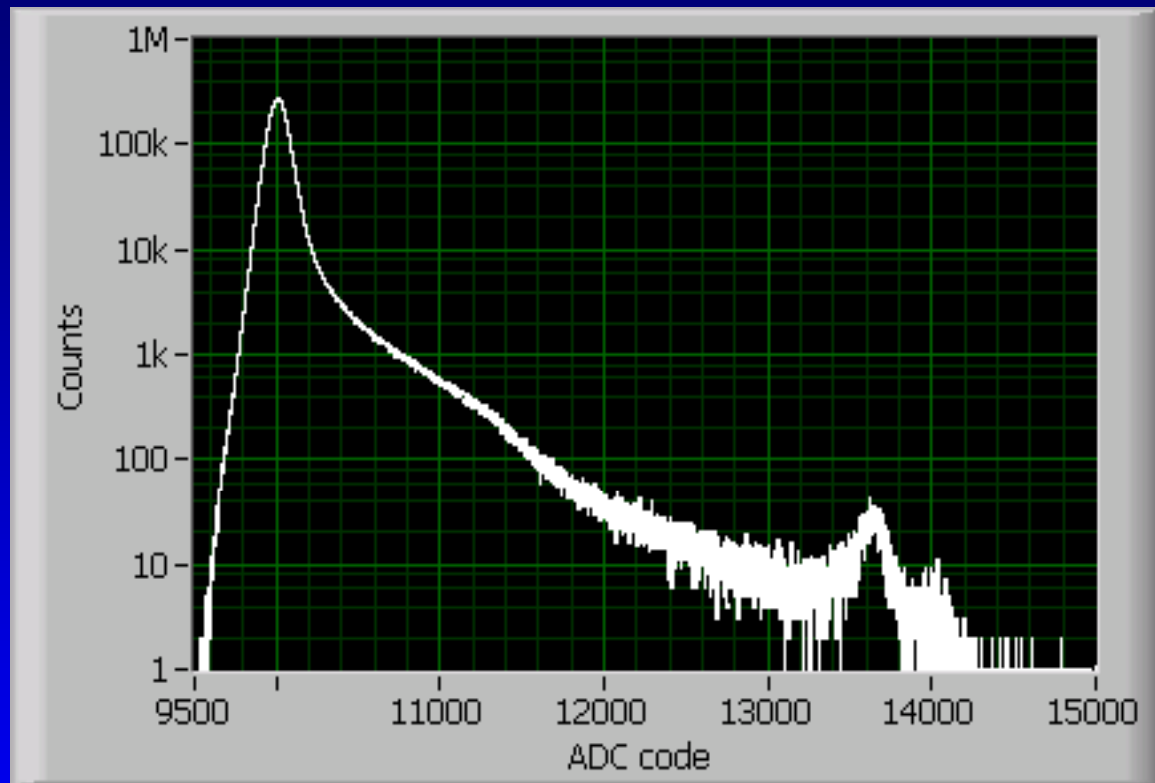


- ❖ High resistivity (intrinsic) silicon enlarges the depletion region to fully occupy the pixel
  - Majority of deposited charge now falls in a depletion region and is collected by electric field
  - Improved charge collection efficiency
  - Faster charge collection (drift vs diffusion)
- ❖ Some FORTIS have high res

# FORTIS Results



# FORTIS results

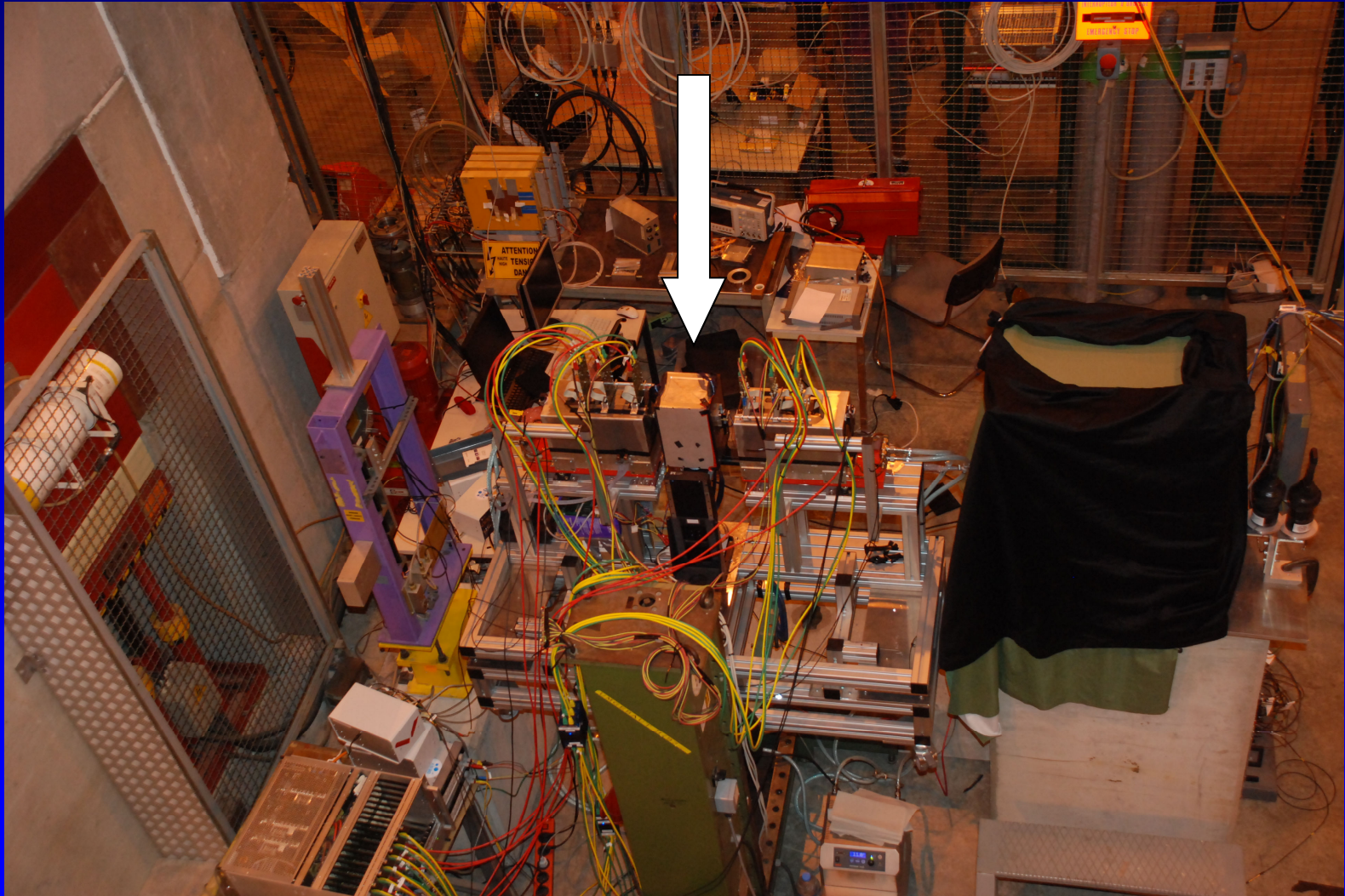


## ♦ $^{55}\text{Fe}$ Photons (preliminary)

- Conversion gain =  $56 \mu\text{V}/e^-$
- Noise (from dark fwhm) =  $7.7e^-$

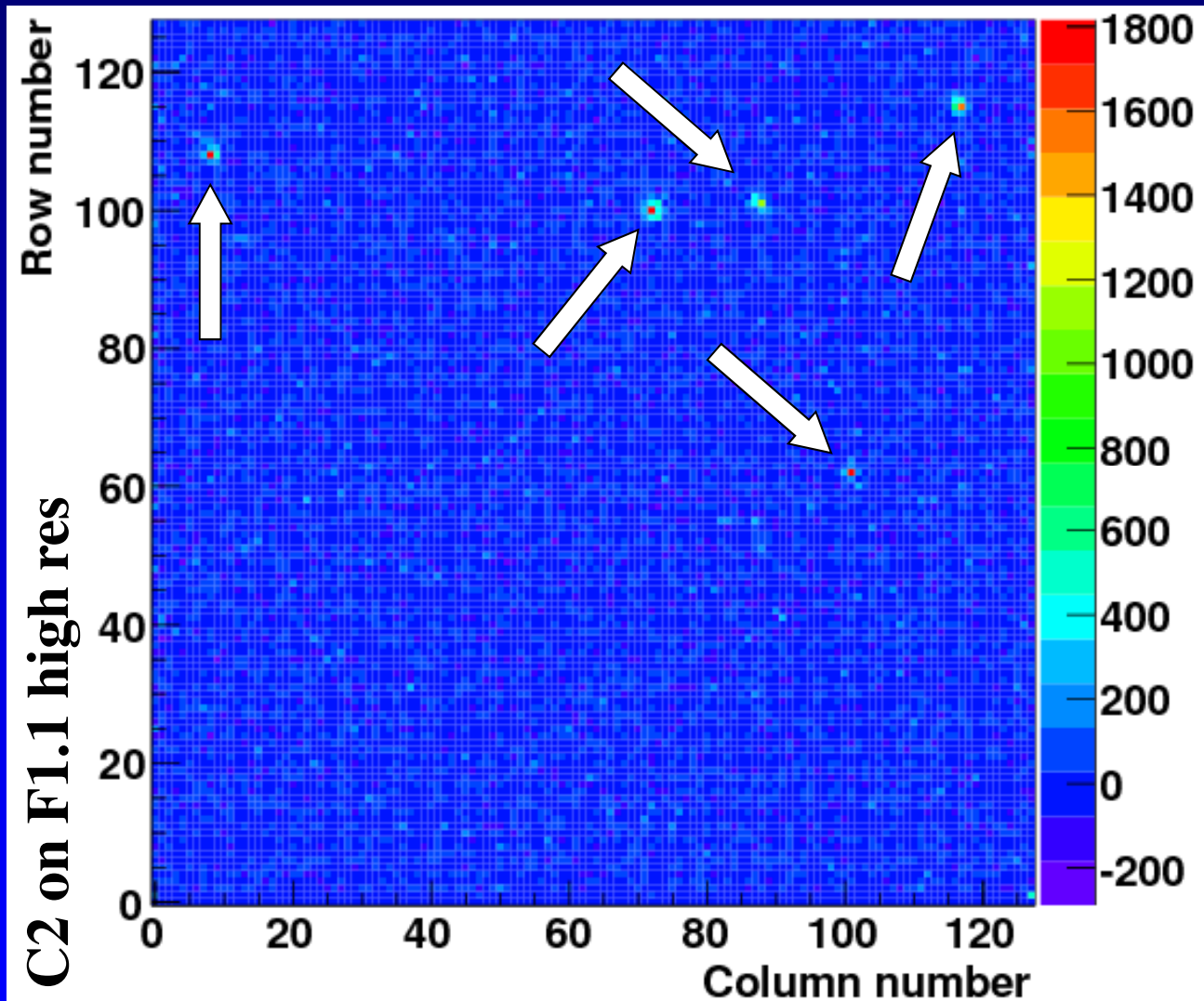


# Some test beam pictures

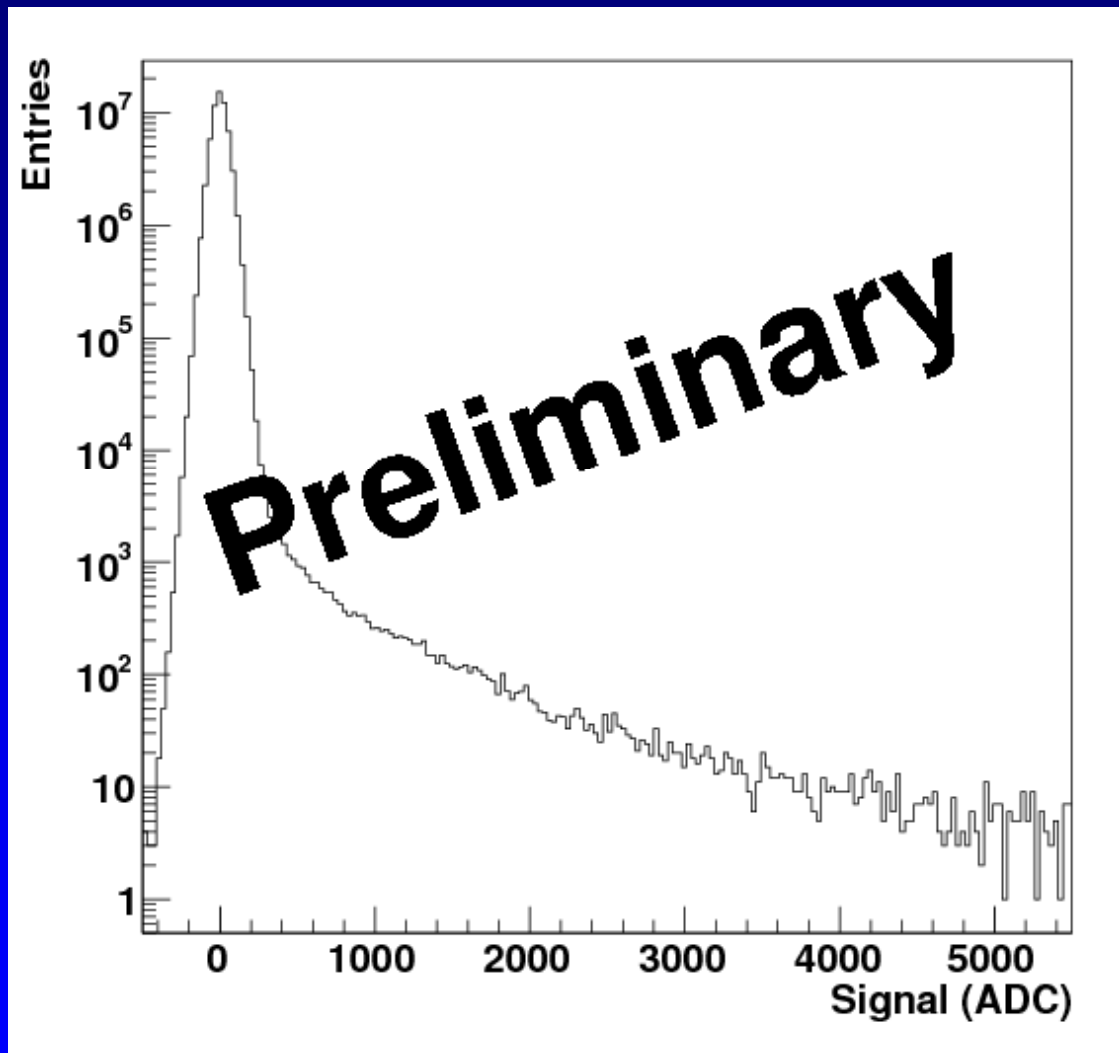


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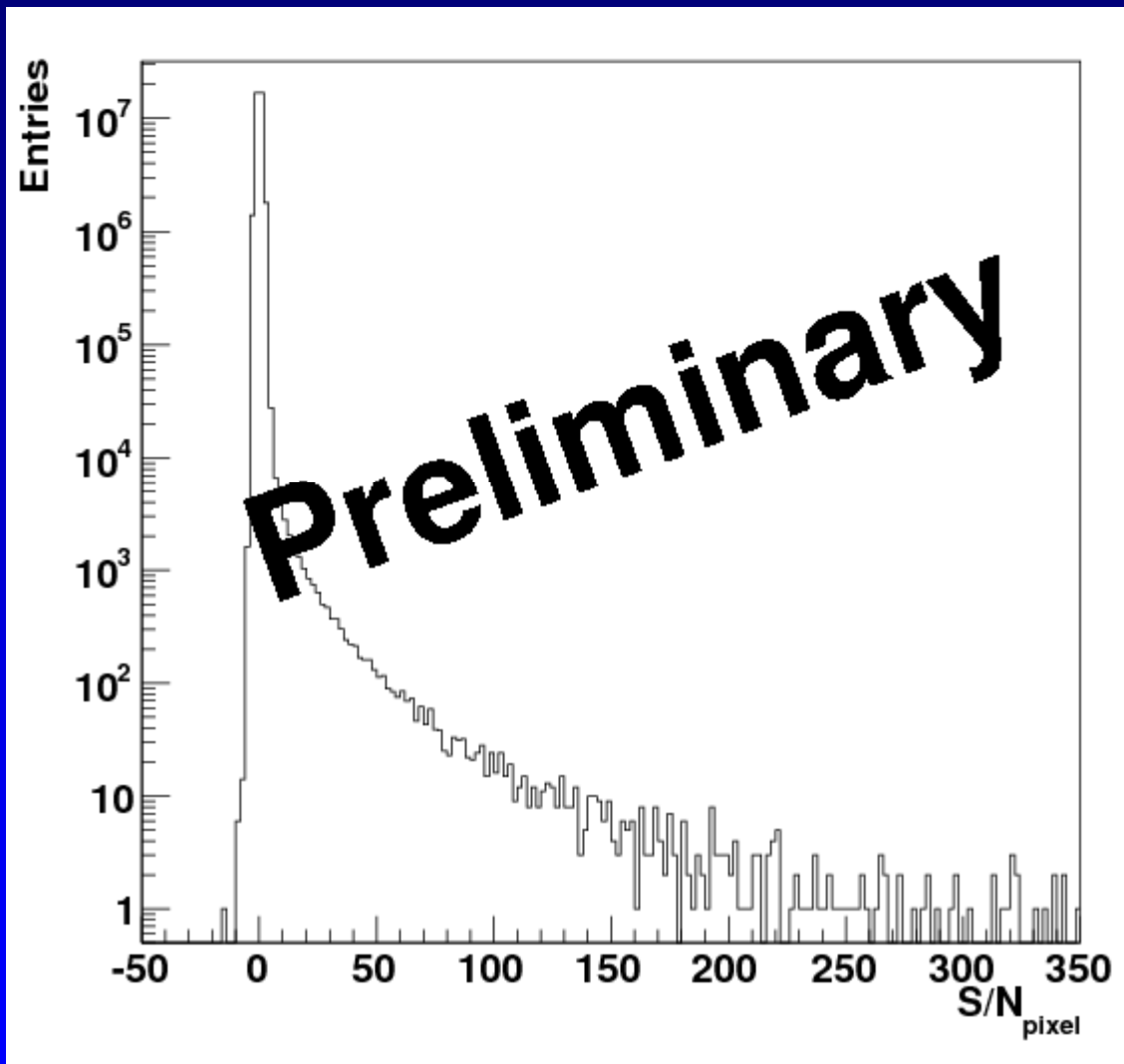
We see hits...



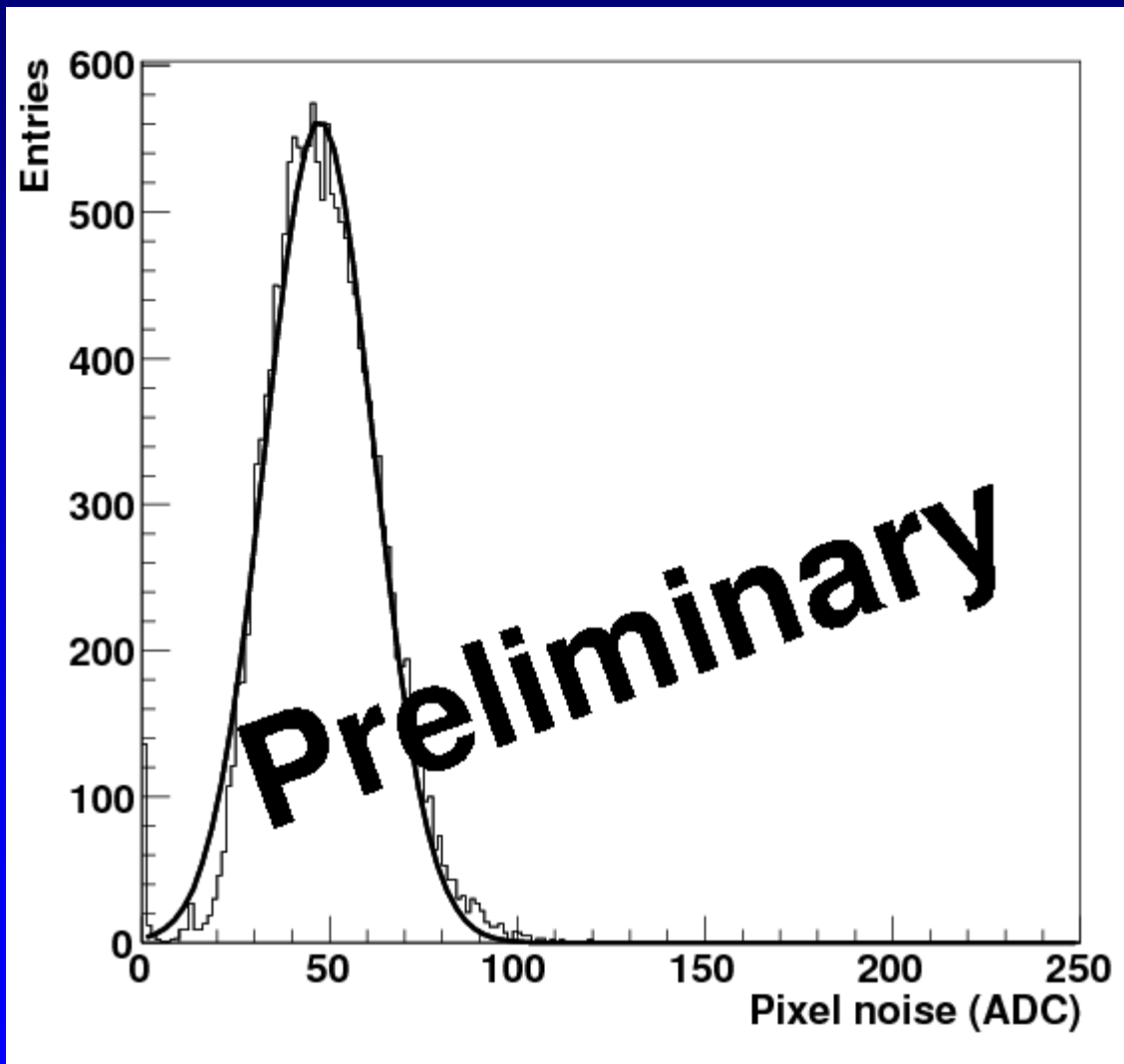
# Raw signals



# Raw S/N for each pixel

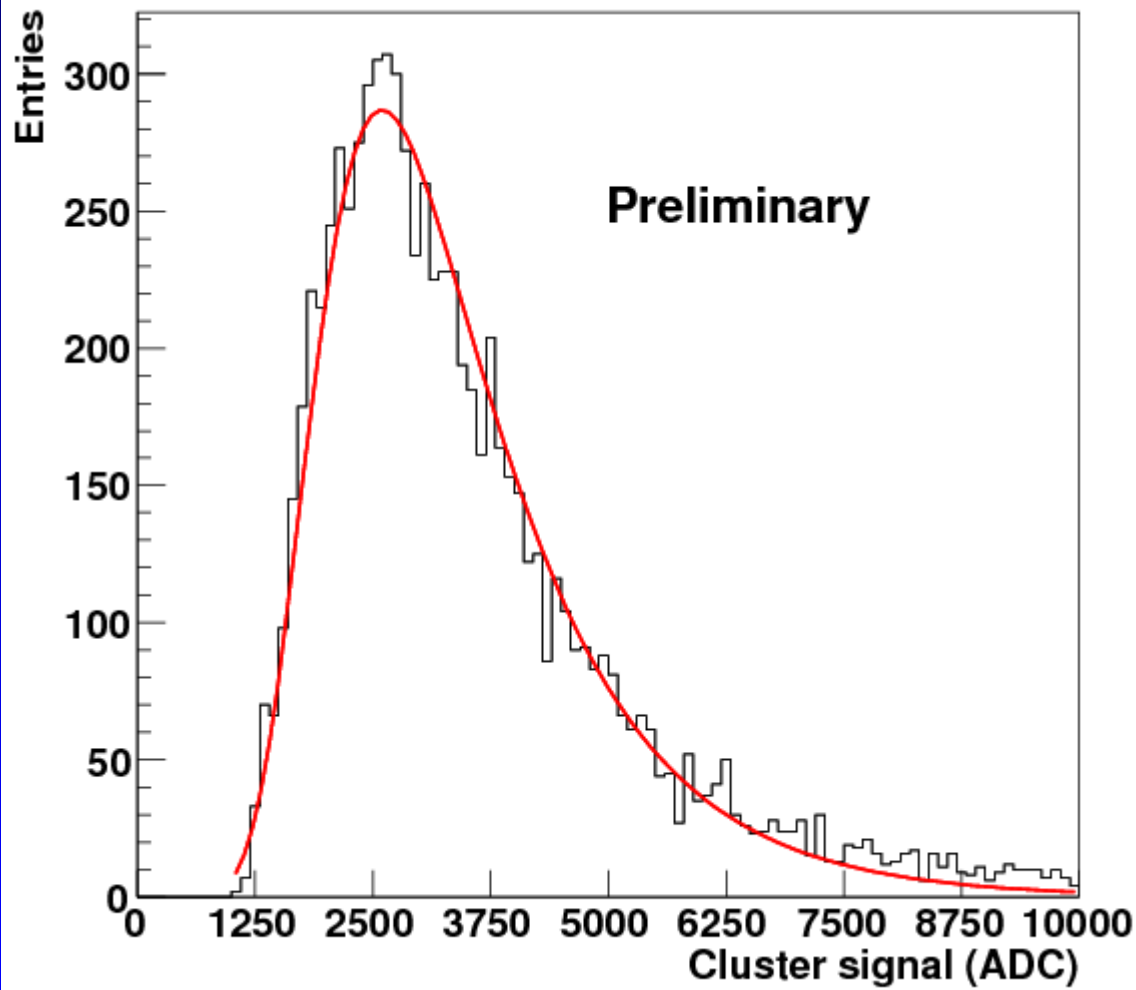


# Pixel Noise



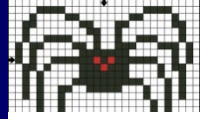


# Cluster signal

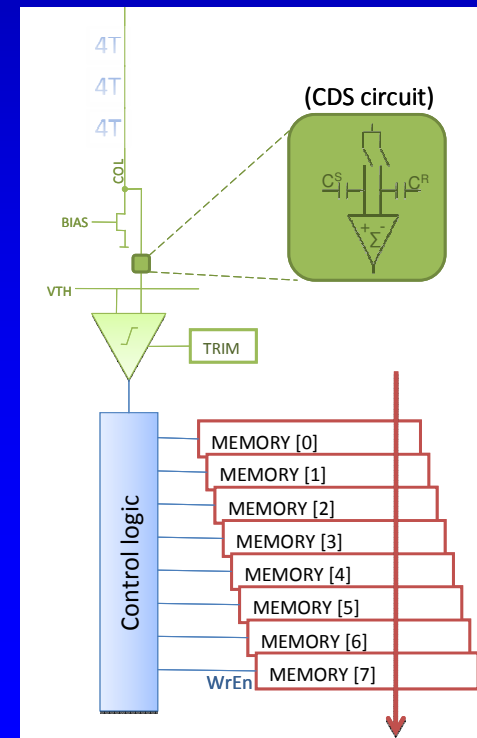
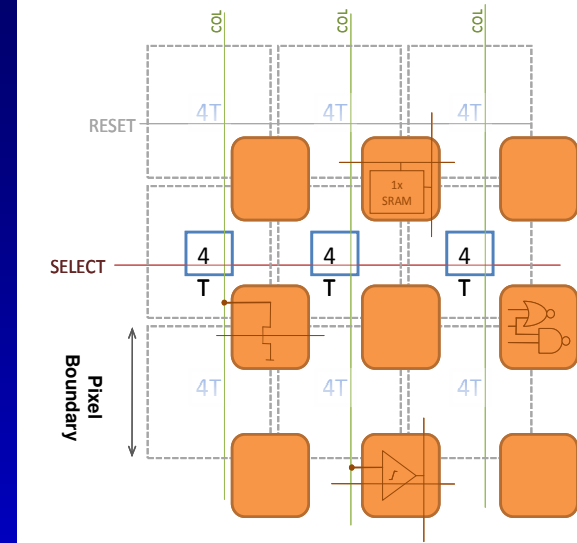


- ◇ Corresponds to  $S/N \sim 50$
- ◇ Data analysis just started
- ◇ Still need to match up with telescope

# The future: Cherwell



- ♦ Uses INMAPS plus 4T to achieve
  - 100% fill factor with integrated sensor and readout electronics
  - ♦ Incorporation of complex logic within a pixel
  - ♦ Investigation of data reduction/clustering
- Low noise using transfer gate, CDS and in-pixel amplification
- Low power using rolling shutter readout
- Combine 128 pixels in 1 strixel



# Future plans

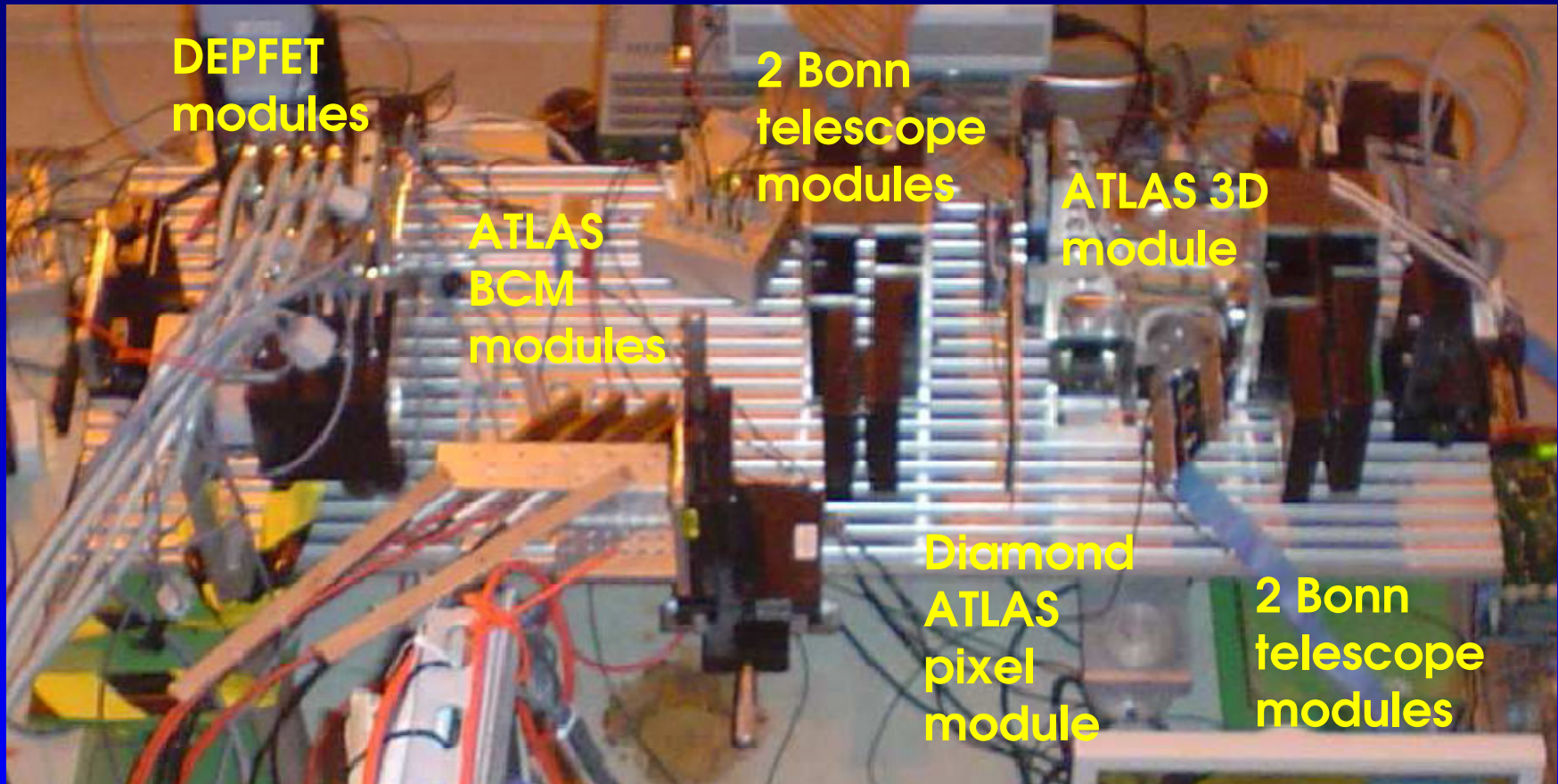
- ♦ Cherwell1 will be submitted in spring
  - Tests using sources & laser; no beam test
- ♦ Cherwell2 will be submitted beginning 2012
  - Cherwell2 will be extensively tested
  - 3 week beam test at CERN with high momentum pions



# Our needs/wishes

- ♦ Beam time!
- ♦ Need telescope
  - Really like EUDET concept:
    - ♦ Know the TLU; no big interfacing problems to be solved onsite
    - ♦ Tracking and alignment software provided
    - ♦ Essentially get the tracks
- ♦ Would like patch panels (bnc and fiber optic) between hut and area
  - Cabling is pain
- ♦ Would like large XY-stage
- ♦ Would like cooling option
- ♦ If possible could arrange many user beam tests
  - Remote shifts; saves lots of travel money

# Nice example



- ♦ Tested 4 different devices at the same time
  - Currently only possible because 1 institute + friendly colleagues

# Summary

- ♦ SPIDER is developing a novel tracking device based on MAPS with in-pixel data processing
- ♦ Two iterations. Final chip will be delivered in summer 2012.
- ♦ Would be great to have common infrastructure: patch panels, large XY stage, cooling & TLU
- ♦ Very interested in collaborating with many other users