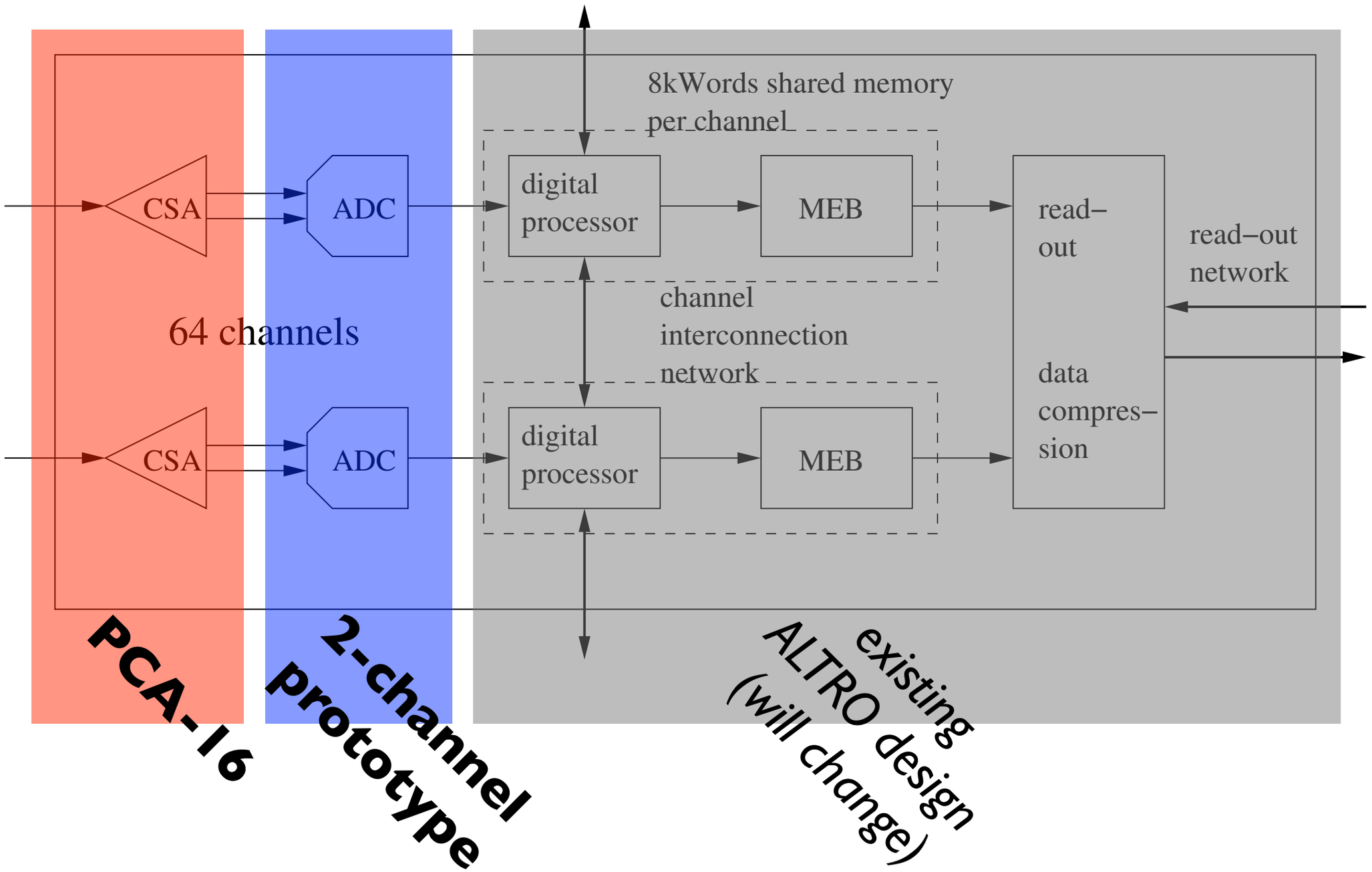
S-ALTRO

Summary of prototypes and design plans

Outline

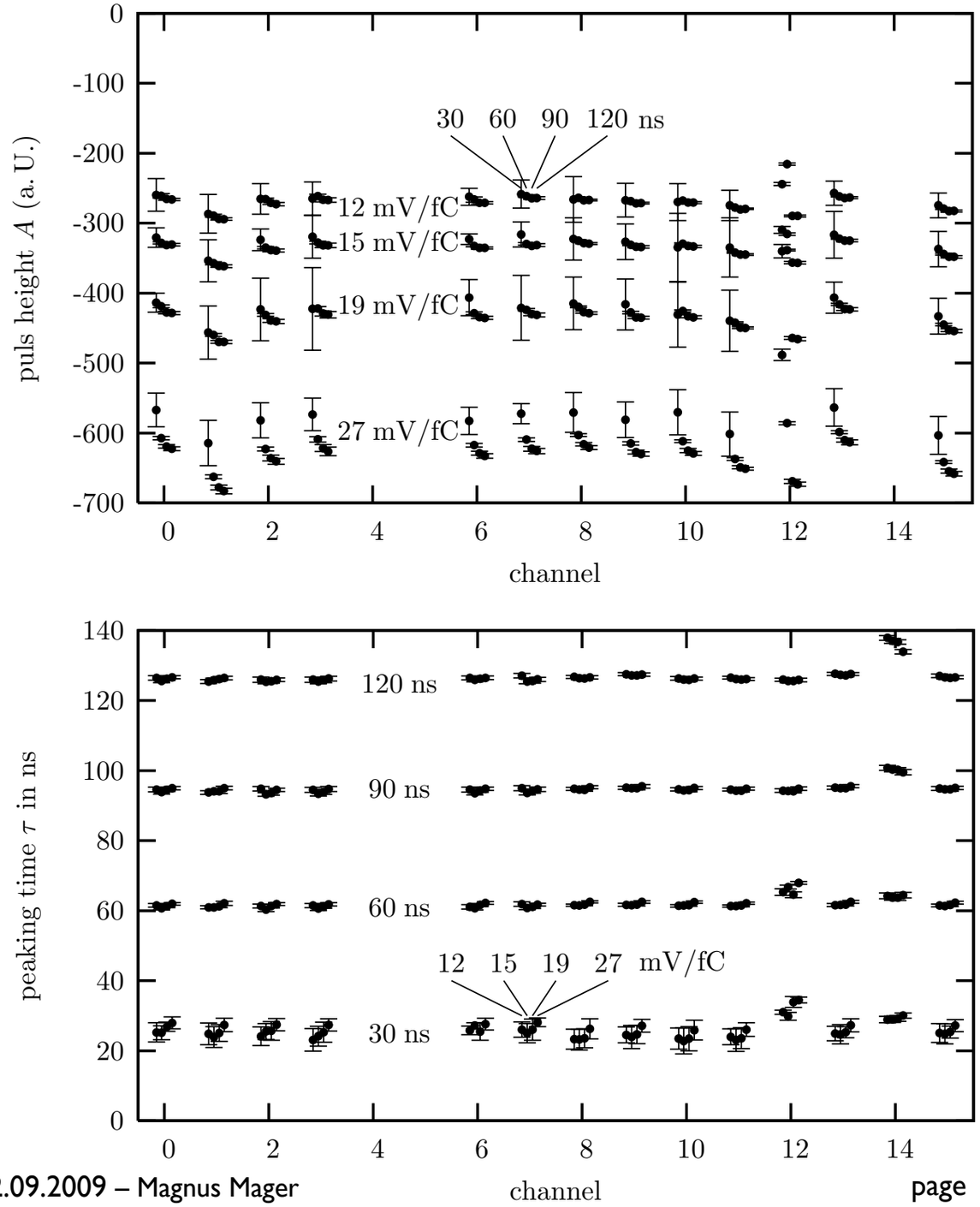
- Amplifier (PCA-16) – short summary
- ADC (2 channel prototype) – preliminary results (courtesy of Hugo França)
- S-ALTRO 16 channel demonstrator – design/planning

S-ALTRO design – current status

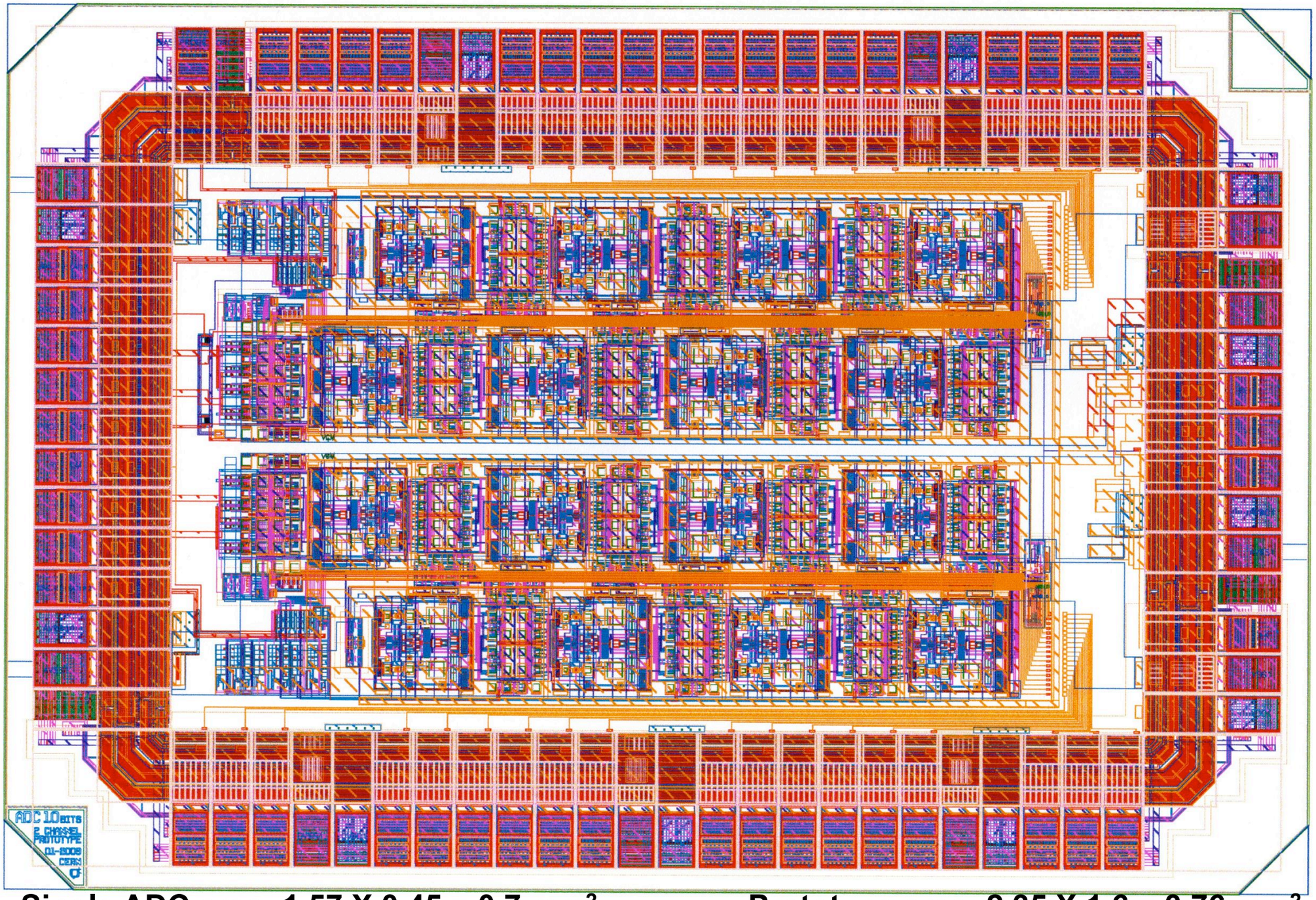


PCA-16

- CMOS 130 nm
- 0.2 mm^2/channel
- < 8 mW/channel
  - <1mW in standby
- works according specifications
- is already in use (e.g. at DESY)

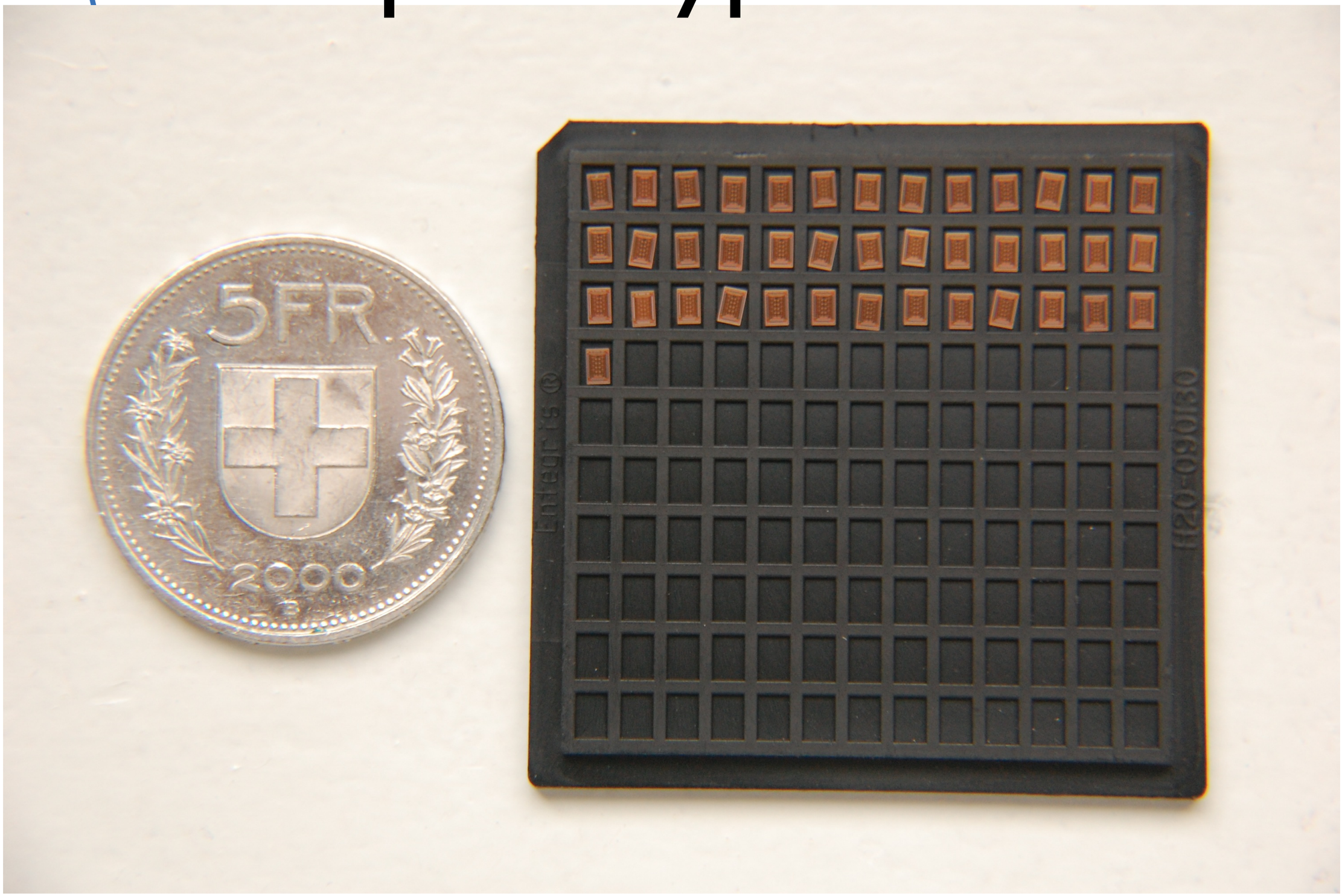


ADC prototype – design

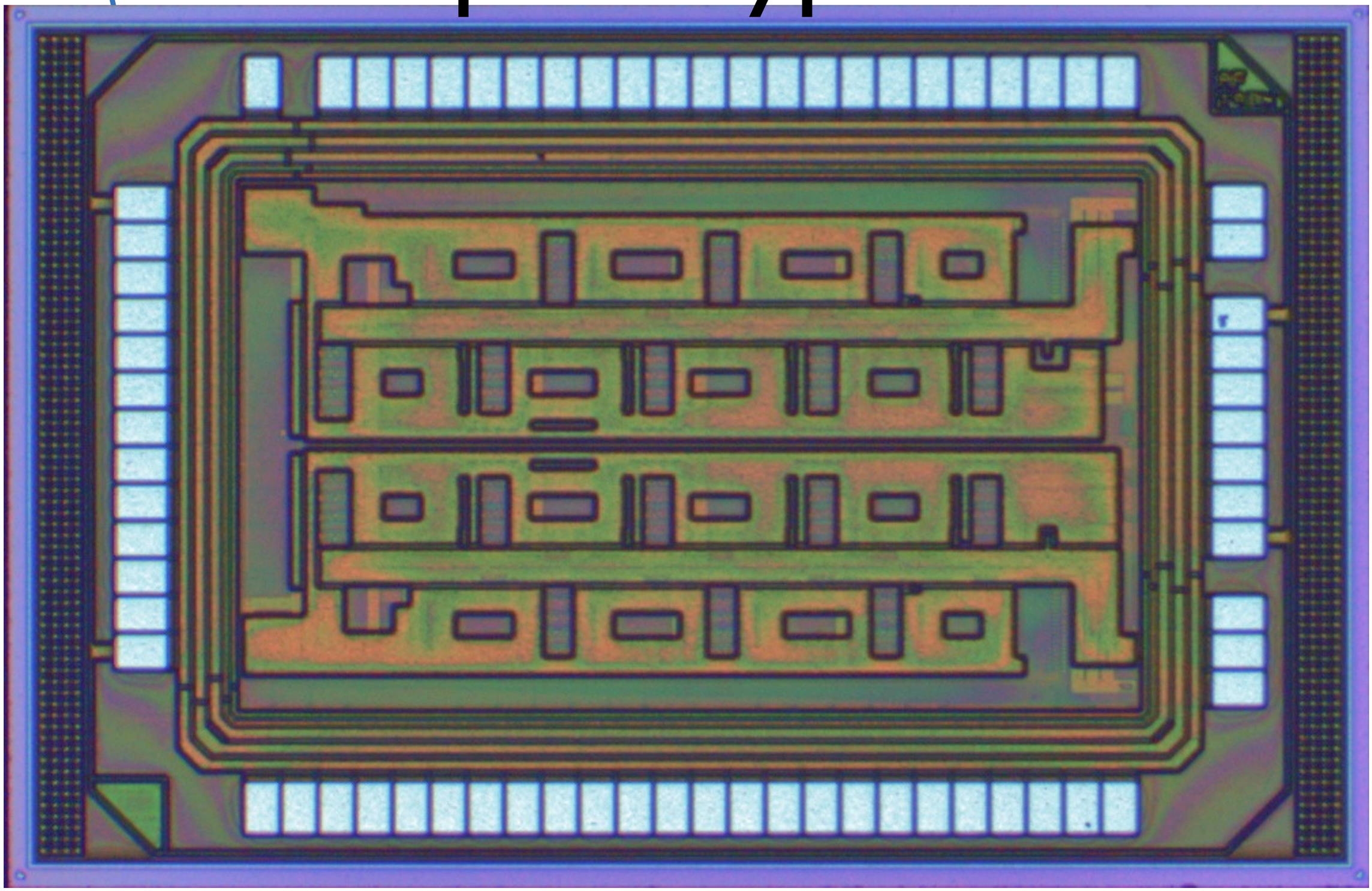


Single ADC area: 1.57 X 0.45 = 0.7 mm² **Prototype area: 2.35 X 1.6 = 3.76 mm²**

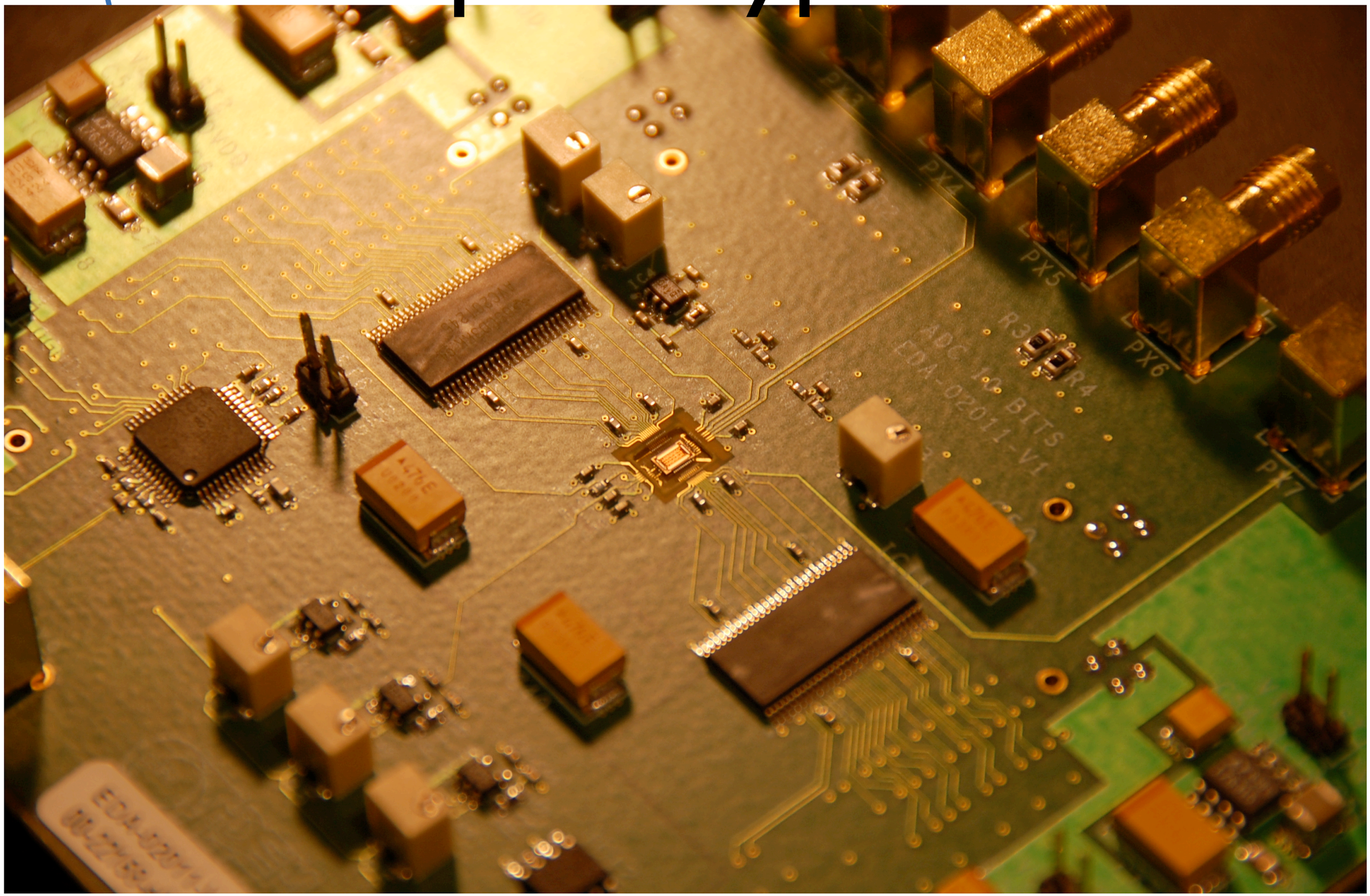
ADC prototype – arrival



ADC prototype – real

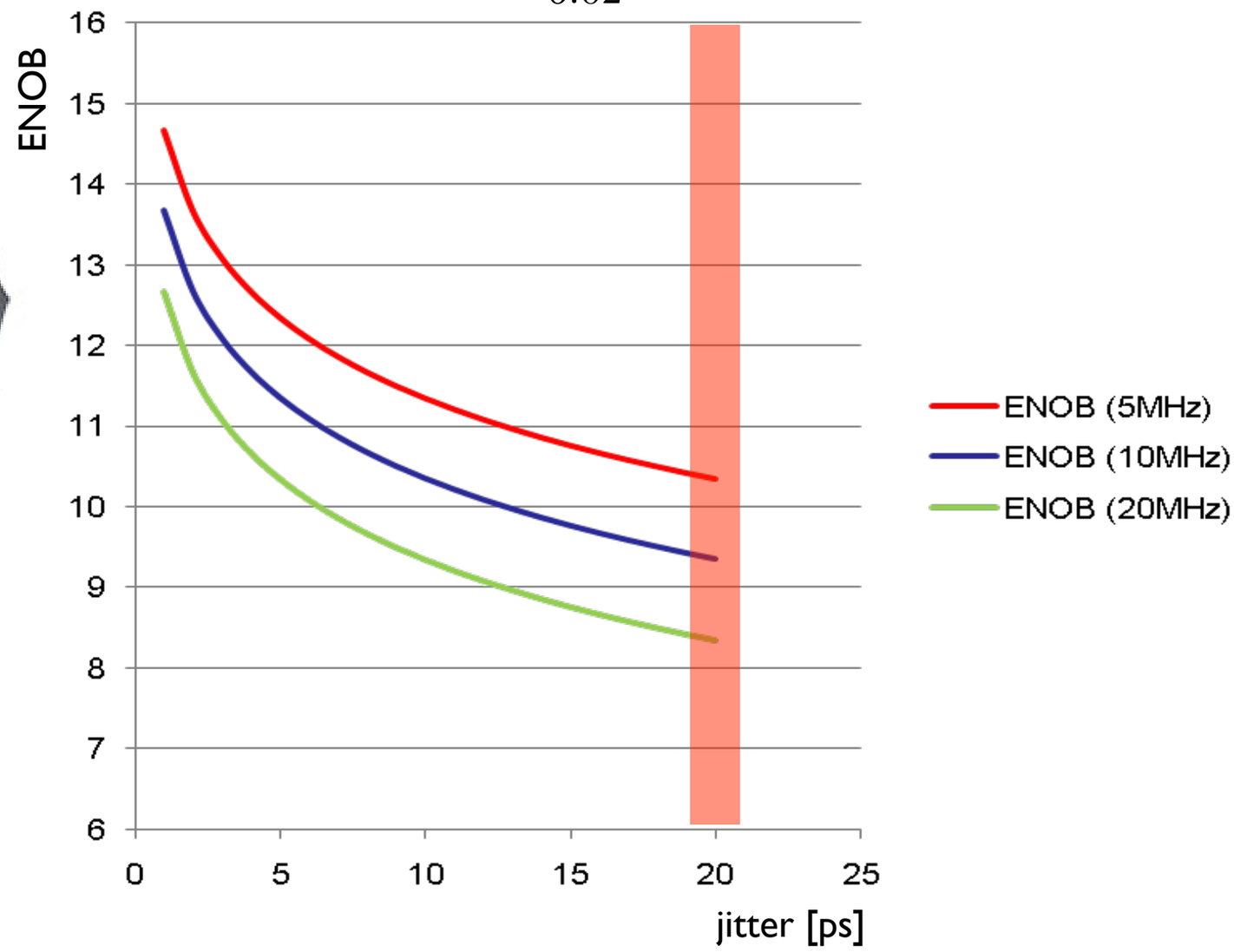


ADC prototype – test



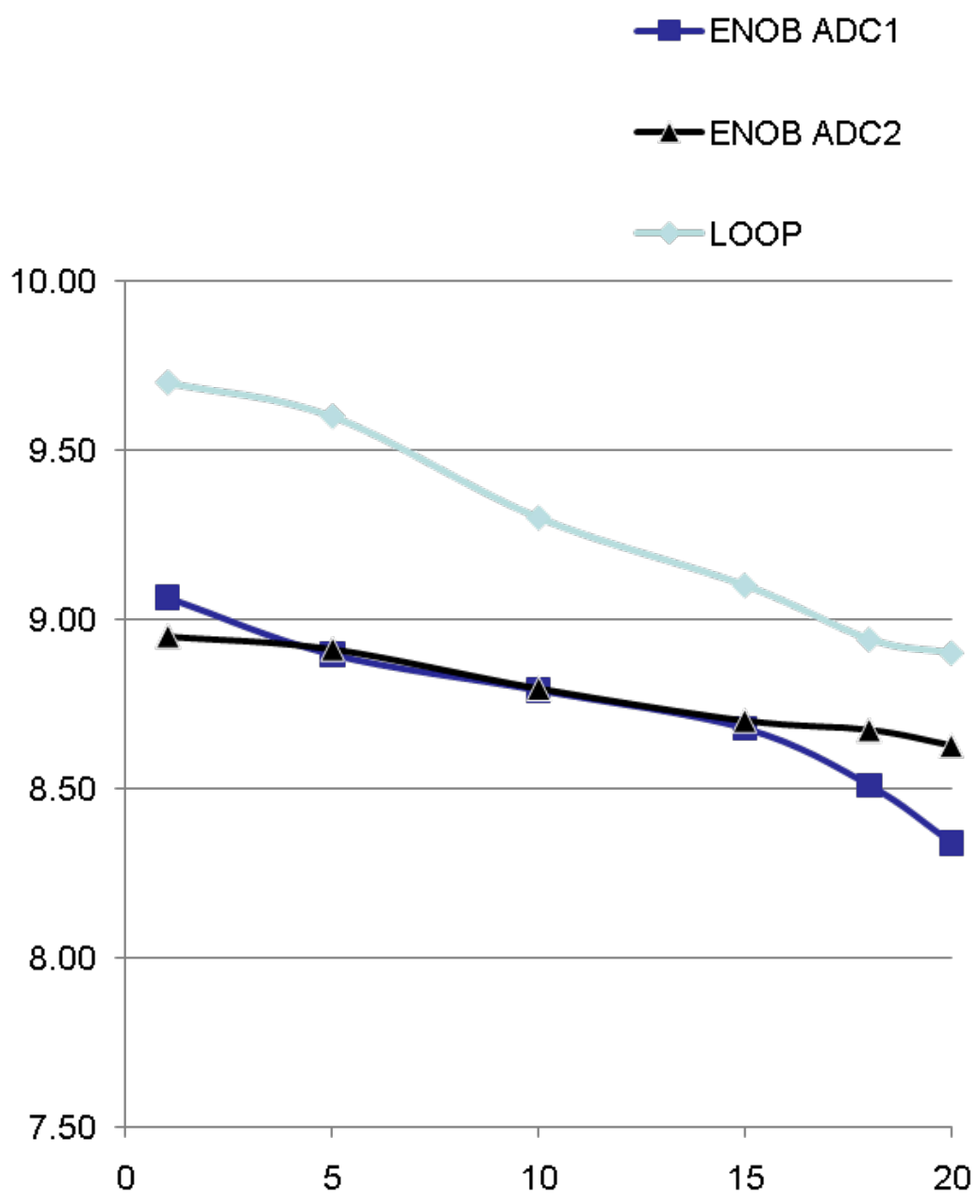
ADC prototype – test II

$$ENOB = \frac{10\log\frac{1}{2\pi f_{\text{in}}\sigma} - 1.76}{6.02}$$



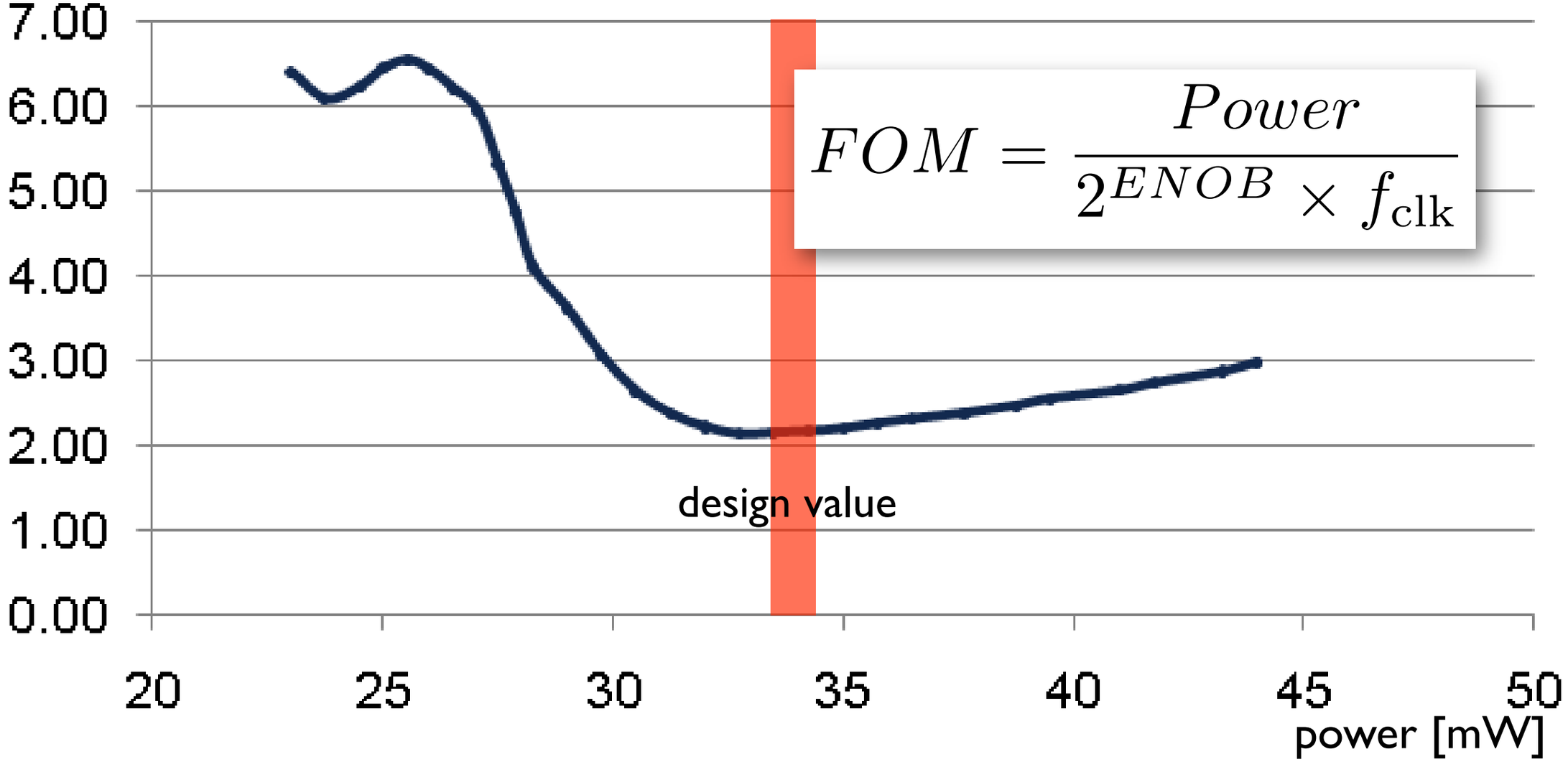
ADC prototype – summary

Dynamic Performance at 40MS/s					
PARAMETER	INPUT FREQUENCY	ADC1	ADC2	LOOP	UNIT
Effective Number of Bits (ENOB)	1.0071MHz	9.07	8.95	9.70	Bits
	4.9988MHz	8.90	8.91	9.60	
	9.9915MHz	8.79	8.80	9.30	
	14.9841MHz	8.68	8.70	9.10	
	17.9993MHz	8.51	8.67	8.94	
	19.9890MHz	8.34	8.63	8.90	
Signal to noise and distortion ratio (SINAD)	1.0071MHz	56.33	55.63		dB
	4.9988MHz	55.32	55.41		
	9.9915MHz	54.68	54.71		
	14.9841MHz	54.00	54.14		
	17.9993MHz	52.98	53.97		
	19.9890MHz	51.96	53.70		
Spurious free dynamic range (SFDR)	1.0071MHz	-75.03	-74.08		dB
	4.9988MHz	-71.12	-69.94		
	9.9915MHz	-64.78	-68.74		
	14.9841MHz	-61.13	-72.25		
	17.9993MHz	-58.89	-66.34		
	19.9890MHz	-56.89	-68.06		
Total Harmonic Distortion (THD)	1.0071MHz	-69.66	-70.73	-73.00	dB
	4.9988MHz	-63.12	-66.90	-71.00	
	9.9915MHz	-64.44	-65.65	-68.80	
	14.9841MHz	-67.57	-69.26	-66.50	
	17.9993MHz	-62.01	-64.66	-66.40	
	19.9890MHz	-60.87	-65.69	-70.00	



ADC prototype – summary II

FOM (pJ) @ 40 MS/s



Digital processor

- Using the ALTRO digital processor for demonstrator (migrated to 130 nm and slightly modified)
- Advantages are:
  - easy benchmarking using real FECs in real set-ups/experiments
  - focus on key-issue: integration of charge sensitive amplifier and ADC

Plans

- Submission of 16 channel prototype beginning of 2010
- Characterisation (including mounting onto FECs) in summer 2010
- Detailed review of critical parameters (sampling rate, shaping time, etc.)
- Design of the 64-channel chip as of fall 2010