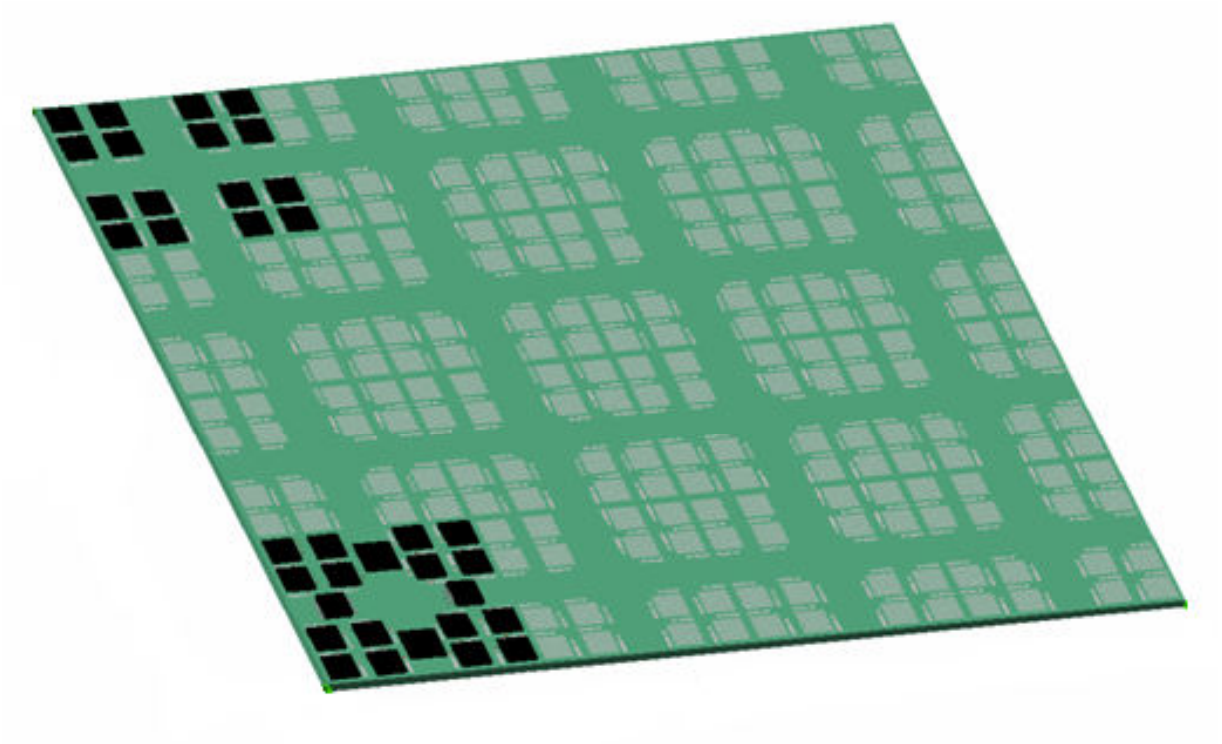
Tests of power delivery, power switching and cooling for S-ALTRO End-Plate

22/Sep/2009
LCTPC Collaboration Meeting
Takahiro Fusayasu
Nagasaki Institute of Applied Science

S-ALTRO mounted Advanced End-Plate



- S-ALTRO, under development, is designed so that it can be mounted on TPC end-plates. For high-density frontend electronics, we have various issues to be investigated.

What should be known

- How can we cool the end-plate equipped with S-ALTRO?
- Power pulsing cannot be avoided. What's the effect?
- What's the effect pf power pulsing under strong magnetic field?
- Assembly possibilities?

1. Cooling

Considerations on power dissipation

Power consumption

- amplifier 8 mW / channel
- ADC 12mW/channel (10MSPS), 34 mW / channel (40MSPS)
- Digital Proc 2 mW / channel
- data links 2 mW / channel
- power regulation efficiency: 75%
- Total power 32mW/channel (10MSPS), 60mW/channel (40MSPS)

Owing to the bunch-train time structure (beam duty cycle 0.5%), for the ILC and CLIC TPCs electronics a basic ingredient is power pulsing

In principle a factor ~70 (~1.5% electronics duty cycle) can be achieved

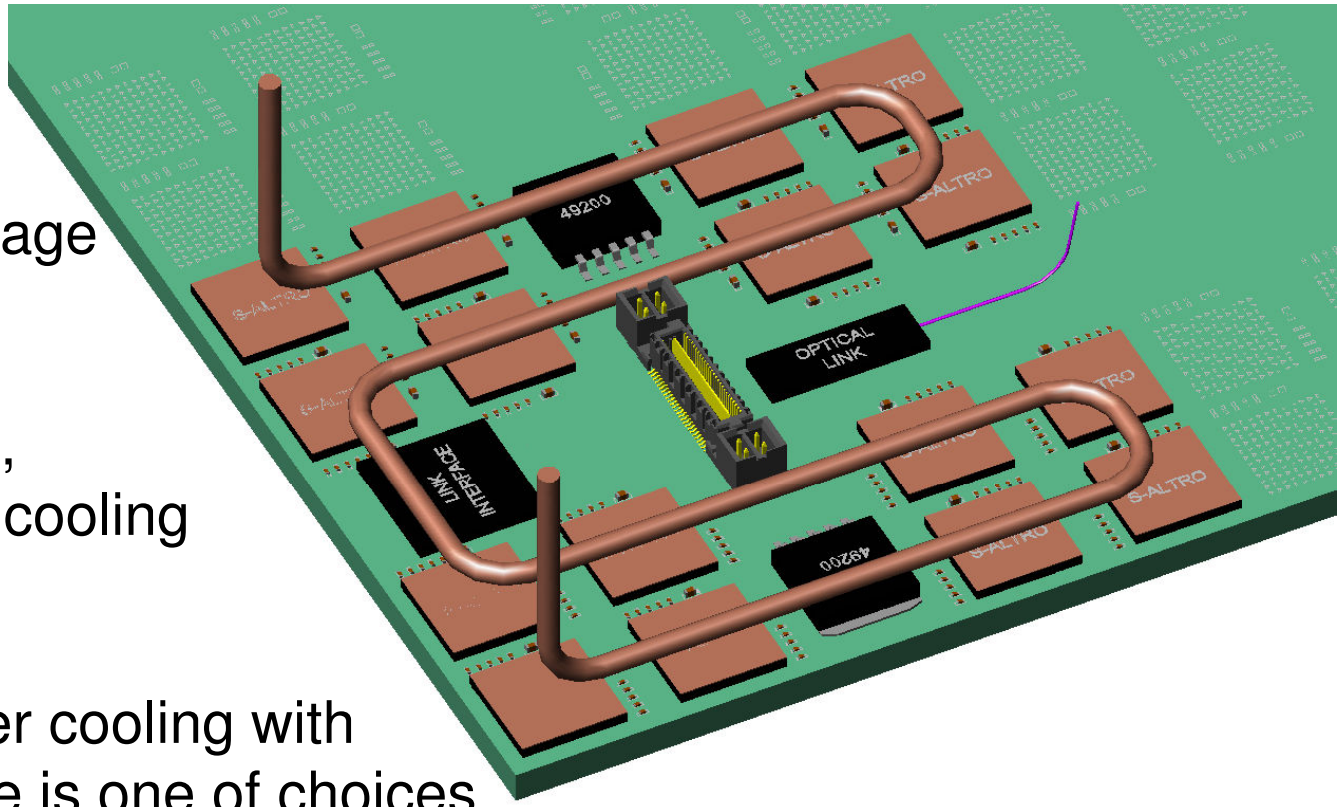
What can be achieved in practice is an important R&D issue

- duty cycle 1.5%
- average power / channel 0.5 mW / channel (at 10 MSPS)
- average power / m^2 100 W (at 10MSPS)

Power pulsing cannot be applied to PANDA

1. Cooling

Proper cooling is necessary to avoid not only thermal damage of chips themselves, but also temperature change of gas region, with small amount of cooling material.

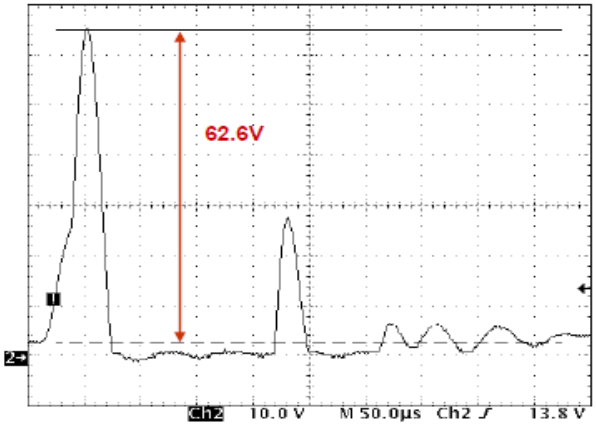


Although water cooling with aluminum pipe is one of choices, we should also carefully investigate possible other choices. After selecting one (or, two or three) of choices, we need to perform cooling test.

2. Power Pulsing

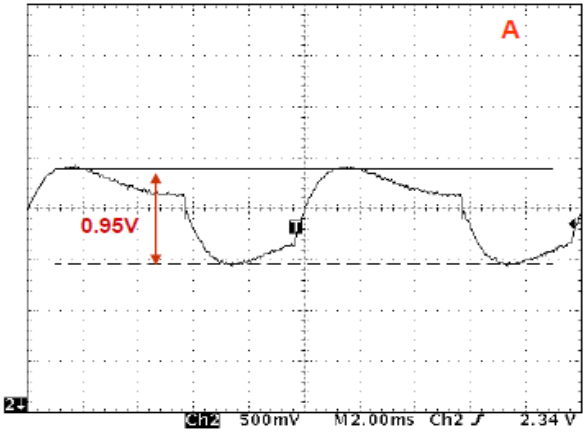
Configuration A
R = 0, C=0

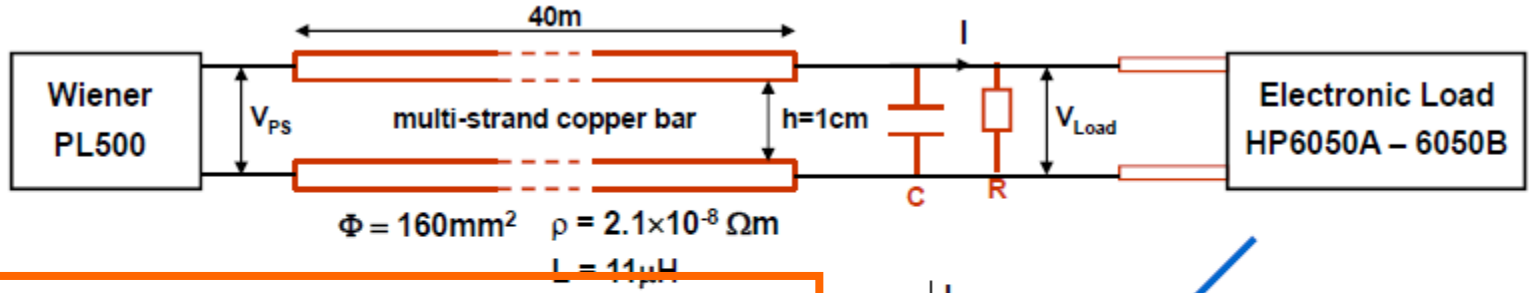
Sudden interruption of current can damage FEE

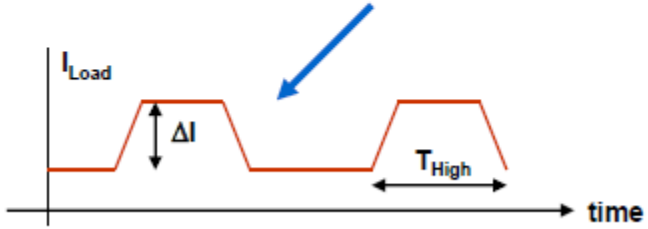


Configuration C
R = 25mΩ, C=70mF

70mF in parallel to load can absorb the large spikes







To be tested with a system very similar to the real (S-ALTRO based) end-plate.

3. Power Pulsing under Magnetic Field

- With power pulsing in strong magnetic field, unwanted mechanical oscillation may result because of Lorentz force.
  → It should be tested.

4. Possibility of Assembly

- Mounting many (16 x 16 FPGA) BGA parts on a board at the same time is possible, we think, but it should be confirmed by performing it actually.

We discussed….

- In order to discuss how to proceed with the advanced end-plate development, we met on 17/Sep/2009 at CERN.
- Members: Ron, Luciano, Antoine, Magnus, Takeshi, Akira and Takahiro.
- …followed by a small meeting on the next day.

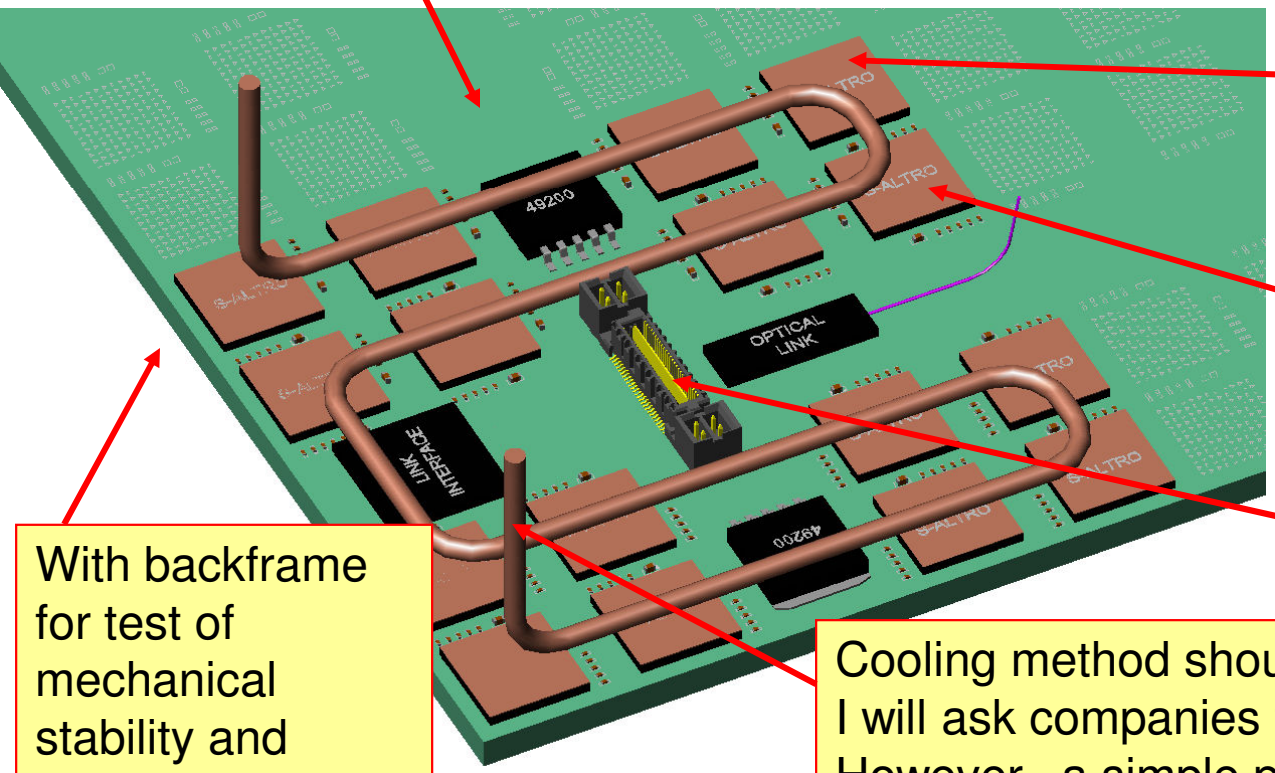
How we proceed….

- Luciano's team will concentrate on development of S-ALTRO, which includes design, verification, fabrication, characterization, etc.
- In the meantime, Japanese group, will contribute to tests of power delivery, power switching and cooling.

Test Plan

- FPGA and OPamp “dummy” are mounted instead of S-ALTRO

Layers, pads and routing of PCB similar to the final board design. Need to measure pad temperature.



Replaced by FPGA’s as current loads and thermal source

Some of them will be commercial OPamps or ADCs as “analog” current sources.

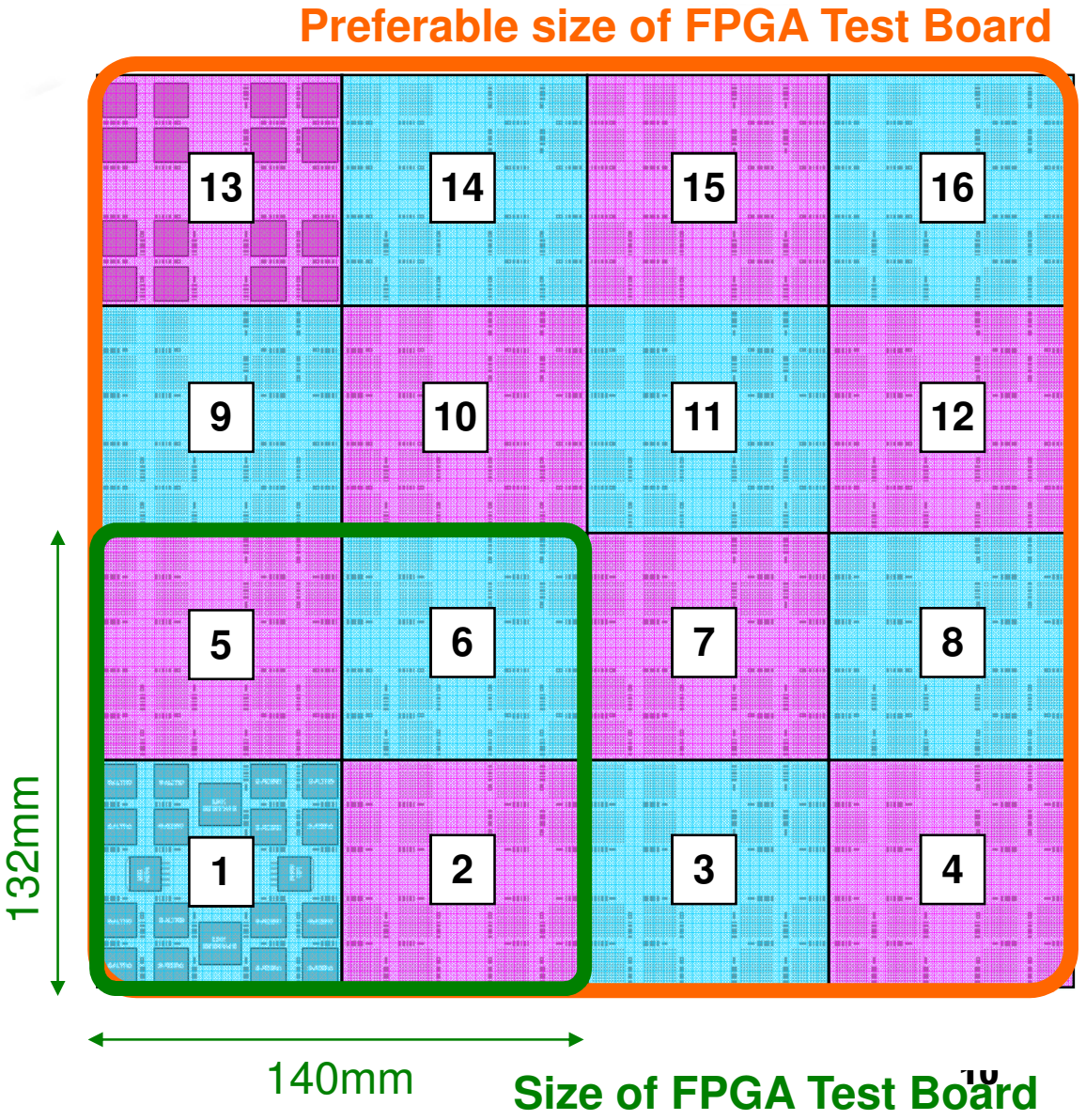
Power in (and control)

With backframe for test of mechanical stability and thermal conductance

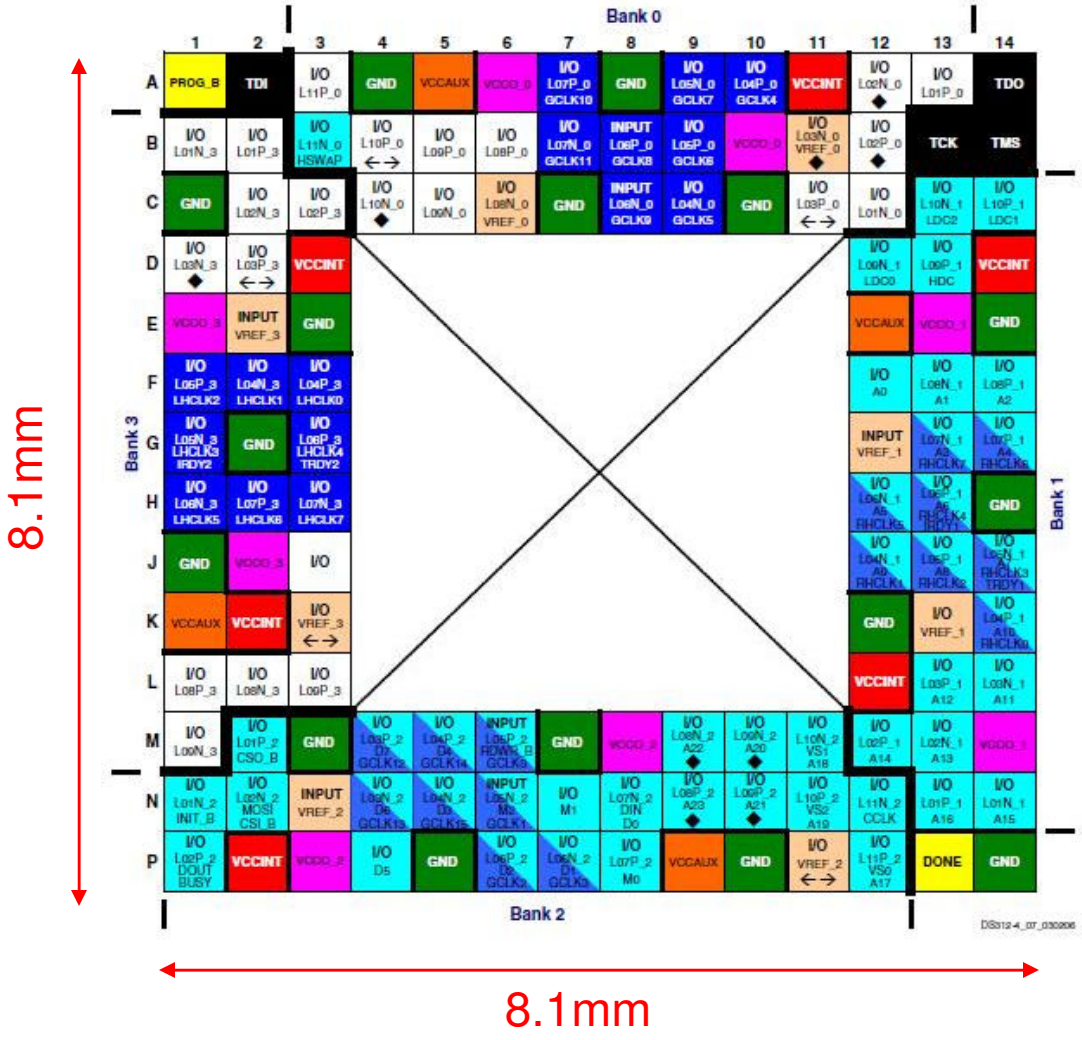
Cooling method should be carefully investigated. I will ask companies for existing technologies. However, a simple plane metal can be used as the first step.

Test Plan

- If budget is not enough, test with a quarter-size test board is one idea.
- However, full size is preferable because we need to verify the possibility of assembly of large number of BGA chips.
- Luciano kindly helps us for PCB layout and fabrication of cooling material.



FPGA – Spartan 3E XC3Sxxx (CP132)



92 I/O pins

*) Final S-ALTRO will have size of 10mm x 10mm and 64 channel pad input.

What to Test

- Thermal test with proper cooling (Cooling method is not determined yet now) → cooling method to be investigated.
- Power pulsing.
- Magnetic field effect.

What to Measure

- Temperature of each part with cooling.
- Voltage/Current transient of power line when power pulsing.
- Mechanical stability at high temperature.
- Mechanical stability in strong magnetic field.

Schedule

- Test with the FPGA board will be performed in ~1yr. (2009 – 2010).
- 16ch version of S-ALTRO will be obtained and characterized in 2010.
- After looking at results of S-ALTRO characterization and FPGA board test, we will discuss on the next step, i.e., how to proceed the final 64ch version of S-ALTRO and the end-plate for real S-ALTRO chips.