

# Status of the 10.000 channels Altro system

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10.000 channels = 78 front end cards

Naked boards produced: 100 boards

Mounted boards 20 MHz: prototype series 5 boards  
first delivery 20 boards  
second delivery 60 boards

Mounted boards 40 MHz 10 boards

⇒ In total 95 boards

These, however, include the 6 that are going to Japan

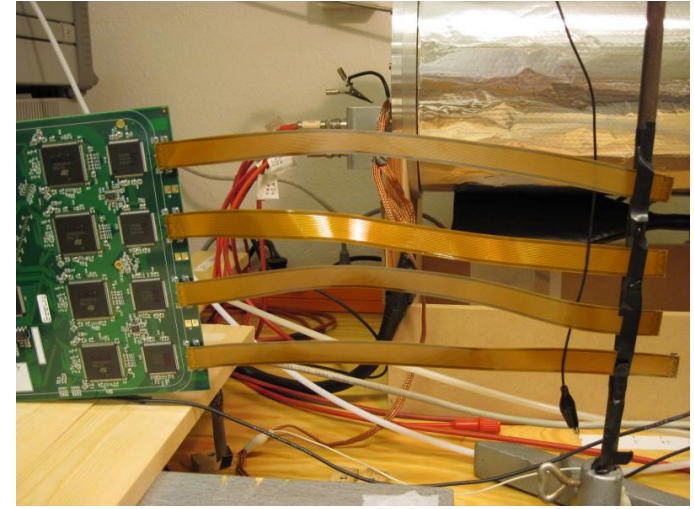
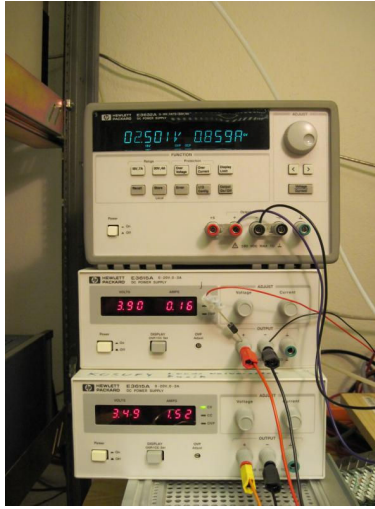
There is an interest from outside institutes to receive either FEC's or PCA16 chips.

# Tests of the FEC's

Every board is tested in the following way:

- Check that the currents are correct
- Perform a test of the registers in the Altro by feeding in different numbers and reading them back to check that they remain the same
- Perform pedestal runs for all parameter settings of the PCA16 and check that the pedestal and noise levels are within limits
- Inject charge by pulsing a wire which is applied across the signal cables (kapton cables)

# Some picture of the test set up



Power settings

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50

RCU0 RCU1 RCU2 RCU3

Load lookup tables at power on  Load lookup tables at Start DAQ

PCA settings

Polarity  Shutdown  Preamp enable  Gain  Shaper  Decay time

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[2009-05-28 16:54:11] SRV:*POW S0 0 RCU0 14000000 P0 14000000 S1 1 RCU1 3FE1FFE P1 0 S2 1 RCU2 7165 L
[2009-05-28 16:54:11] Retrieving PCA settings...
[2009-05-28 16:54:11] SRV:*PCA SR 128 DAC 1000 ERR 0
[2009-05-28 16:54:13] Stopping DAQ.
[2009-05-28 16:54:13] SRV:*STATUS DAQ_0 RUN 0 LOG 1 MON 1 EVT 515 TYPE 3 MODE 1 RUNNB 7165 L
[2009-05-28 16:54:15] Powering off...
[2009-05-28 16:54:20] SRV:*POW S0 1 RCU0 14000000 P0 0 S1 1 RCU1 3FE1FFE P1 0 S2 1 RCU2 FFFF1D
[2009-05-28 16:54:22] Powering on and loading lookup table...
[2009-05-28 16:54:23] SRV:*POW S0 0 RCU0 14000000 P0 14000000 S1 1 RCU1 3FE1FFE P1 0 S2 1 RCU2
[2009-05-28 16:54:54] Starting DAQ.
[2009-05-28 16:54:54] *START CONTROL 1 MODE 1 TYPE 3 LOAD 2
[2009-05-28 16:54:55] SRV:*STATUS DAQ_1 RUN 0 LOG 1 MON 1 EVT 515 TYPE 3 MODE 1 RUNNB 7165 L
[2009-05-28 16:54:55] Retrieving power status...
[2009-05-28 16:54:55] SRV:*POW S0 0 RCU0 14000000 P0 14000000 S1 1 RCU1 3FE1FFE P1 0 S2 1 RCU2
[2009-05-28 16:54:55] Retrieving PCA settings...
[2009-05-28 16:54:55] SRV:*PCA SR 128 DAC 1000 ERR 0
```

Run comment (max 240 characters):

Events: 515

Run:7165  
[2009-05-28 15:18:27]

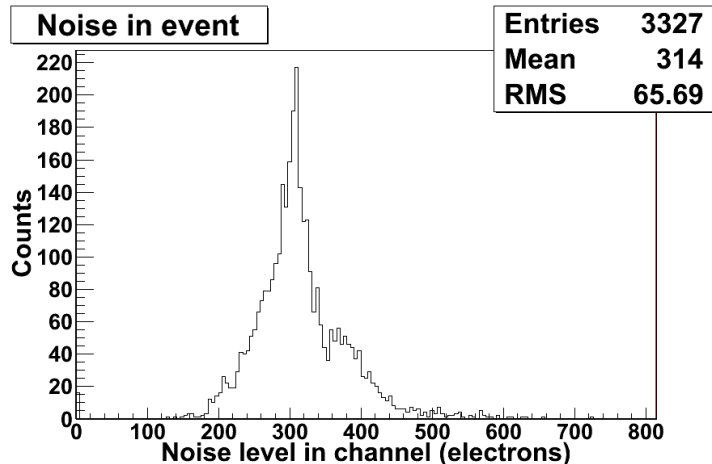
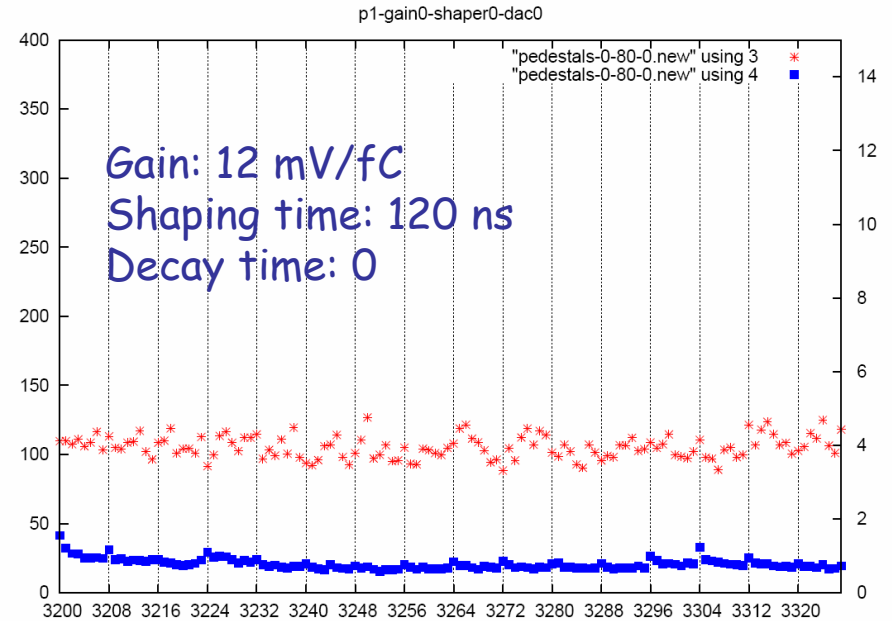
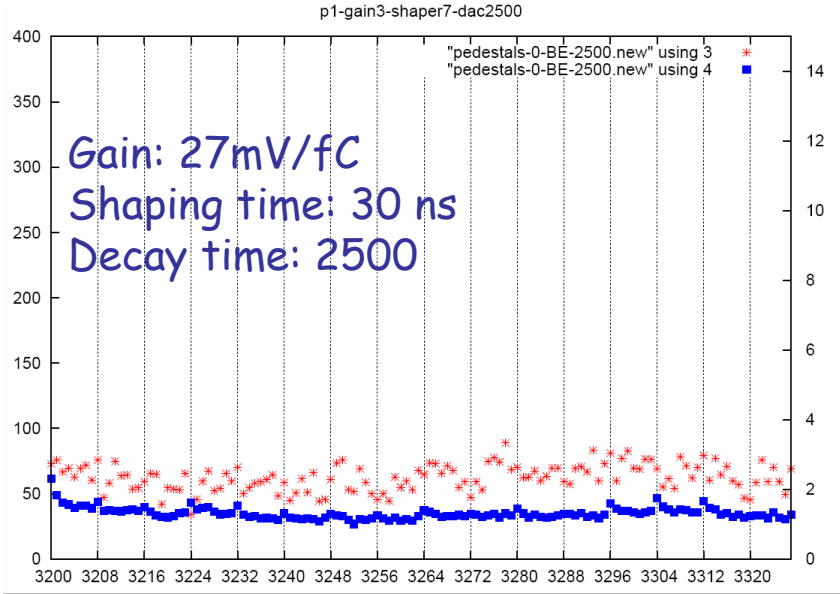
--- Write run comment ---

Run type:  Physics  Pedestals  Test

Run mode:  Pedestal subtraction  Zero suppression  Logging

Monitor

# Typical pedestal runs (FEC 26)



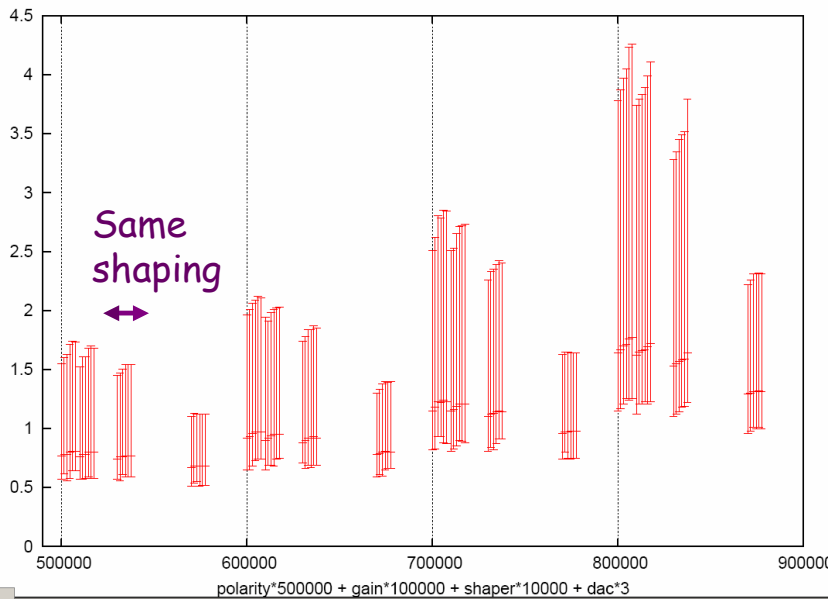
Noise distribution of 3000 channels in the 3 module set-up with gain 12 mV/fC and shaping time 120 ns

Note: the average noise is 314 electrons

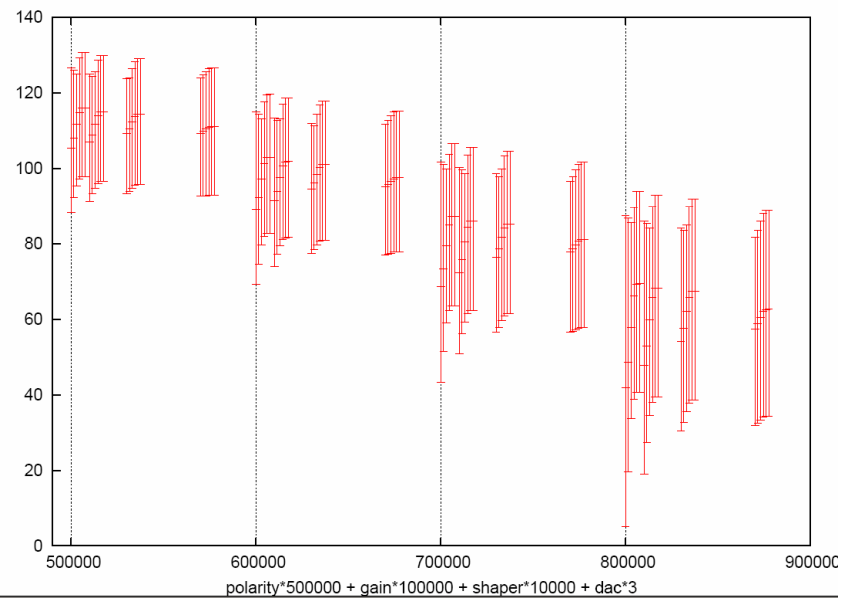
# Summary of pedestal and noise (FEC 26)

$$\text{polarity} \cdot 50000 + \text{gain} \cdot 10000 + \text{shaper} \cdot 1000 + \text{dac} \cdot 3$$

noise



pedestals



Same gain

Same polarity

## Status of FEC tests

Tested so far:                    5 from the prototype series  
   20 from the first delivery  
   29 from the second delivery

⇒ In total:                        54 FEC's

Remain to be tested:            31 from the second delivery  
   10 with 40 MHz Altro

The tests of the FEC's with 40 MHz Altro's will be done at 20 MHz to start with  
For tests at 40 MHz a 40 MHz sampling clock is needed in the RCU (firmware)

# Future plans

- Perform tests with 10.000 channels  
⇒ bring the FEC crate + FEC's + RCU + computers to Lund
- Every RCU can take 32 FEC's  
⇒ 3-4 RCU's are needed depending on how the FEC's are distributed
- The DAQ system is prepared to run with 10.000 channels but has to be tested
- Temperatur sensors for the FEC's have to be developed
- A new cooling system has to be designed
- In addition to the tests described above, also Altro memory tests will be performed
- Get the distribution box running (Brussels), since this is needed to in order to operate the TPC together with the pixel detector