TLU Developments

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Outline

- Test-beam experience of TLU v0.2
- Hardware enhancements
- Hardware enhancements
- Plans.
- Conclusions.

Test-beam Experience

- TLU used at JRA1 beam-test at CERN
- Many new firmware features introduced to support (s)LHC users
  - Lead to number of significant "regressions" in firmware.
- Bug fixing underway.
  - Following a period of non-LC activities.

Hardware Enhancements

- Clock board produced using TI cdce949.
  - Produces two TTL and two LVDS clock outputs.
  - Frequency controllable by I2C.
  - Clock either produced from crystal or input from front-panel.
  - Can be retrofitted to existing TLUs (but needs new front panel)
  - New front panel also has mounting for LVTTL general purpose I/O connector.
  - https://svn.phy.bris.ac.uk/svn/uob-hep-pc017a/trunk/www/Schematics/pc017c_clock_board.pdf

Hardware Enhancements

- 15V supply for photo-multiplers upgraded:
  - Includes adjustable 0-1V control voltage (I2C interface).
  - Can be retrofitted to existing TLU v0.2 (no new front panel required)
  - Uses 4-pole Lemo wired to “DESY standard”.

Firmware Enhancements

- Can generate “synchronization pulse”
  - LVTTL on front panel Lemo
  - Pulse width and repetition frequency set terms of clock cycles.
  - Implemented for Timepix.
  - Armed by writing to width/frequency registers. Starts running when timestamp reset.
- Resetting time-stamp results in pulse on reset line of active DUTs.

Firmware Enhancements

- Block transfer doesn't time-out

  Also requires changes to TLUProducer.exe

  (no longer try to start/stop transfer, but continuous transfer)

- Trigger-only handshake-mode

  Issues fixed length trigger pulse to DUT (ignores BUSY line).

  Mode selectable on DUT-by-DUT basis (can be mixed with TRIGGER/BUSY handshake)

- More information about FSM status available.

Firmware Updates

- Option for DUT to initiate “busy” by raising DUT_CLK line (outside a trigger/ busy handshake sequence).
  - Can be selected on a DUT-by-DUT basis
  - Removes race condition where DUT raising BUSY and then thinks it has suspended triggers and *simultaneously* TLU sends trigger and thinks that BUSY is raised in response.

Firmware Updates

- Time-stamp precision has been increased from a single clock cycle (20.8ns by default) to 1/8 clock cycle (2.6ns)

Accuracy isn't as good as this - bins not equal size due to timing skew between different derived clocks.

- Trigger masks improved..

Existing AND-Mask and Or-Mask work as before.

Can write a 16-bit number that defined what combination of inputs will result in trigger.

Second, independent, trigger connected to scaler. Use for e.g.

Future Firmware Updates

- Code needs a substantial tidy up
  - Code for interface hardware (EZ-USB chip) completely mixed with TLU specific code.
  - Factorize to make it easier to add new modules.
  - Make it easier to run simulations - hence fewer bugs in released code (hopefully!)
  - Regressions, and existing bugs need to be removed.

Firmware Proposal

- An idea arising from a discussion with Diamond Detector physicist.
  - Have a “readout with scope mode”
  - Supply a trigger (no handshake)
  - Clock out trigger number using internal TLU clock (also provide a clock from TLU)
  - Read out detector with a ‘scope (perhaps MSO)
  - Allows charge collection efficiency to be mapped.

Plans

- Priority:

  1) Fix existing bugs.

  2) Finish work to make block transfer reliable.

  3) Debug new features.

- Possible:

1) Work towards tagging mode. Probably involves taking time-stamp of every incoming trigger.

2) Investigate possible hardware enhancements (would require moving to a different hadware platform.)

* More trigger inputs

* Faster FPGA (higher accuracy time-stamp , lower latency, smaller dead-time).

Plans

- Potential Hardware:

1) Commercial hardware (e.g. NI FlexRio , CAEN V1495, Wiener NEMBox)

* Advantage - only need to make custom daughterboards.

* Disadvantage - firmware almost as much effort as custom approach. Requires every site to buy either VME crate or NI crate. With NI board - Dangers of “Microsoftization” of HEP with Labview - short term gain, long term pain.

* (Wiener NEMBox doesn’t seem to have very good block transfer - any body with experience?)

Plans

- Potential Hardware:

2) Use a more powerful FPGA prototyping board.

* Advantages - could make compatible with existing TLU daughterboards. Could use Ethernet and produce a network-attached “TLUProduducer.exe in a Box”. Lower (hardware) cost.

* Disadvantage - need to produce more custom hardware.

Conclusion

- Significant number of new features were introduced for the 2009 beam-test season.
  - This took effort away from debugging existing code.
  - Lead to a number of serious regressions.
- Available effort now concentrated on bug-fixing.
- Once TLU firmware/software is stable again, will move towards prototyping “tagging mode” with existing hardware.