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#### OUTLINE

- Zero Suppressed Digital Chip (MIMOSA26) description
- MIMOSA26 characterization in-lab : summary
- > MIMOSA26 characterization in beam (preliminary)
- Summary



### MIMOSA 26 : description

Main parameters & Functionalities :

- AMS-OPTO 0.35μm
- Pixel Size : 18.4 x 18.4 μm<sup>2</sup>
- Active Area : 1152 x 576 pixels (21.2 x 10.6 mm<sup>2</sup>)
- 8 Analog test Outputs
- 1152 end-column discriminators (663552 pixels)
- Slow Control Interface : JTAG
- Internal Bias (DACs)
- Zero suppression mode (SUZE-01)





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#### Goals of the laboratory tests (done on IPHC test bench)



#### Analog test outputs :

- Temporal Noise (TN)
- Fixed Pattern Noise (FPN)
- Charge to Voltage Conversion Factor (CVF)
- Charge Collection Efficiency (CCE) for 3x3 and 5x5 Clusters

Digital test outputs :

- Characterization of internal DACs
- TN and FPN for discriminators only
- TN and FPN for discriminators + pixels



Working conditions :  $F_{CLK-(chip)}=80MHz (\rightarrow 20 \text{ MHz}) \Rightarrow T_{integ}=112.5 \ \mu s \ ; I_{pix_sf} = 50\mu A \ ; T_{chip}\approx 20 \ ^{\circ}C$ 

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#### **Results on analog test outputs**





고 구	Cluster size	Seed (1x1)	2x2	3x3	5x5
@ 20MF	MIMOSA 26	22 %	55 %	73 %	83 %
	MIMOSA 22	22 %	58 %	75 %	86 %

TN ≤14 e<sup>-</sup> @80MHz, it decreases to≤12e<sup>-</sup>@ 20MHz

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#### **Results on digital test outputs**



#### Zero suppression logic test







Zero suppression is based on row by row sparse data scan readout Zero suppression logic has been extensively investigated

(disconnected from the rest of the chip)



Various patterns were emulated with a pattern generator,

running through the logic millions of time without any errors up to 115 MHz

(1.44 times nominal frequency)

# **Summary of lab-characterized Chips**

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Characterization of 2 different types of sensors :

- 1 wafer of « standard » sensors (23 characterized)  $\rightarrow$  7 for Ingrid + 1 for Angelo
- 1 wafer of 120µm thinned sensors (6 characterized)

34 chips tested



1 chip from each wafer doesn't work (2chips)  $\rightarrow$  32 chips working

#### 29 chips completely characterized



- 1 chip with 1 dead row and 1 dead column
- 4 chips with 1 row or 1 column dead
  - $\rightarrow$  24 chips fully working (77%) / 28 chips working correctly (>90%)

### Setup for the beam tests



#### A lot of measurements:

- 8 chips used : 2 standard, 6 120µm thinned
- 4 studied as DUT : 2 standard, 2 120µm thinned
- 54 runs taken, 25.10<sup>6</sup> events, 0.5To data













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### The different measurements

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The different validation steps of the test beam:

#### 1. validation of our setup

- $\rightarrow$  4 Runs with threshold from 14N to 6N
- 2. characterization of a 120µm thinned chip (chip24)
  - $\rightarrow$  7 Runs with threshold from 12N to 4N

#### 3. characterization of a unthinned chip (chip1)

- $\rightarrow$  9 Runs with 10N to 4.5N thresholds, 2 Vref2
- 4. DUT rotation
  - → 8 Runs at 0°, 45°, 58° (5N-8N threshold)
- 5. Homogeneity of all the arrray check
  - $\rightarrow$  7 Runs by moving the beam or connected only 128 discri.

#### 6. Characterization of 2 other chips as DUT

One 120 $\mu$ m thinned chip (13) and one unthinned chip (4)

- $\rightarrow$  4 Runs (3N-10N threshold)
- 7. Telescope check with different beam intensity
  - $\rightarrow$  3 Runs (5,5k $\rightarrow$ 1.3k)
- 8. Characterisation of chip1 & chip24 @ 20MHz
  - $\rightarrow$  3 Runs (5N $\rightarrow$ 8N)

# **Noise Study**

Temporal noise

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Donahold distribution Indd

16531

Temporal noise

Fixed pattern noise

Threahold distribution in M

165312

Noise distribution ImVI

Noise:

scan of discriminator thresholds performed

Fixed pattern noise

Noise distribution [mV

185

 $\rightarrow$  Same results as in lab

# Fake hit rate study



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# $\varnothing$ output performances with MIPs



- det. eff. ~ 99.5 +/-0.1 % for a fake hit rate ~1.10<sup>-4</sup>
- satisfactory performances for Mi26

(even if they are a little bit bellow one observed for Mi22/Mi22bis)

• resolution ~4.5µm (Mi22 ~4µm)  $\rightarrow$  still in progress to be understood

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### **Cluster characteristics**





- similar tendency between the different MIMOSA22/22bis and MIMOSA26 chips
- for 6N cut -> 3.5 pixels hit in average, for 10% of the events just one pixel touched

# Summary

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# MIMOSA26 is working properly compared to what is expected with MIMOSA22

• TN ~ 0.6-0.7 mV – FPN ~ 0.2-0.3 mV

#### Beam tests :

Lab tests :



- analysis still in progress:
  - $_{\odot}$  improve the cluster position reconstruction
  - $\circ$  Study efficiency per sub-array
  - o study "angle" run
- det. eff. ~ 99.5 +/-0.1 % for a fake hit rate ~1.10<sup>-4</sup>
- resolution ~4.5μm (Mi22 ~4μm)



#### $\Rightarrow$ Mi26 performances are efficient for EuDet telescope

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DUC

# Thank you for your attention



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### MAPS (Monolithic Active Pixel Sensor) Principle

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- sensing elements and processing electronics on the same substrate using a standard CMOS process
- Ionizing particles create e-h pairs in the lowly doped epi-layer
- electrons diffuse thermally to the N-well/P-Epi diode





21.5 mm

#### EUDET Testbeam Infrastructure (JRA1) (Detector R&D toward International Linear Collider)

Provide a large high field magnet lrfu Provide beam telescope with 6 layers of MAPS with : • Very high precision (  $< 3\mu m$  precision even at lower energies) High readout speed (frame rate > 1 kHz), T<sub>integ time</sub> ~100µs/frame • Binary readout saclay • Easy to use (well defined/described interfaces) • Wide range of conditions for devices under test (cooling, positioning, magnetic field) > Major users : Pixels, CCD and DEPFET detectors, TPC. ... Initial setup @ DESY < 6 GeV/c electrons > Transportable : Hadron beams at FNAL, SLAC or CERN PCMAG @ DESY **PCMAG** available 2009 2008 Demonstrator Final Telescope **Integration Starts Available** M22(IDC) M26 submission **Available** 

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