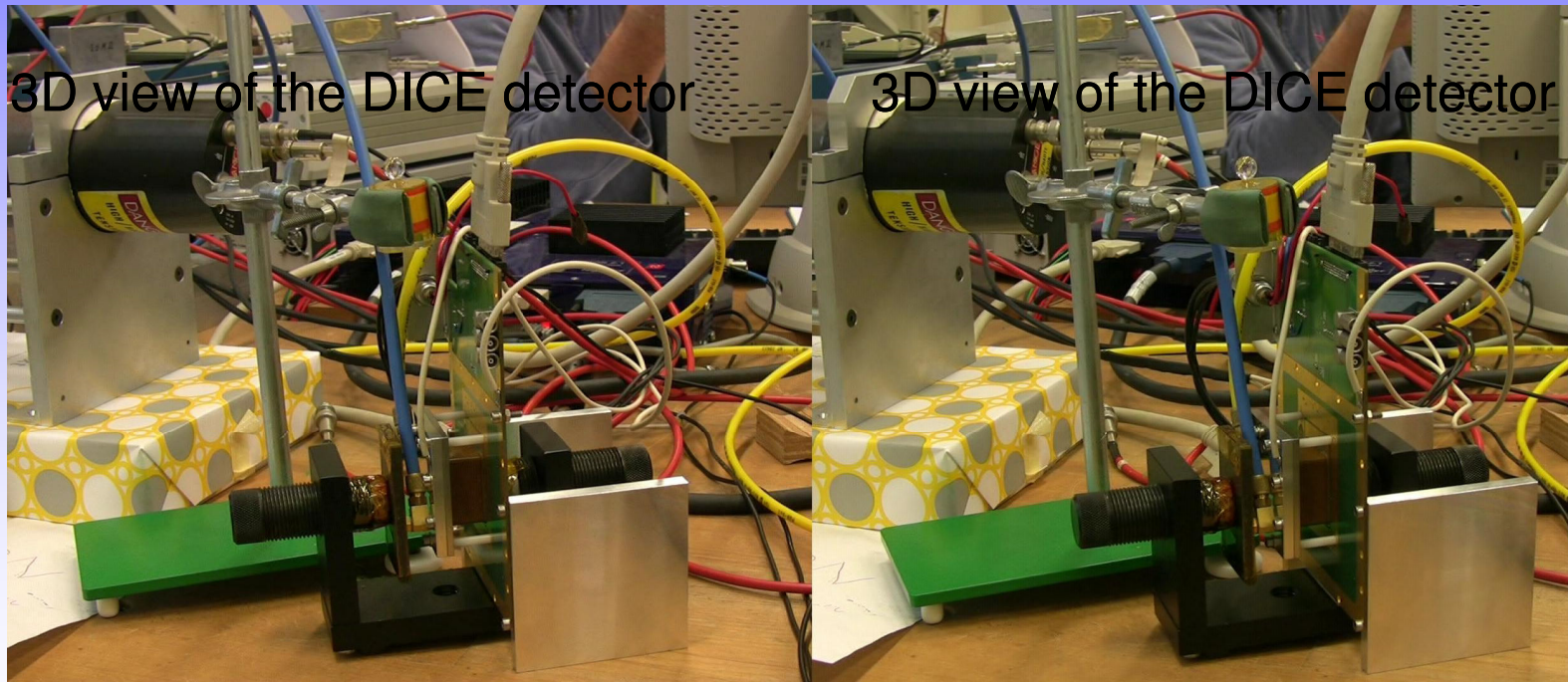


Gridpix; post processing and test results

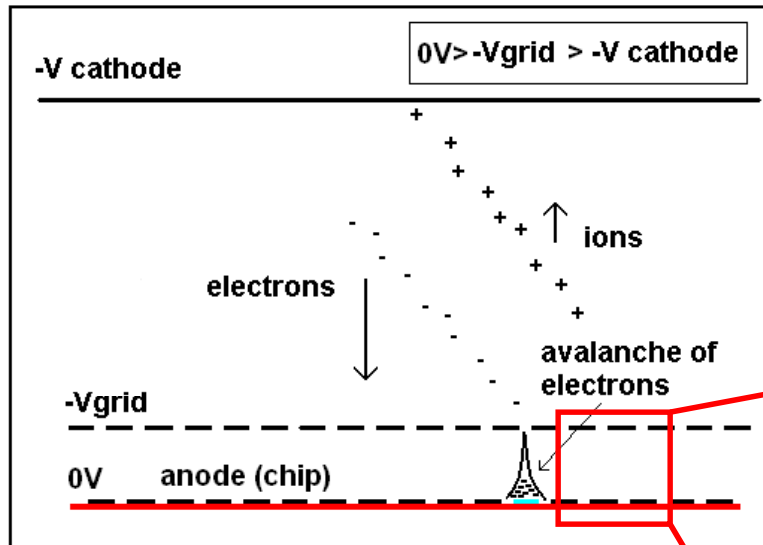
Martin Fransen, Nikhef



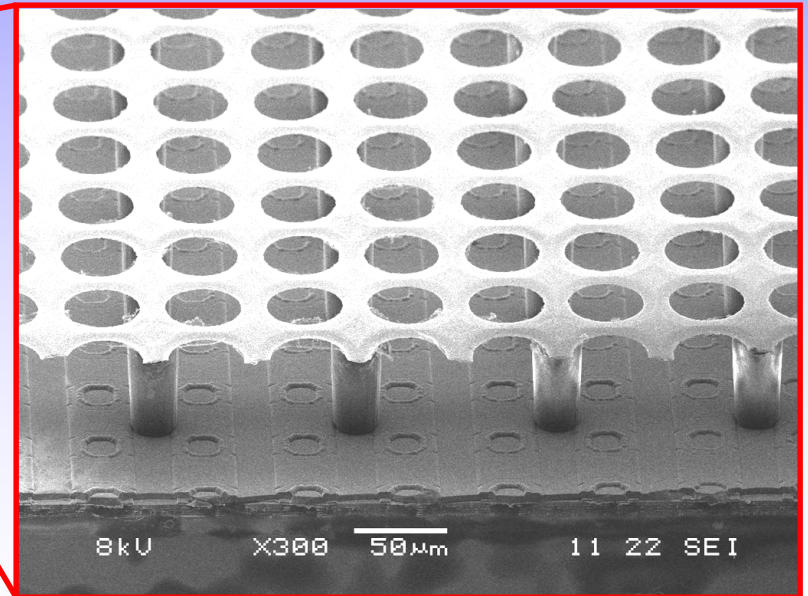
Outline

- Chip post processing
- Testing GridPix at DESY
- Testing Gossip at CERN
- Iflink and optical powering

Gridpix detectors

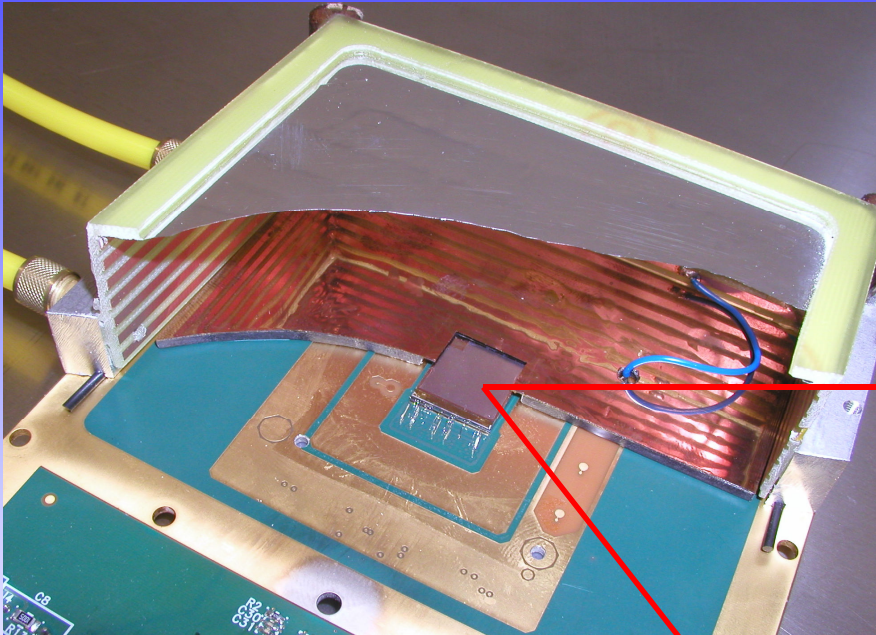


- Drift time gives z coordinate.



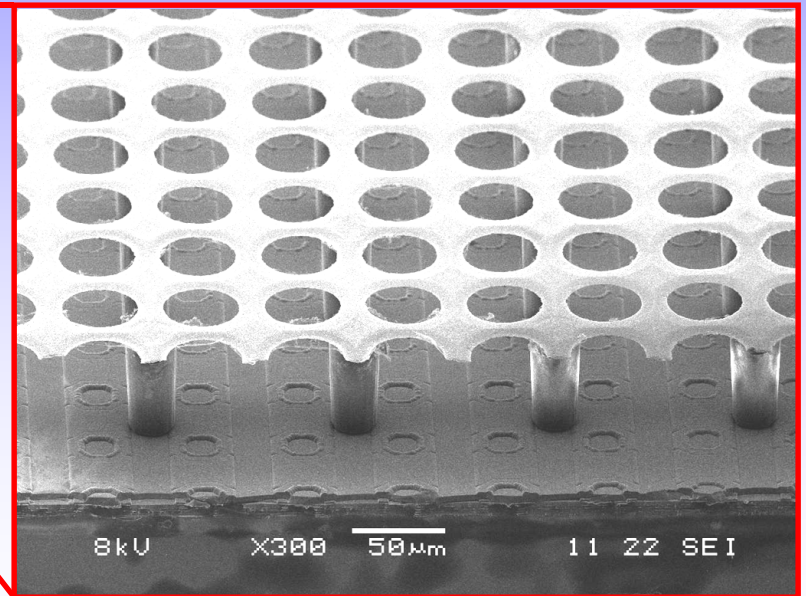
- Cathode
 - Drift volume ($\sim\text{mm}$ to $\sim\text{m}$)
- Grid
 - Gain region ($\sim 50\text{ }\mu\text{m}$)
- Pixel readout chip

Gridpix detectors



- Drift time gives z coordinate.

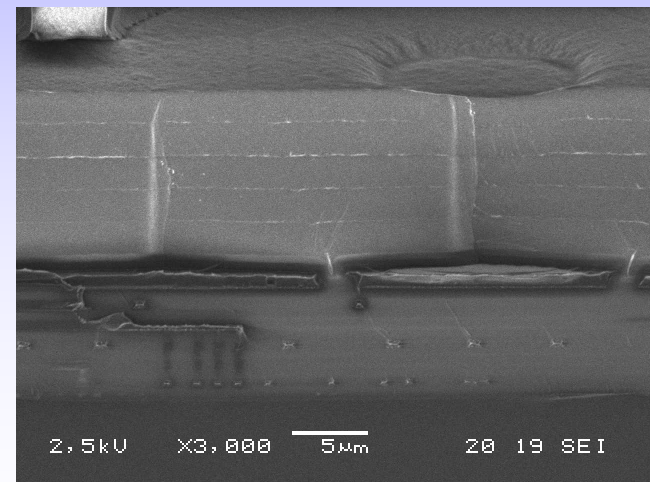
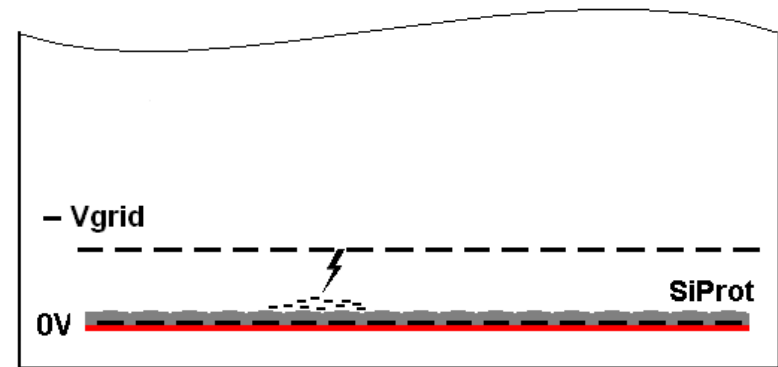
- Cathode
 - Drift volume (\sim mm to \sim m)
- Grid
 - Gain region (\sim 50 μ m)
- Pixel readout chip



Chip post processing

- Apply protection layer
 - Discharge quenching
- Apply Ingrid
 - Gain region

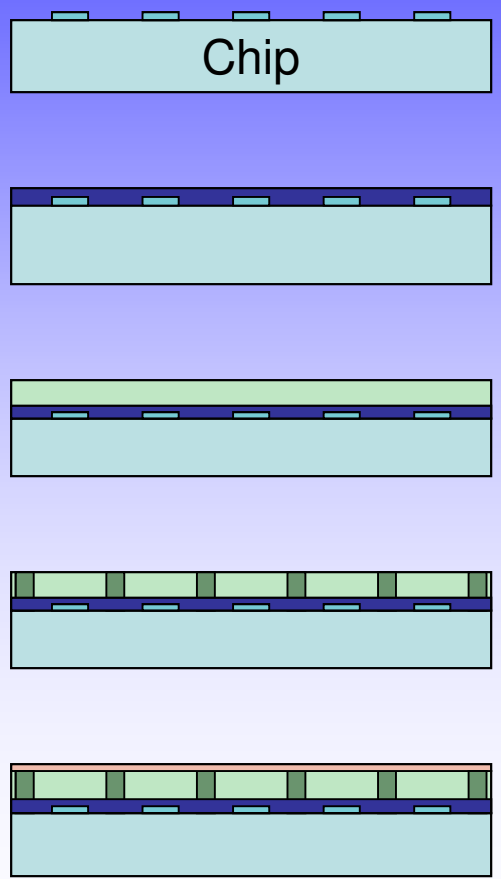
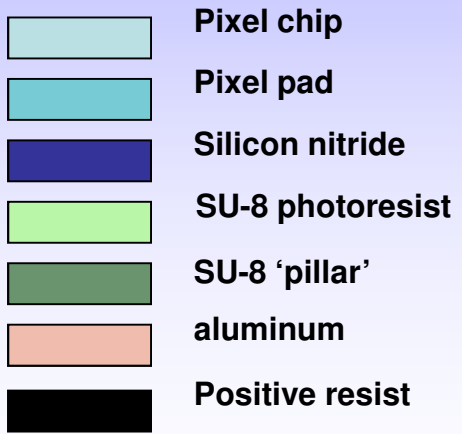
- Si_3N_4 , silicon rich silicon nitride high res layer
- Charge pileup during discharge



Chip post processing

Chip

- TimePix
- PSI-46
- Gossipo-2



- Start with naked chips on square

- Si_3N_4 in Multiple steps to prevent overheating

- Spin coating of SU8

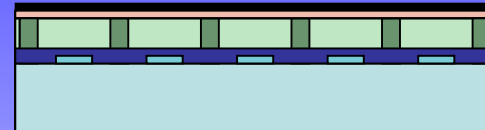
- Exposure for pillars

- alu in Multiple steps to prevent SU8 crosslinking

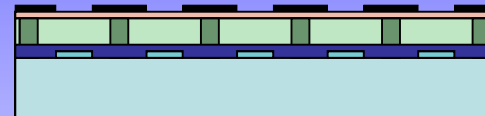
Chip post processing

Chip

TimePix
PSI-46
Gossipo-2



- photoresist on alu

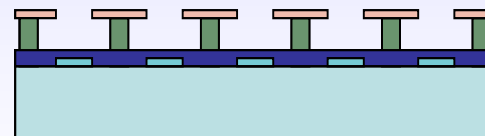


- expose and develop



- etch alu

Dicing



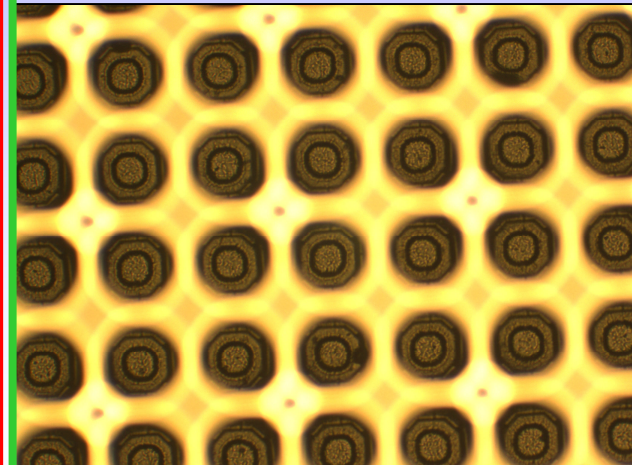
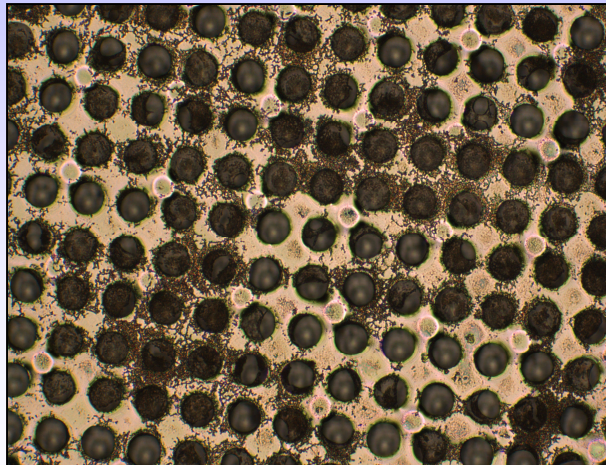
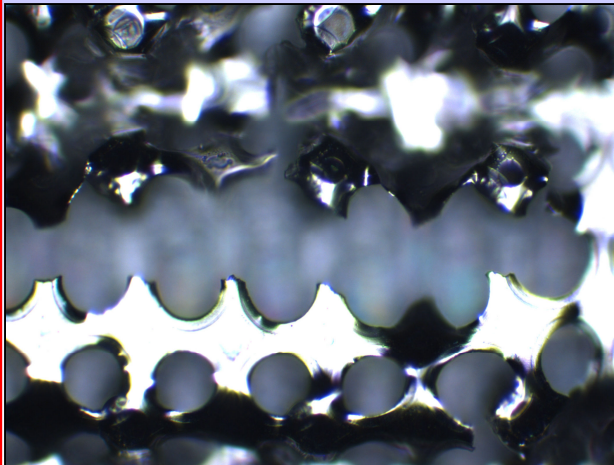
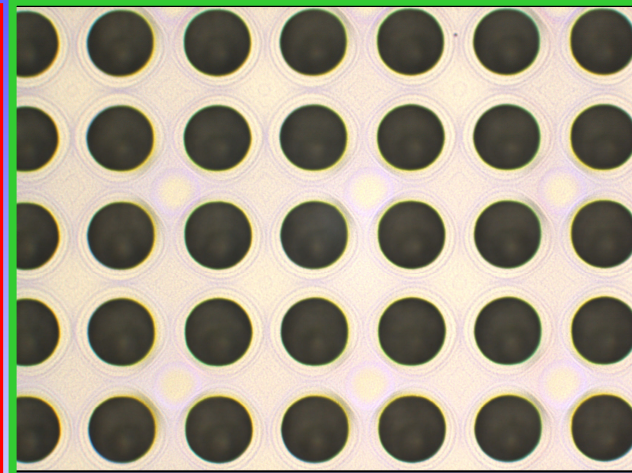
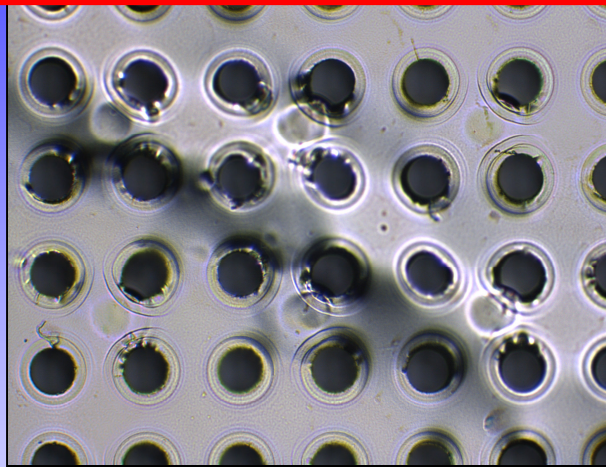
- try not to damage alu, apply temp layer of photoresist

- develop SU8

- Pixel chip
- Pixel pad
- Silicon nitride
- SU-8 photoresist
- SU-8 'pillar'
- aluminum
- Positive resist

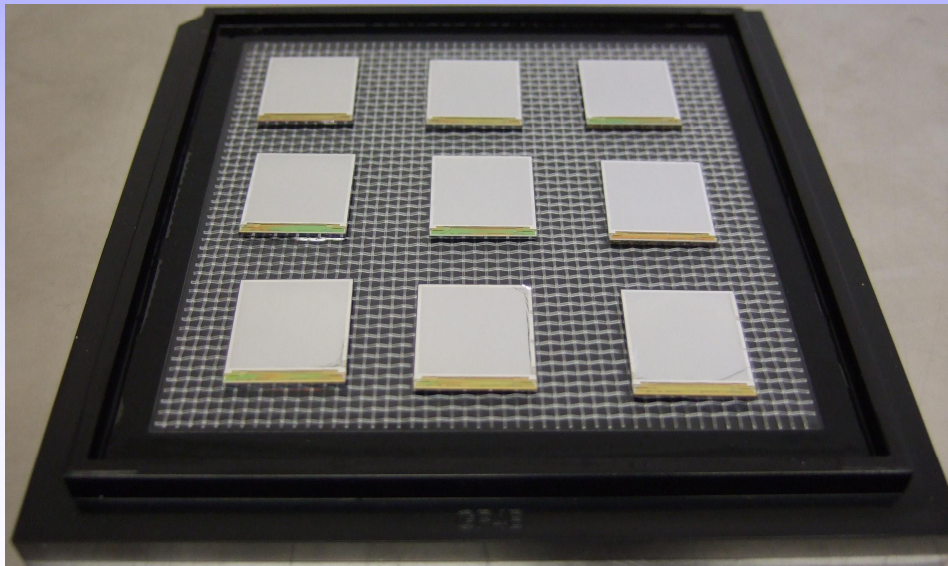
Chip post processing

- A lot of things can go wrong



Chip post processing

- Since October 2009 acceptable yield from parallel processed TimePix chips
- First batch of those to Saclay (finally!) for end modules

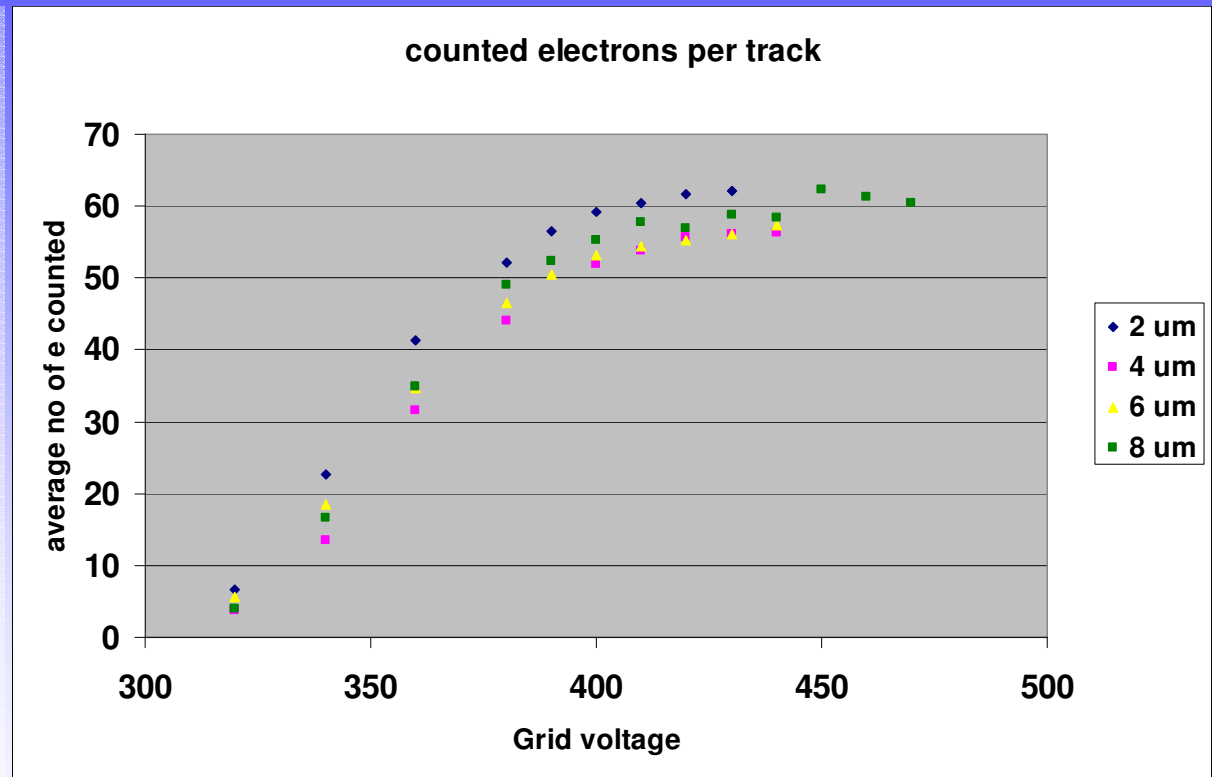


Beamtests at DESY

- Few GeV e^- to test;
- Signal development
- When do the chips break down?
(this is, of course, the last test to be performed)
- The Gridpix detectors:
- TimePix chips with 2,4,6, and 8 μm silicon nitride
- 11.5 mm drift gaps
- Used gases:
 - Ar/ISO 80:20
 - He/ISO 80:20
 - T2K, Ar/CF₄/ISO 95:3:2
 - Ar/CO₂ 70:30
 - He/CO₂ 70:30

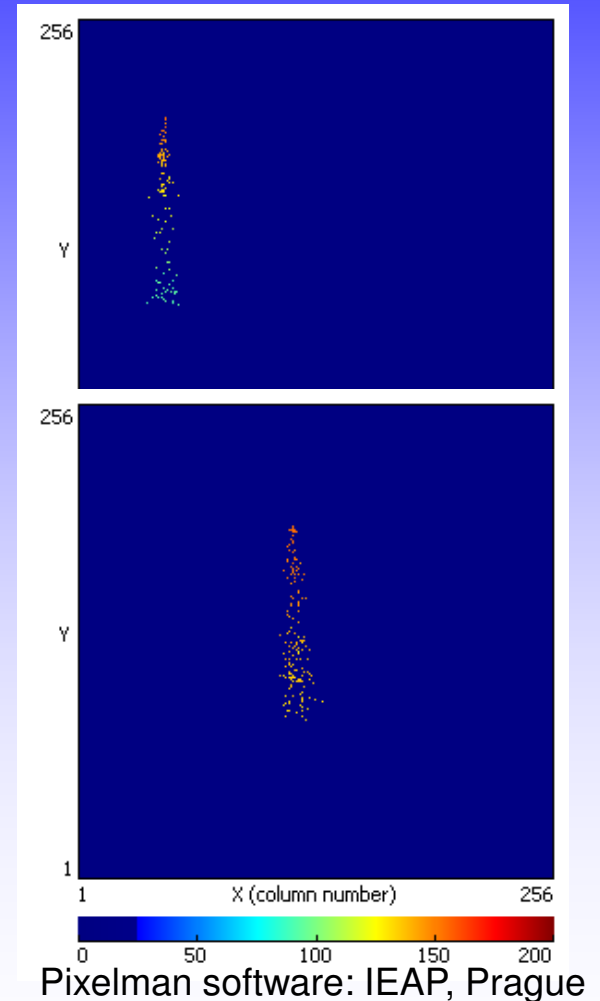
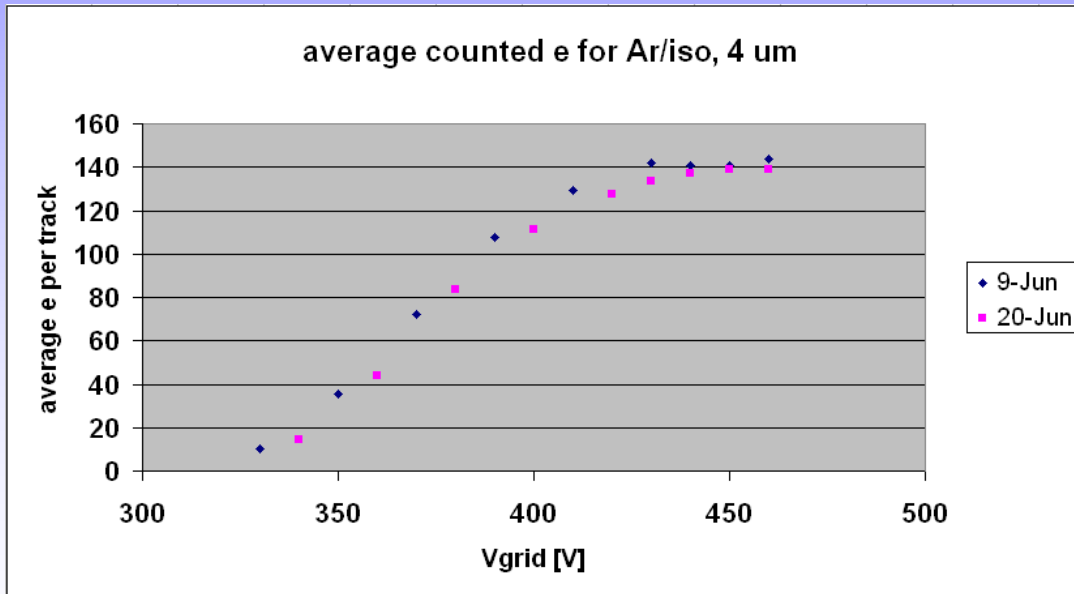
Beamtests at DESY

- (pretty) raw data
- He/ISO 80:20
- E drift = 450V/cm
- counting electrons per track.
- compare this per chip.
- Until sparking (and the 8 um a bit further)



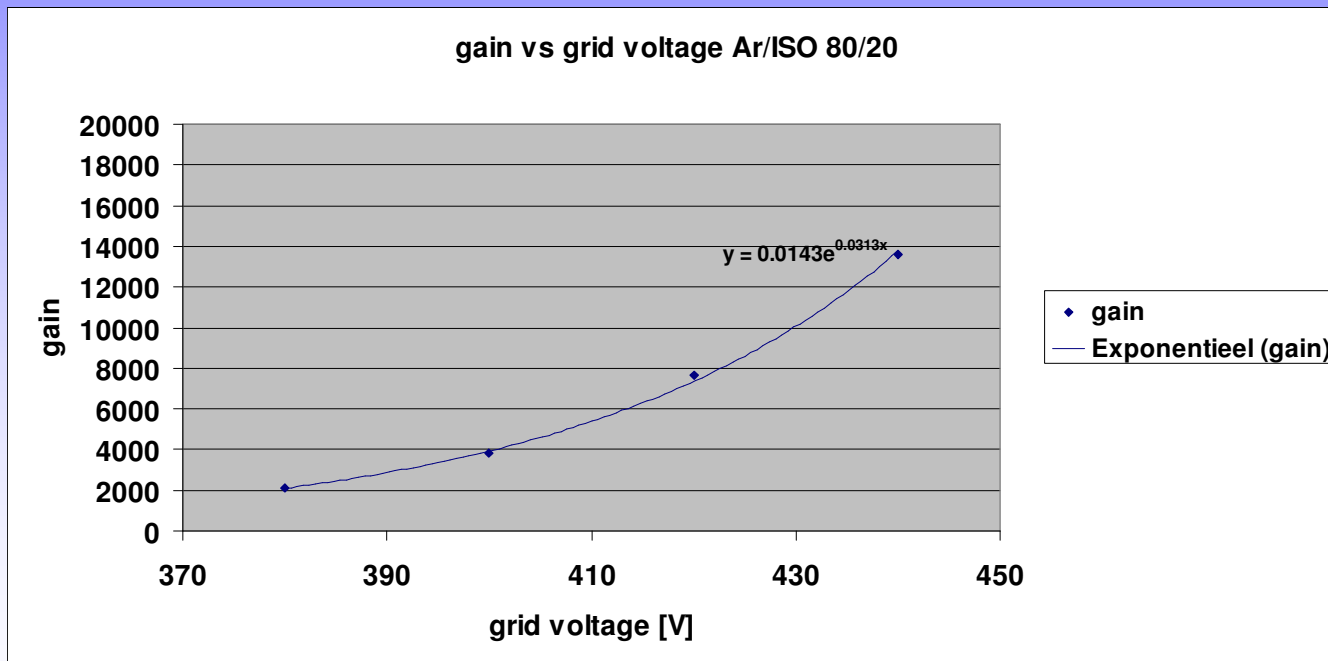
Beamtests at DESY

- Ar/ISO 80:20
- E drift = 900V/cm
- continue using the 4 um chip
- For other gasses no plateau reached



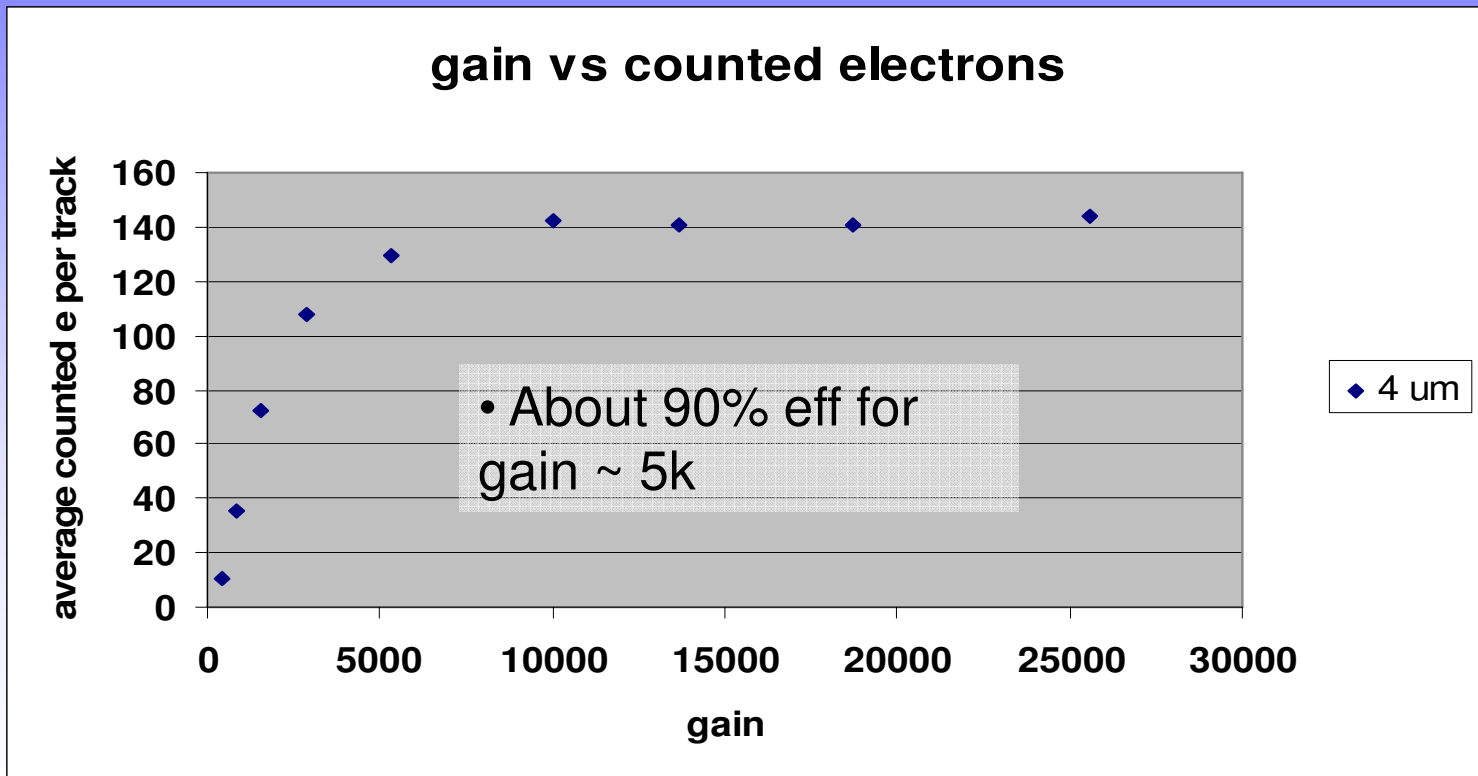
Beamtests at DESY

- Ar/ISO 80:20
- Use 55Fe
- Give or take 50%



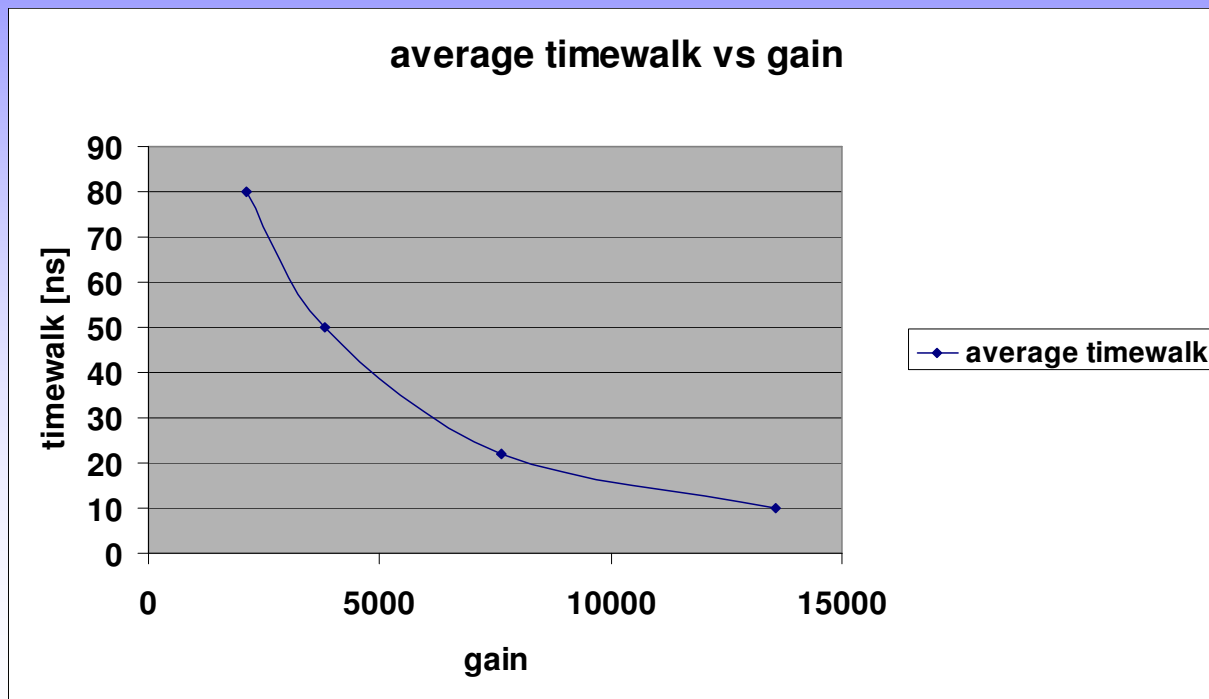
Beamtests at DESY

- Ar/ISO 80:20



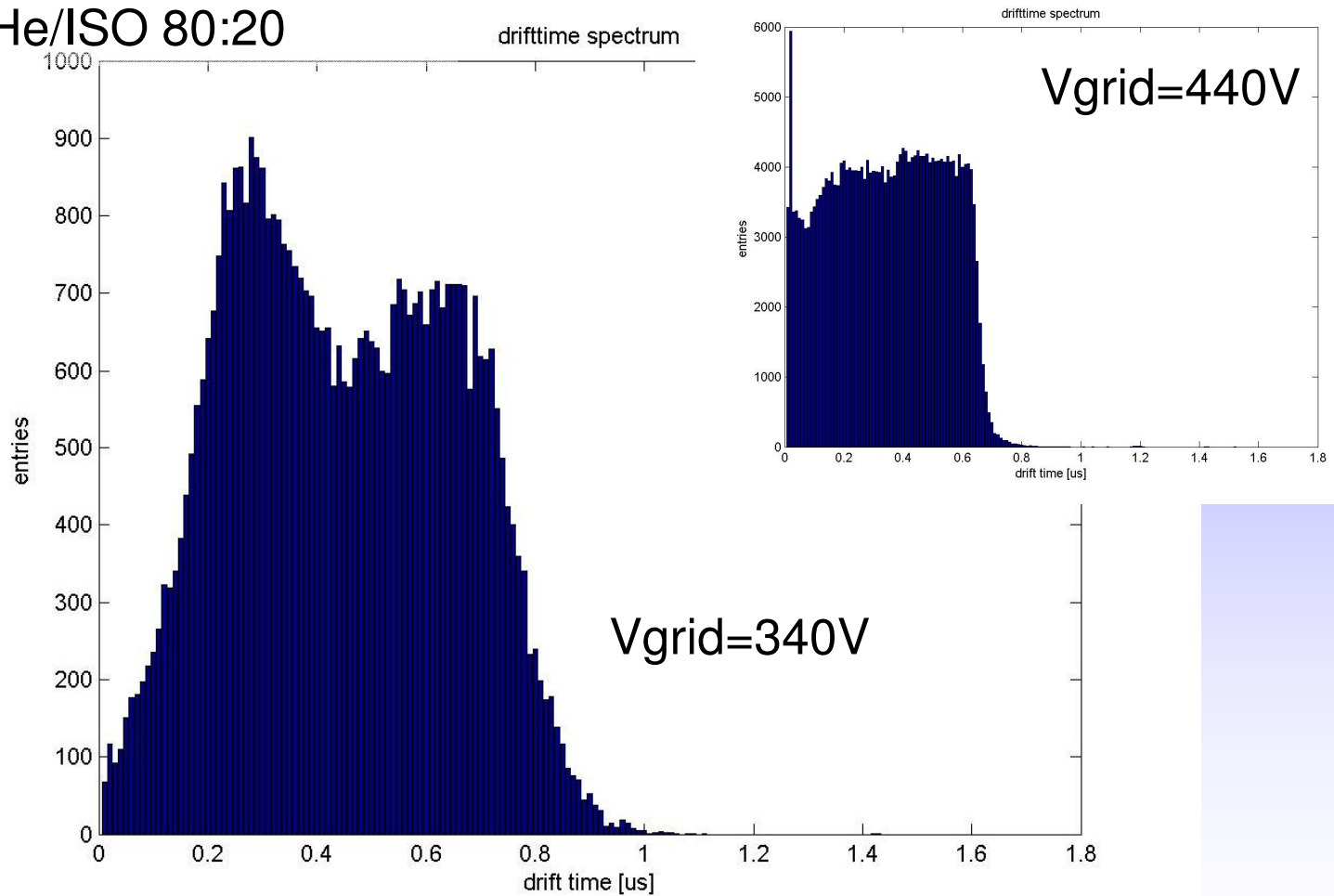
Beamtests at DESY

- Ar/ISO 80:20
- probably worse for low gains



Beamtests at DESY

- He/ISO 80:20

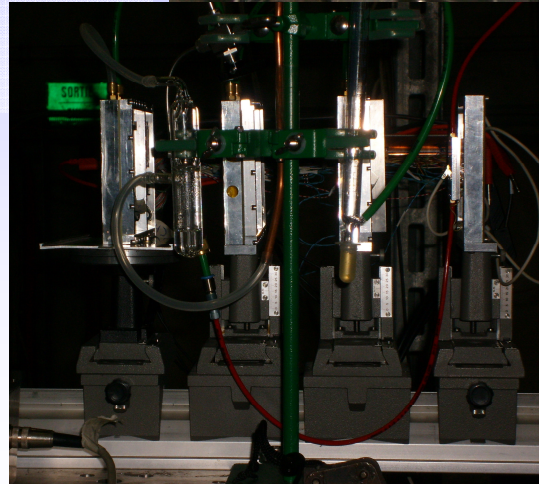
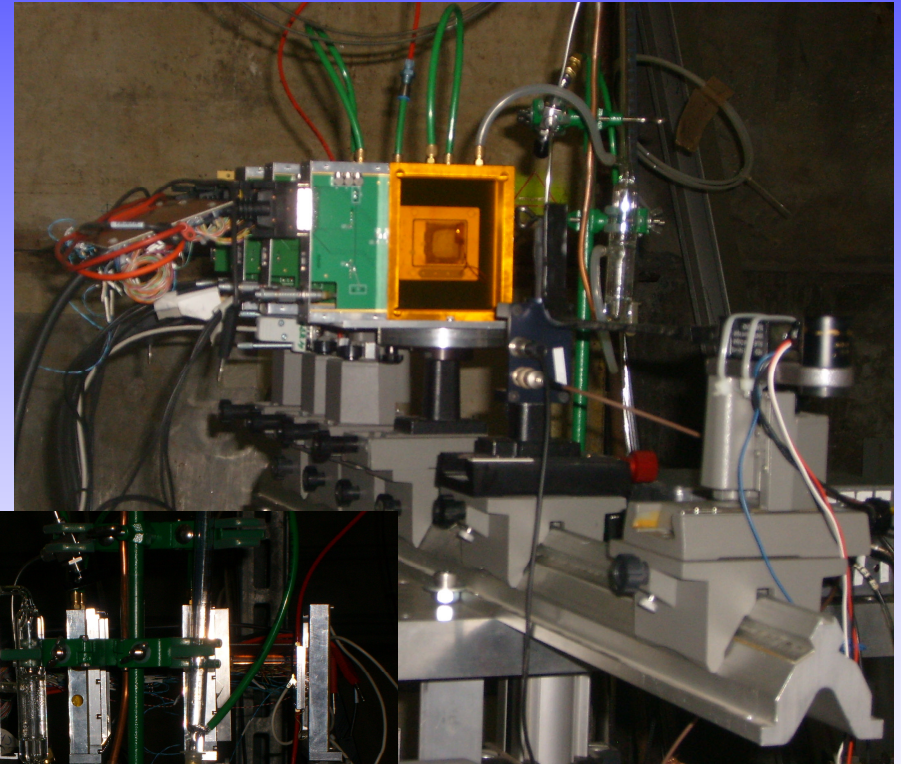


Beamtests at DESY

- And finally destruction...
- After hours of suffering >2 sparks/sec, the 4 μm chip is still doing fine BUT:
- After few more days, under normal operation:
 - The 6 μm dies (Ar/ISO 80:20, Vgrid -430V)
 - 10 days later the 2 μm dies (He/CO2 70:30, Vgrid -520V)
 - Another 6 days, the 4 μm (T2K, Vgrid -360V)
- All breakdowns are similar, regardless of thickness of SiNi Layer.

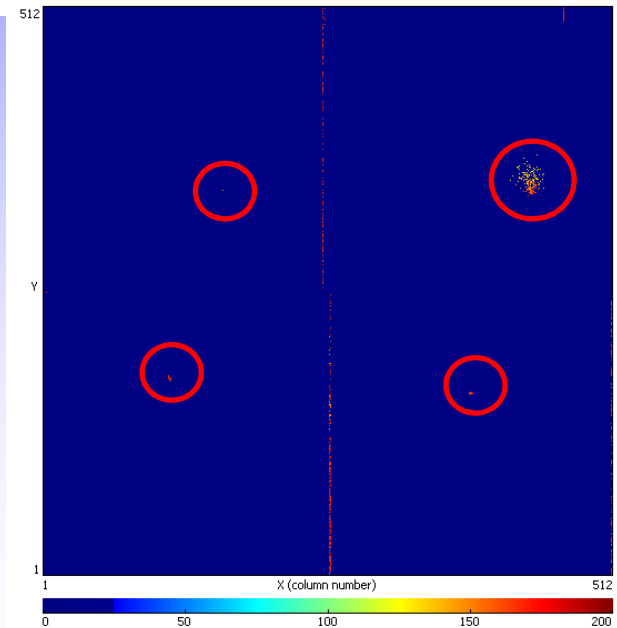
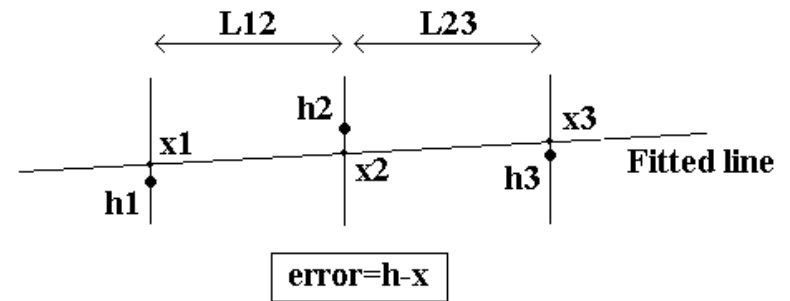
Beamtests at CERN

- TimePix chips
- 3 X Gossip and DICE in series
- DICE drift length 19.5 mm
- Gossips: 1, 1.4 and 1.5 mm drift
- Ar/ISO 80:20 and CO₂/DME 50:50
- E drift = 900V/cm and 2kV/cm



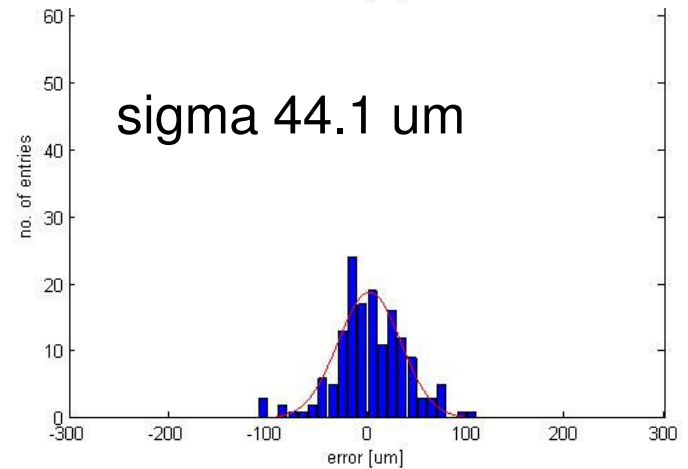
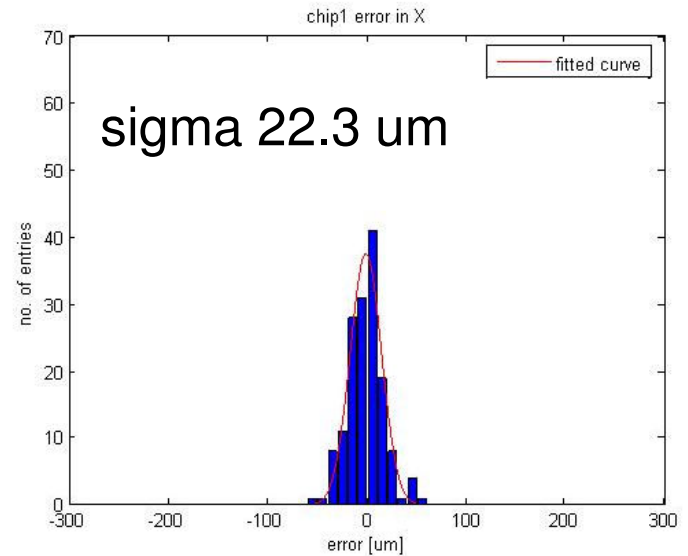
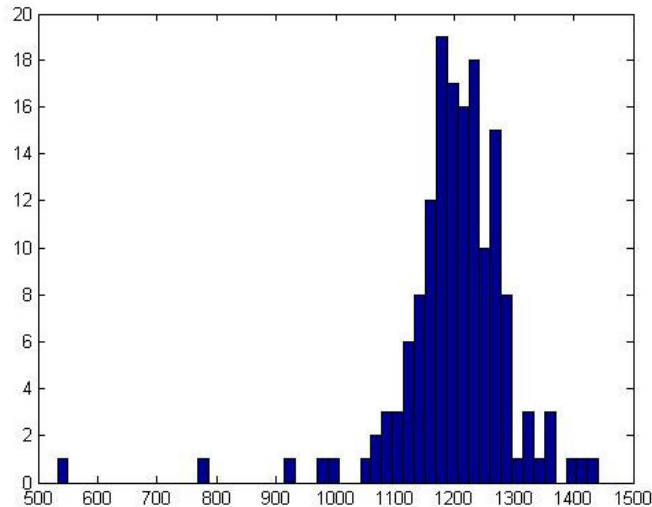
Beamtests at CERN

- DICE is reference detector
- Determine center of gravities h_1, h_2 and h_3
- No time information used (too much timewalk)
- Determine relative positions of chips
- L_{12}, L_{23} ; distance between detectors
- $X_{1,2,3}$; best fit



Beamtests at CERN

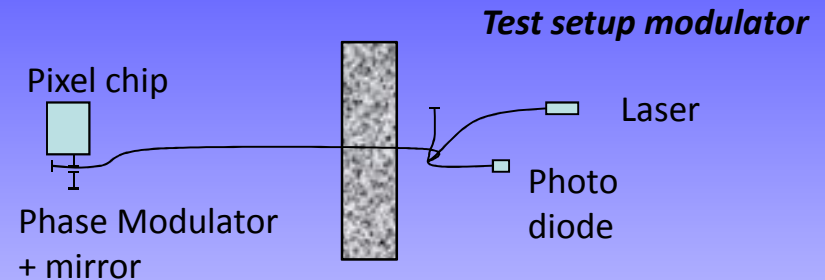
- 150 GeV “stuff” from SPS
- Ar/ISO 80:20



Iflink

- Optical data connection
 - based on interferometer
 - Laser and sensor outside detector
-
- Low material budget
 - Low power requirement inside detector
 - Fast, Gb/s

H vd Graaf, Nikhef, Amsterdam
vdgraaf@nikhef.nl



- First tests done
- Issues to work on:
 - sensitivity
 - Rad hard?
 - Noise (one interferometer 'arm' in 'rough' environment)

- optical 'twisted pair'

Optical powering

- Investigate feasibility for an optical power connection
- Lots of lasers through lots of fibers to distribute power.
- Why?
- Low material budget $\text{Cu} \rightarrow \text{SiO}_2$
(remember, high I low V required)
- Power pulsing easily possible
- floating electronics (less pickup, no groundloops, no serial powering problems etc.)

- since a few years, multi W ~ 808 nm lasers are affordable
- commercial laser efficiency 40-50% ($\sim 60\%$ in lab experiments)
- Theoretical P_i to P_e conversion $>60\%$ efficient for single wavelength for kW/cm^2 .

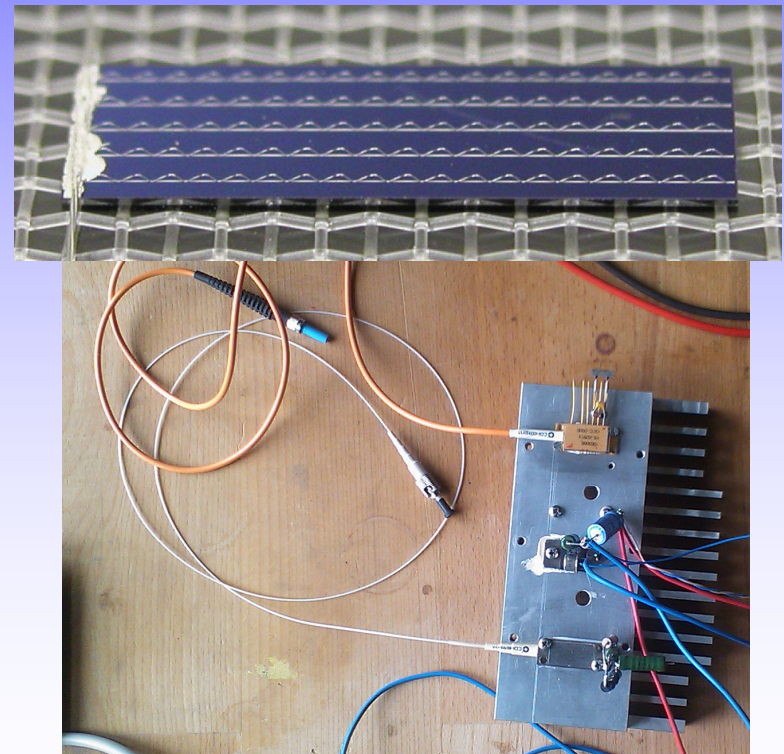
H. Miyakawa et al. / Solar Energy Materials & Solar Cells
86 (2005) 253–267

- about 40-50% eff for present power supplies (cable losses)
- In this case 15-30 % efficiency

Optical powering

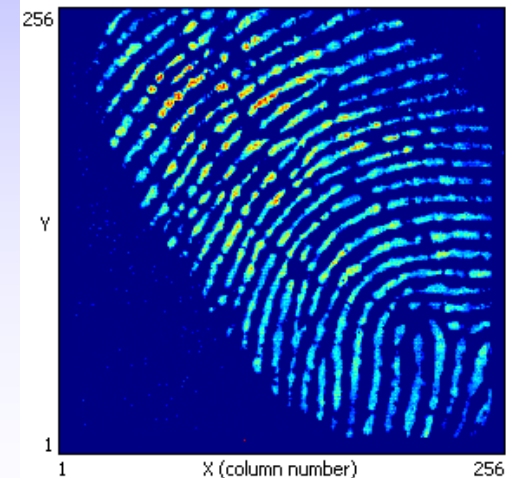
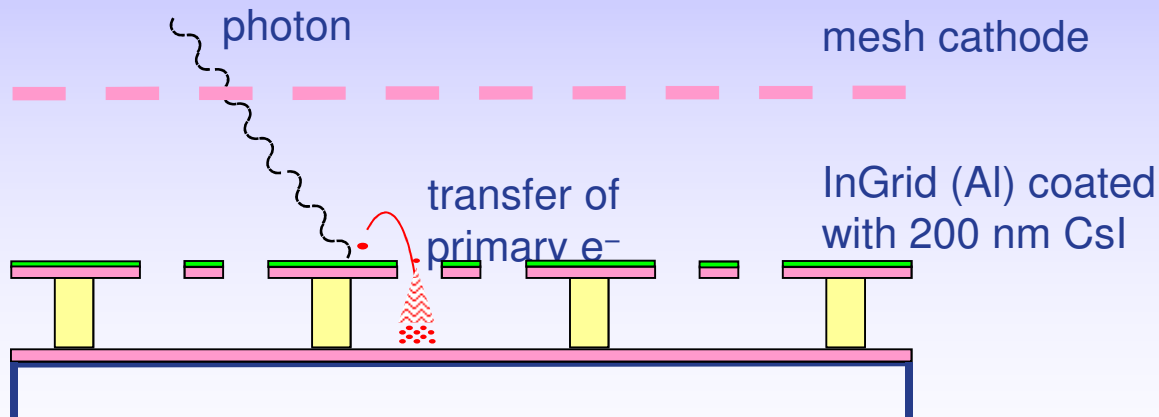
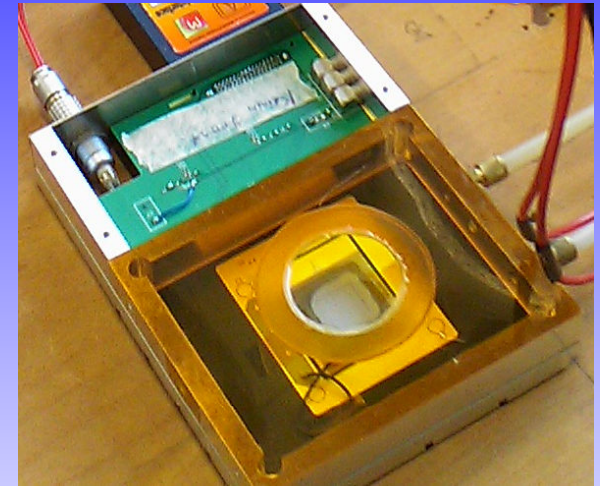
- Some naïve numbers:
- Assume 'thick' 250 μm fibers
- 30 kW power needed
- 2-3 W laser light per fiber
- 1 W electrical output per fiber \rightarrow
- 30000 fibers needed, bundle of ~ 5 cm
- Lots of heat at the wrong place (CO₂ cooling?)
- Expensive? ($\sim 500\text{k}$ EUR on lasers)

- Rad hard? (fiber, PD)
- Other practical problems?



'Optical' Gridpix

- Univ. Twente and Weizmann institute
- Timepix with 80 μm InGrid
- Gossip detector set up
- UV light source D₂ lamp



Summary

- Reproducible parallel postprocessing possible
- a good 4 um silicon nitride layer is sufficient spark protection
- But what causes that still sometimes a chip dies?
- for He/iso and Ar/iso mixture we can run with $e_{eff} > 90\%$
- Do more analysis on the data
- use data to verify/improve Gridpix simulations
- Investigate improvement of Ilink
- Investigate feasibility of optical powering

Questions? (or remarks)