IN2P3

Omega

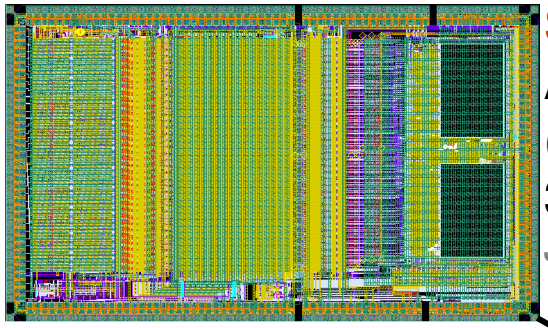
CALICE/EUDET FEE

status

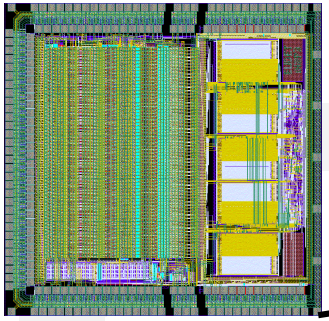
C. de LA TAILLE

Orsay MicroElectronic Group Associated

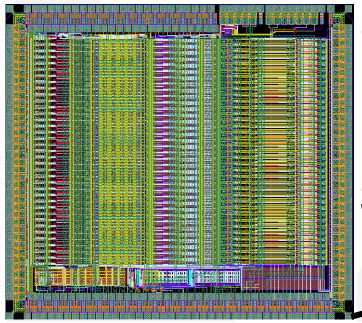
ILC front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

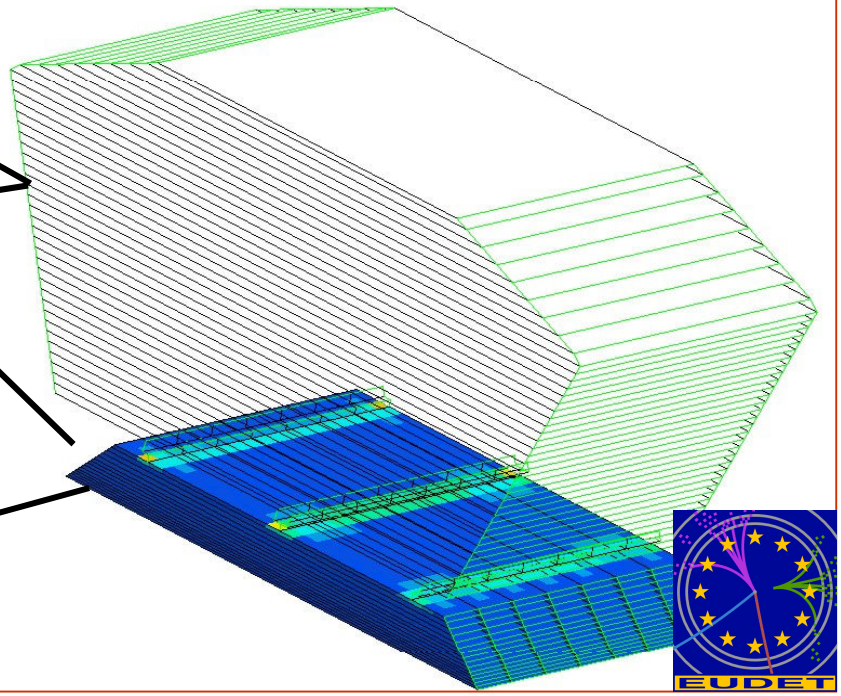


HARDROC
Digital HCAL
(RPC or µmegas)
64 ch. 16mm²
Sept 06



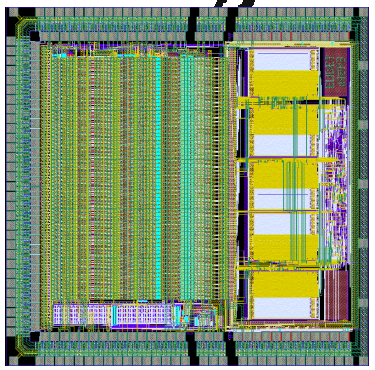
SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

- Technological prototypes : full scale modules (~2m)
- EUDET EU funding (06-09)
- ECAL, AHCAL, DHCAL
- B=5T

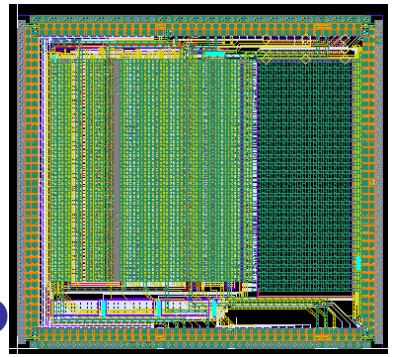


HaRDROC status

- 240 chips HARDROC1 produced in june 2007 to equip 4-chip and 24-chip RPC and Micromegas detectors
  - Package PQFP240
  - Not completely power-pulsed

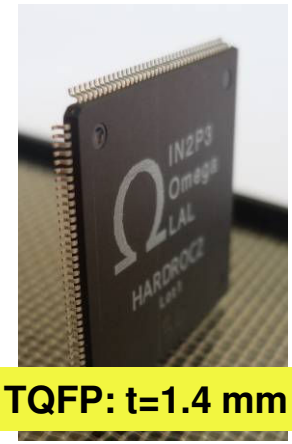


- 400 chips HARDROC2 produced in june 2008 to equip 24-chip RPC and Micromegas PCBs for square meter
  - 3 thresholds (0.1-1-10 pC)
  - Power pulsed to 5-8 µW/ch
  - Package TQFP160
  - **Some difficulties loading Slow Control : SOLVED in HARDROC2B** (submitted in June 09 for a medical application)



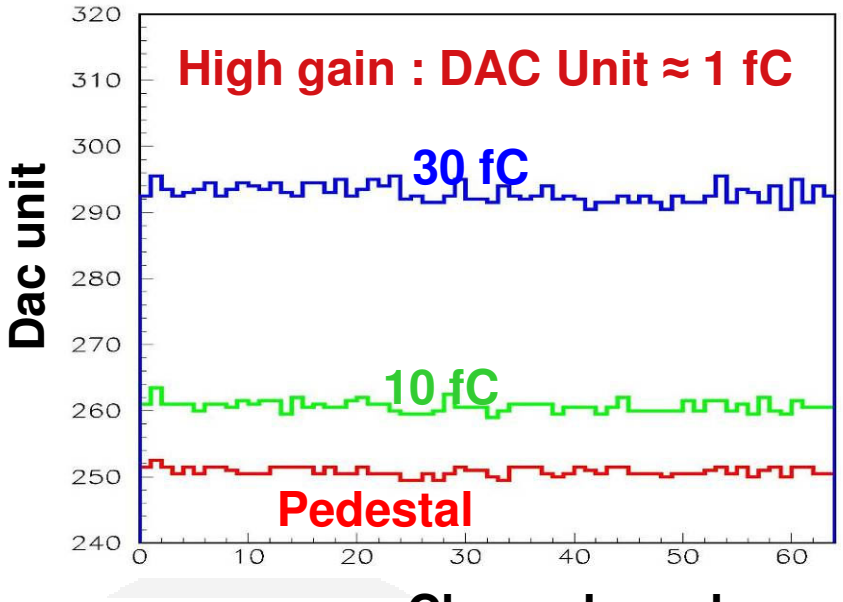
- Essential for readout + DAQ2 validation

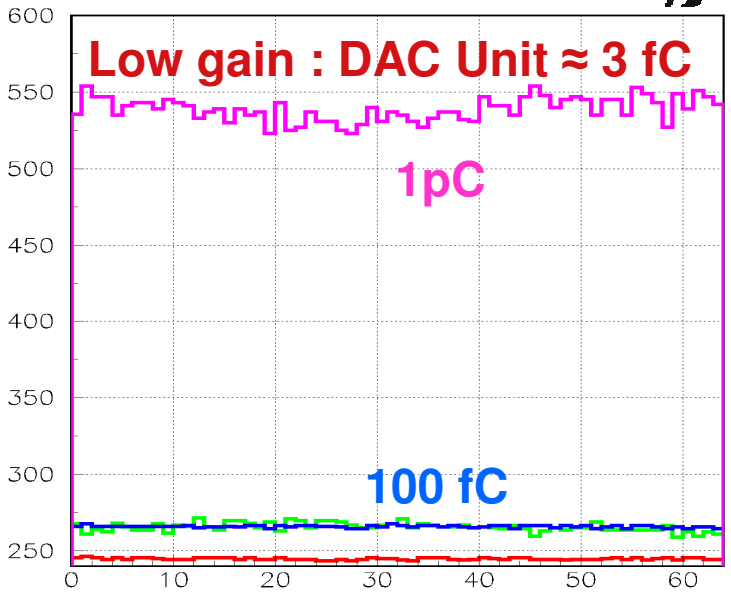
- Full production run: in 2010
  - Paid by french ANR project (I. Laktineh)

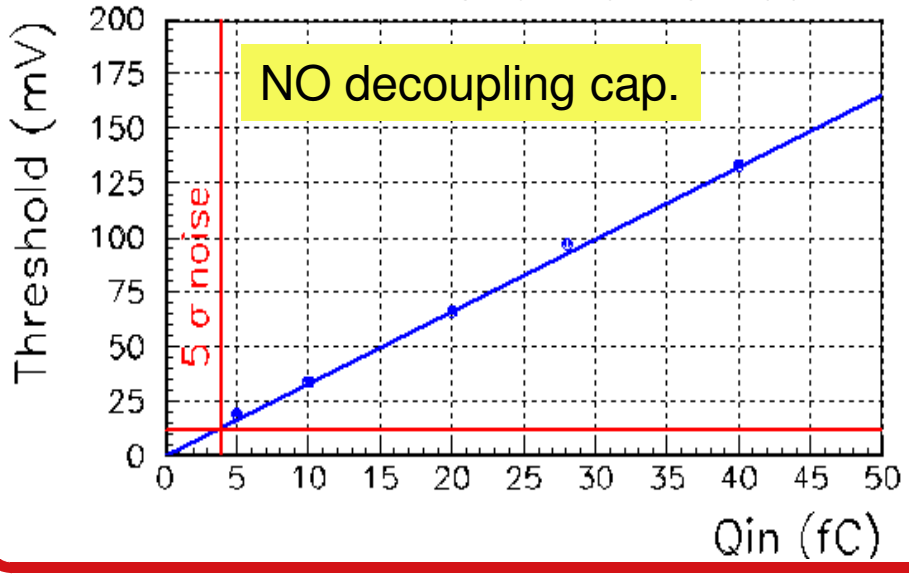


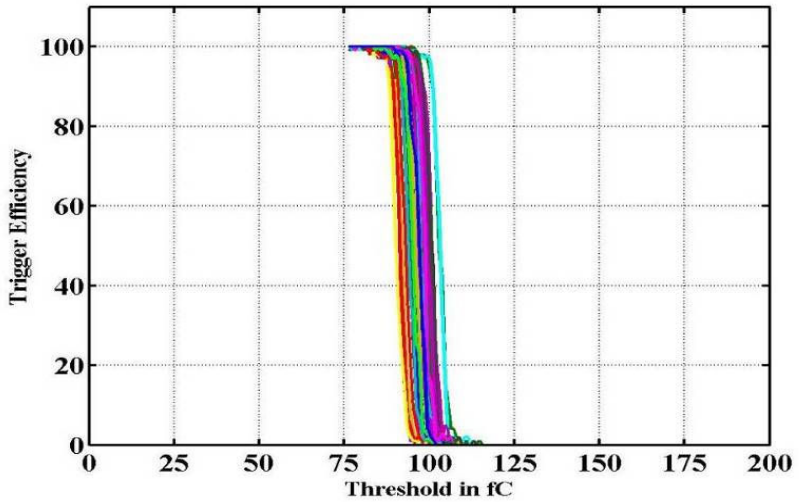
TQFP: t=1.4 mm

Trigger efficiency measurements



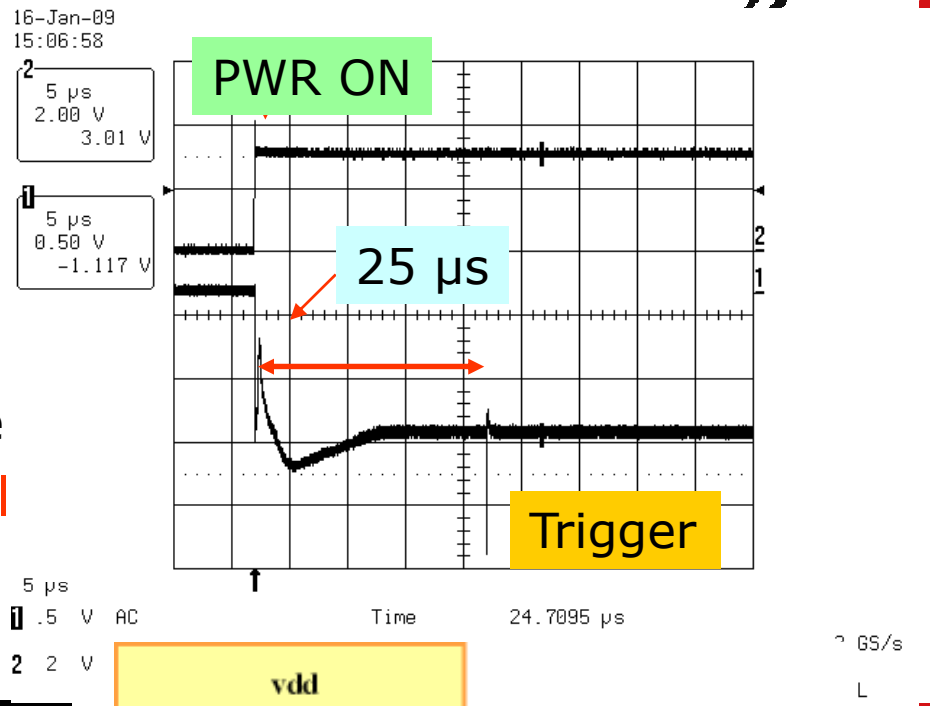




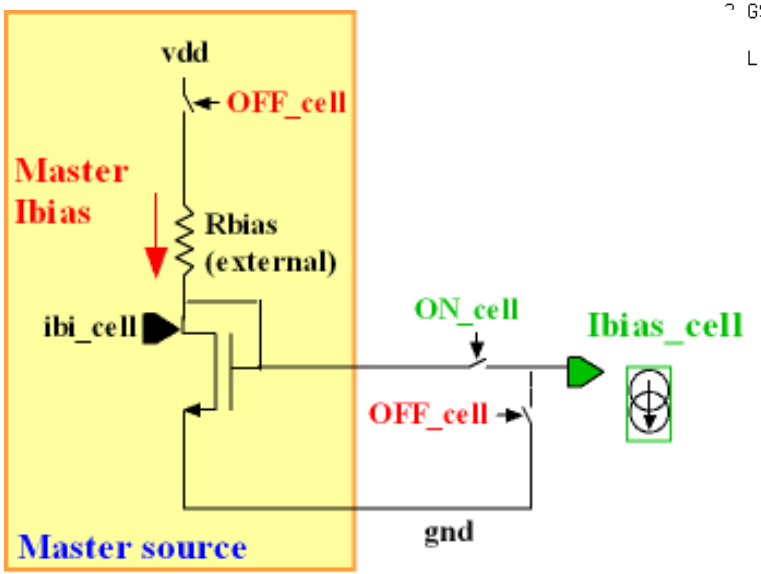


Power pulsing

- Total power on : 100 mW
- Total power off : 10 µW
- Power dissipation
  - 1.5 mW/ch continuous
  - 25 µs awake time
  - 7.5 µW/ch with 0.5% duty cycle
- 10 µW/ch = 24h operation of ful slab with 2 AAA batteries !

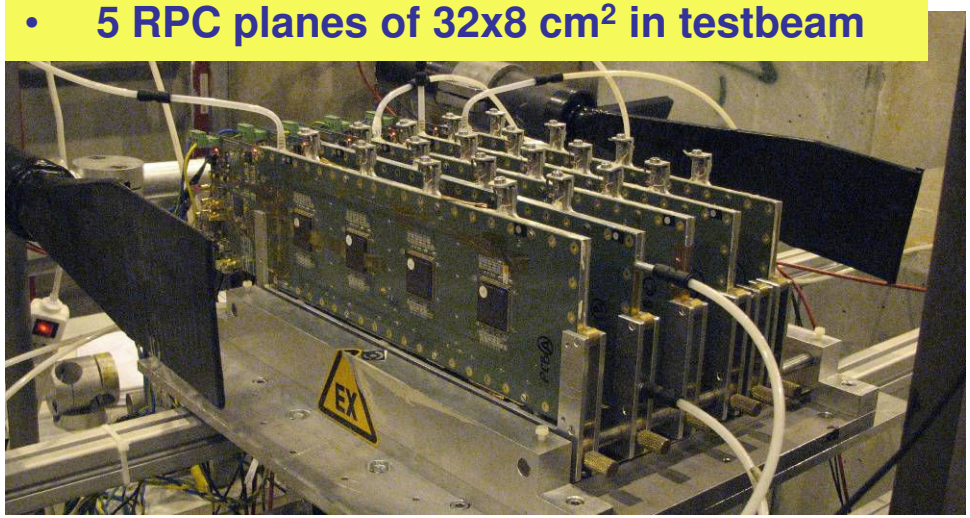


PA	5.46mA	DAC	0.84mA
3 FSB	12.3mA	BG	1.2mA
SS	*9.3mA*	vddd	0.67mA
3 Discris	7.3mA	vddd2	0.4mA (=0 if 40MHz OFF)
TOTAL	38mA		



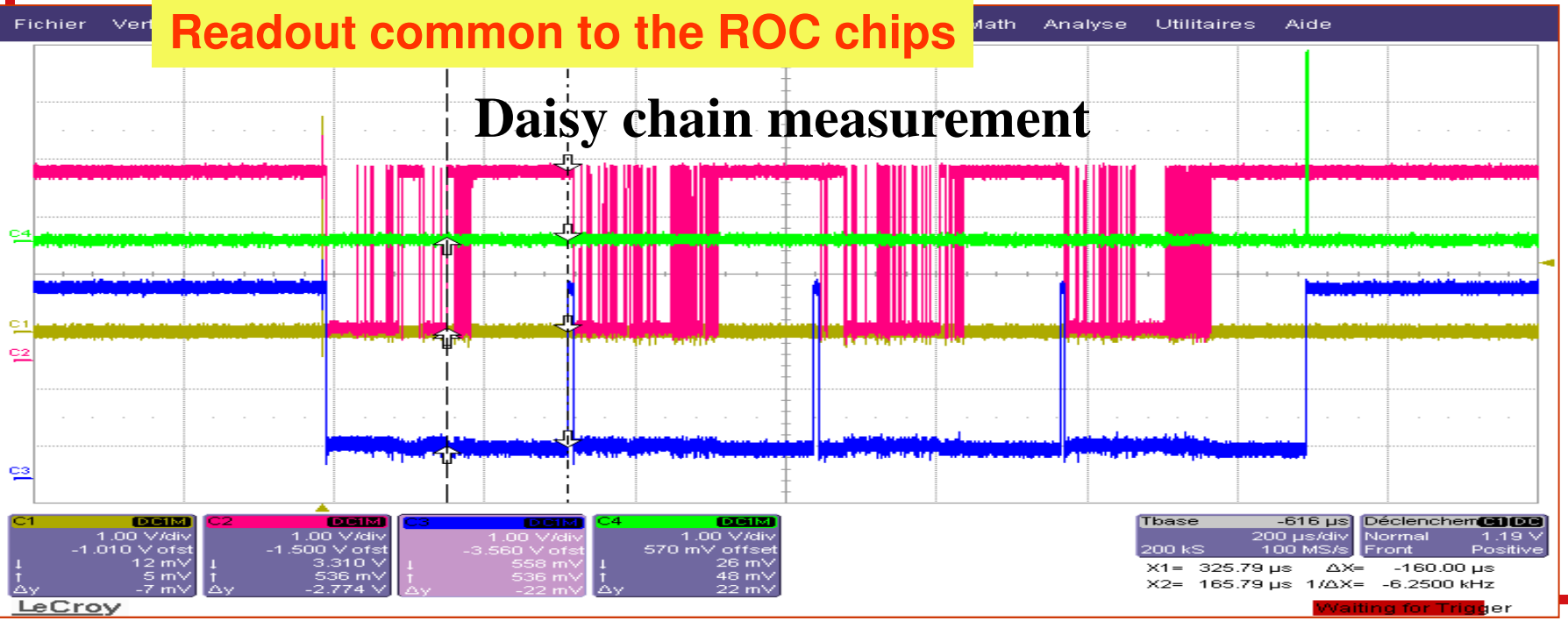
Readout validation with HARDROC (2008)

- **5 RPC planes of 32x8 cm^2 in testbeam**



To validate the semi-digital electronics readout system in beam conditions (daisy chain,stability, efficiency, no external componant)

Readout common to the ROC chips



Towards technological prototype (2009)

GRPC

Slab #1

Slab #2

DIF #1

DIF #2

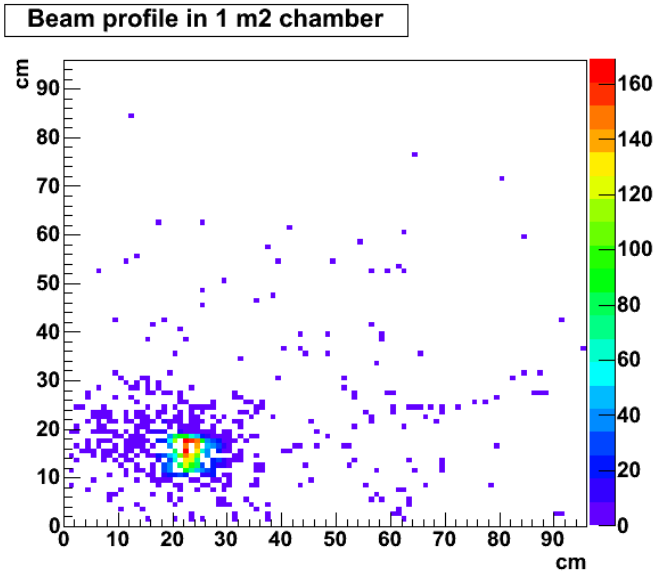
DIF #3

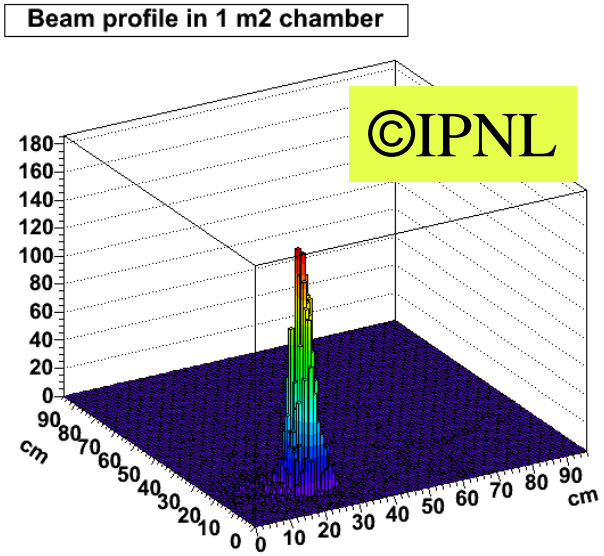
Fully equipped large scalable detector tested in cosmic rays bench and in test beam at CERN in **summer 09** [I. Laktineh et al.]

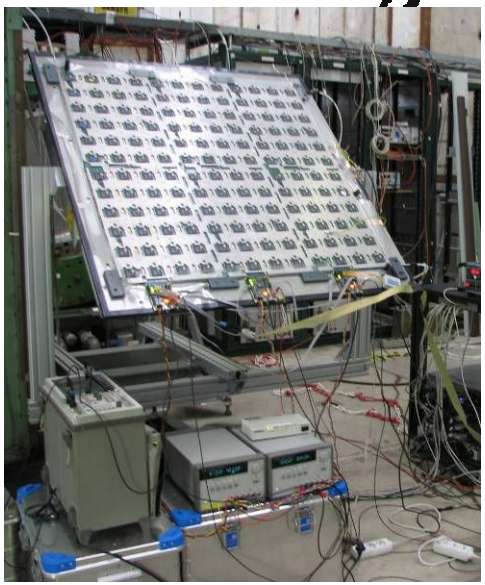
Similar development with µMEGAS [C. Adloff et al.]

A NICE PROOF of INFRASTRUCTURE

1m² in testbeam (CERN, Summer 2009)







Pads over (low) threshold

Up to 93% efficiency

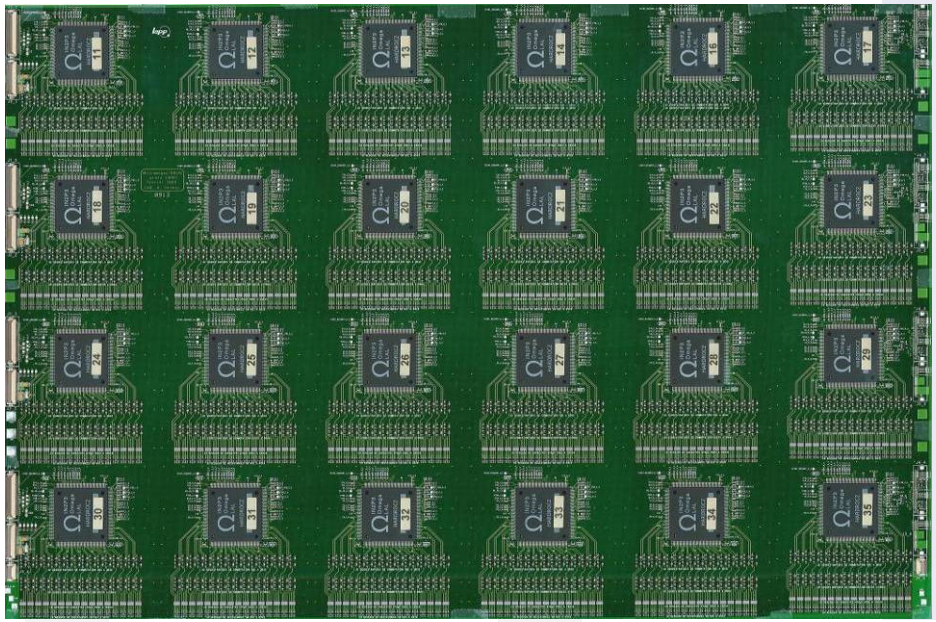
Ready for power pulsing tests

pion /muon beam

MICROMEGAS detector equipped with HR2

- Two 32x48 pad ASU (Active Unit Sensor)
- 24 HARDROC2 chips

©LAPP Annecy



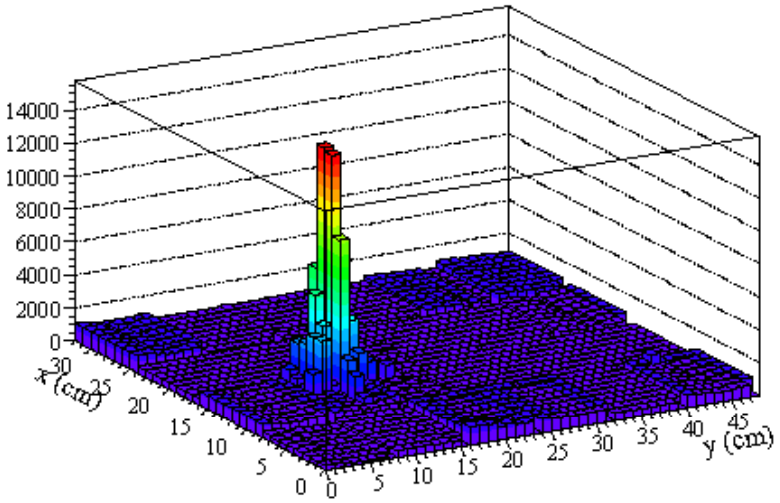
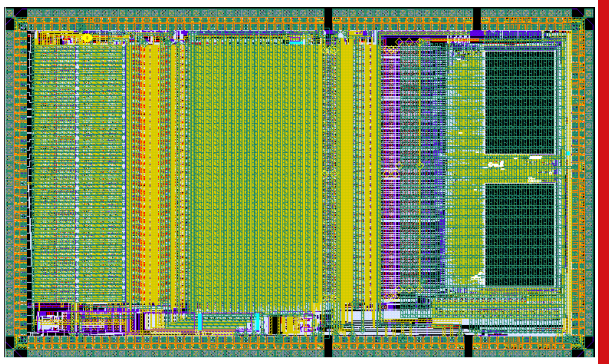


Figure: Response of a 32×48 pad ASU after irradiation with an ^{55}Fe source

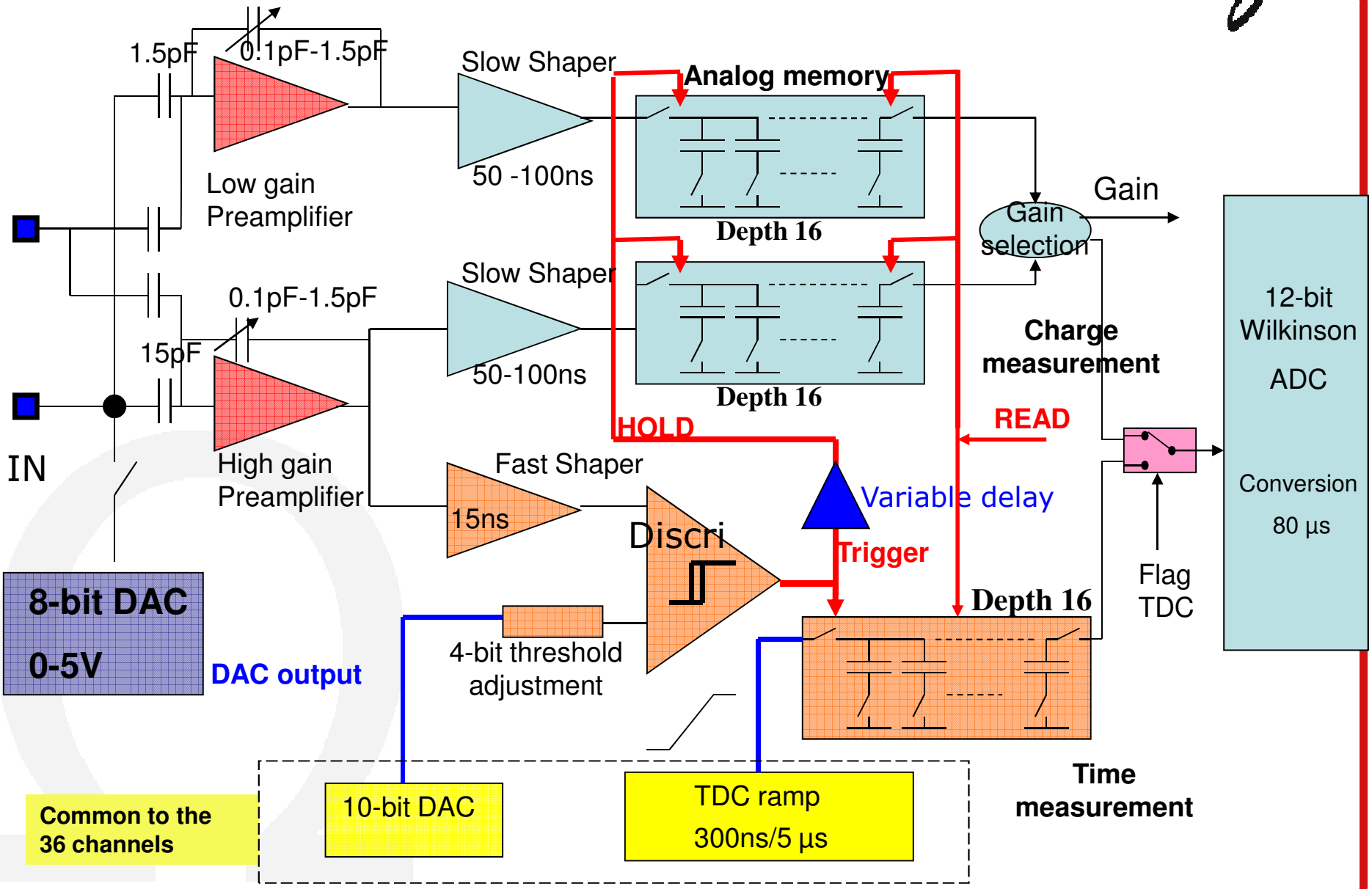
- A $1m^2$ detector equiped with 144 HR2 chips to be tested in test beam this Autumn

SPIROC for AHCAL

- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC **1 pe → 2000 pe**
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout



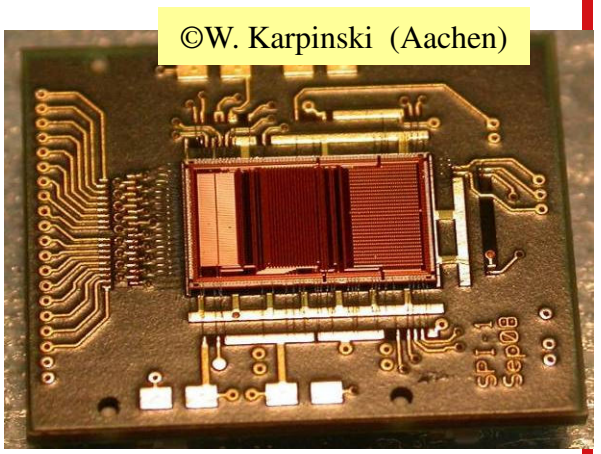
SPIROC : One channel schematic



SPIROC status

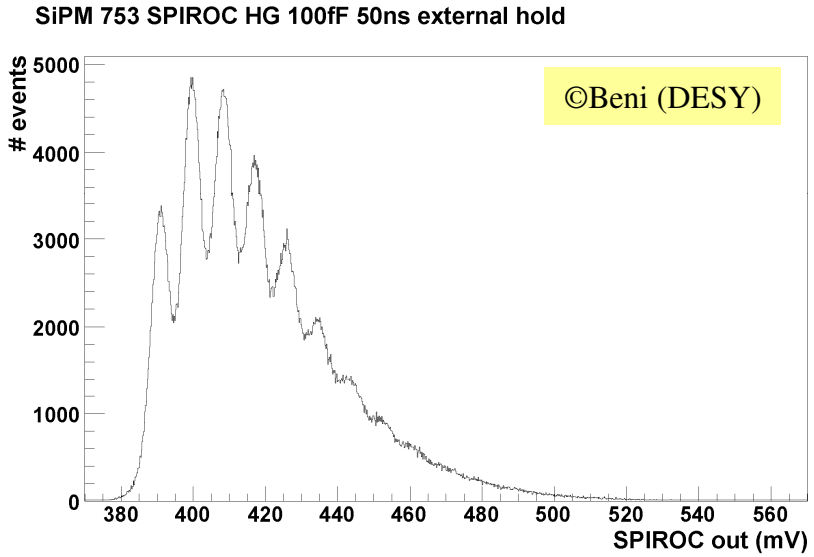
- 200 chips SPIROC1 produced in nov 2006
  - Package PQFP240
  - Good analog performance
  - Bug in ADC ramp : no digital data out !

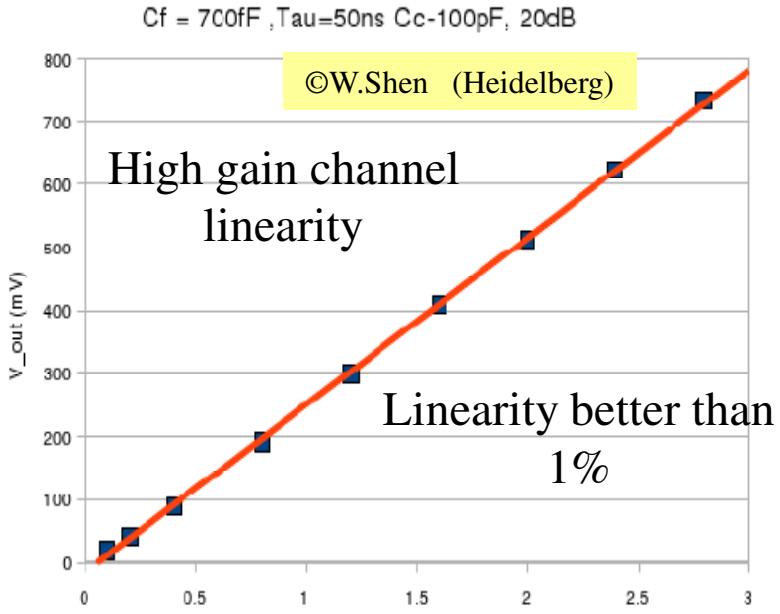
- 50 chips **SPIROC2** produced in june 2008 to equip AHCAL and ECAL EUDET modules
  - **Fulfiled EUDET milestone**
  - Package TQFP208 (w=1.4 mm)
  - Difficult slow control loading (solved in HR2b)
  - Measurements (slowly) coming in
  - Complex chip
  - Collab LAL, DESY, Heidelberg

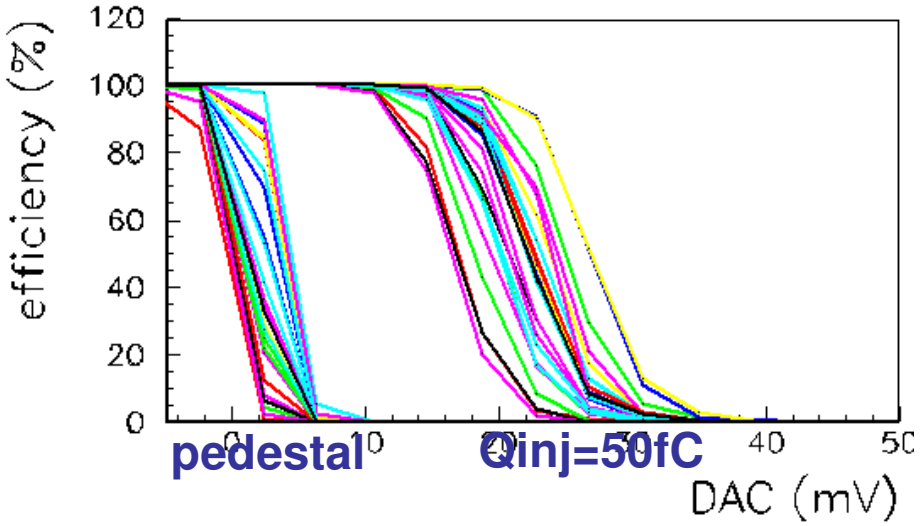


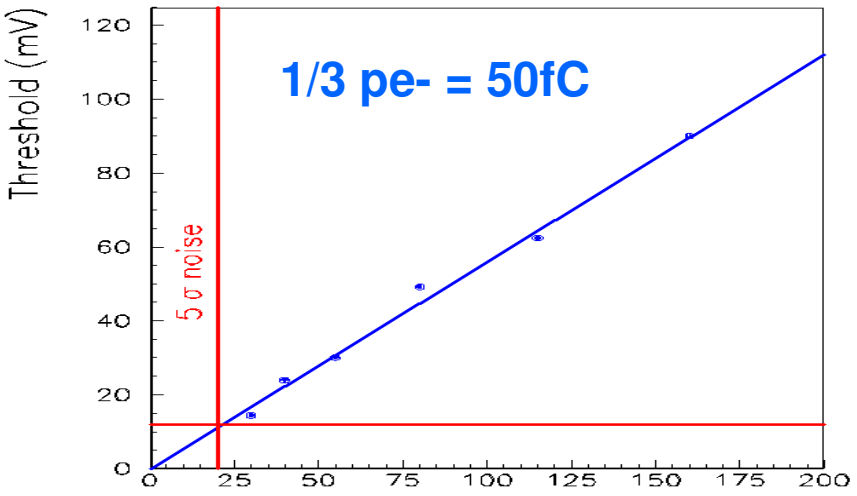
- External requests :
  - astrophysics PEBS (Aachen), medical imaging (Roma, Pisa, Valencia…), nuclear physics (IPNO), Vulcanology (Napoli)

Performance

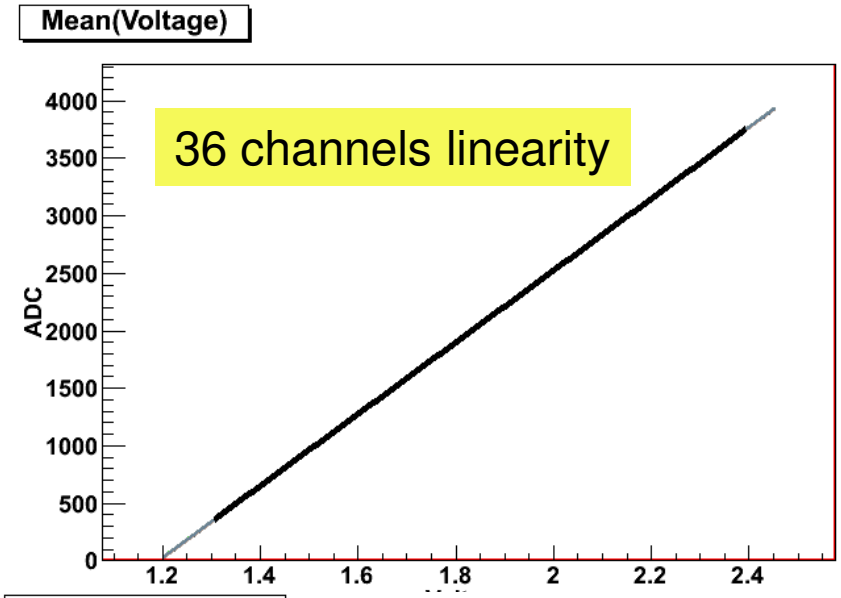


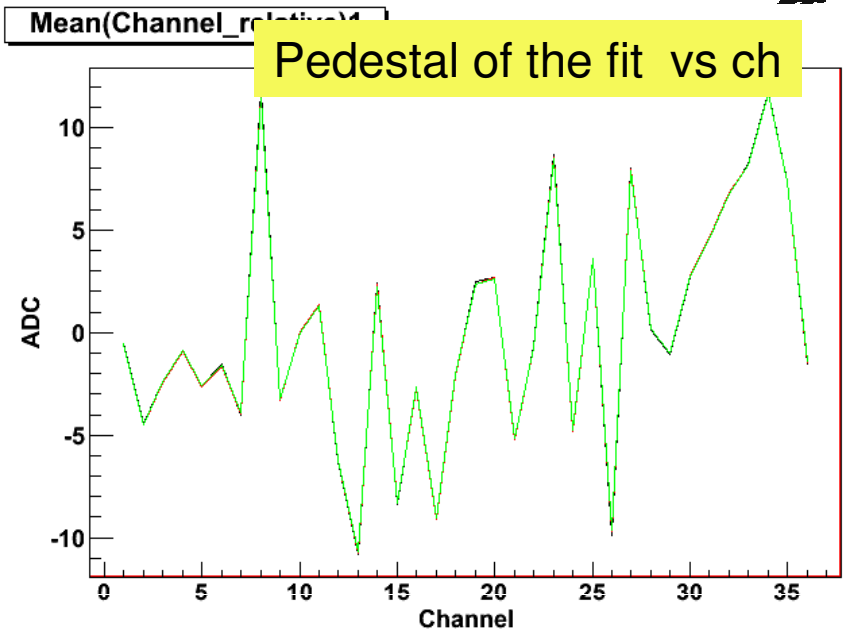


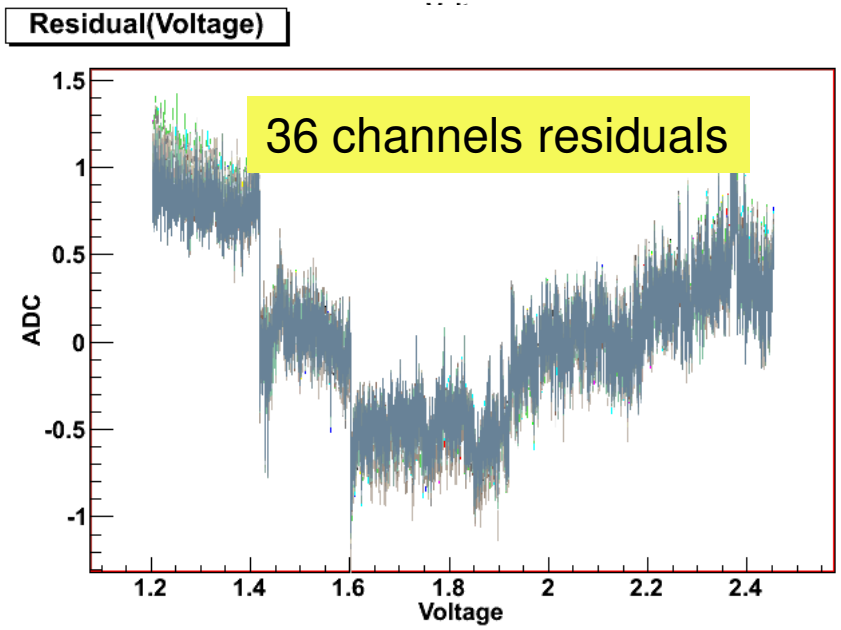


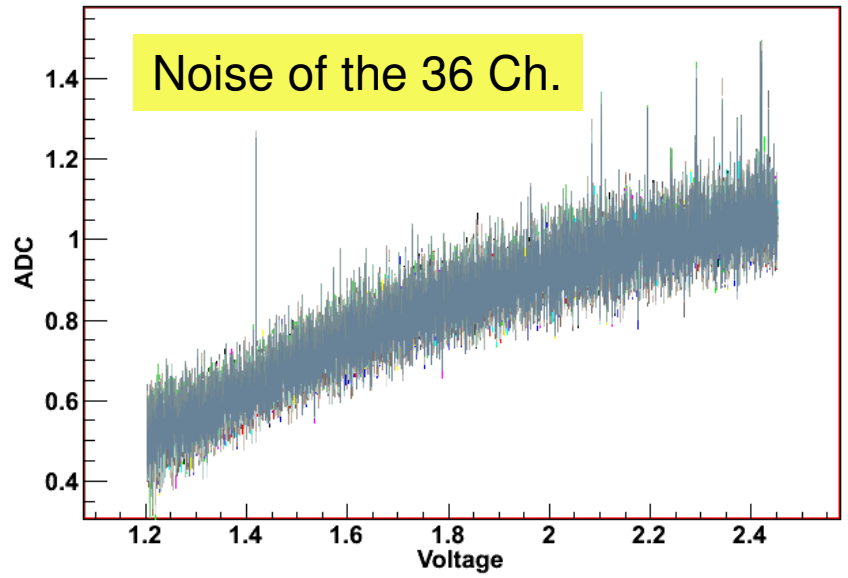


Internal 12-bit ADC performance

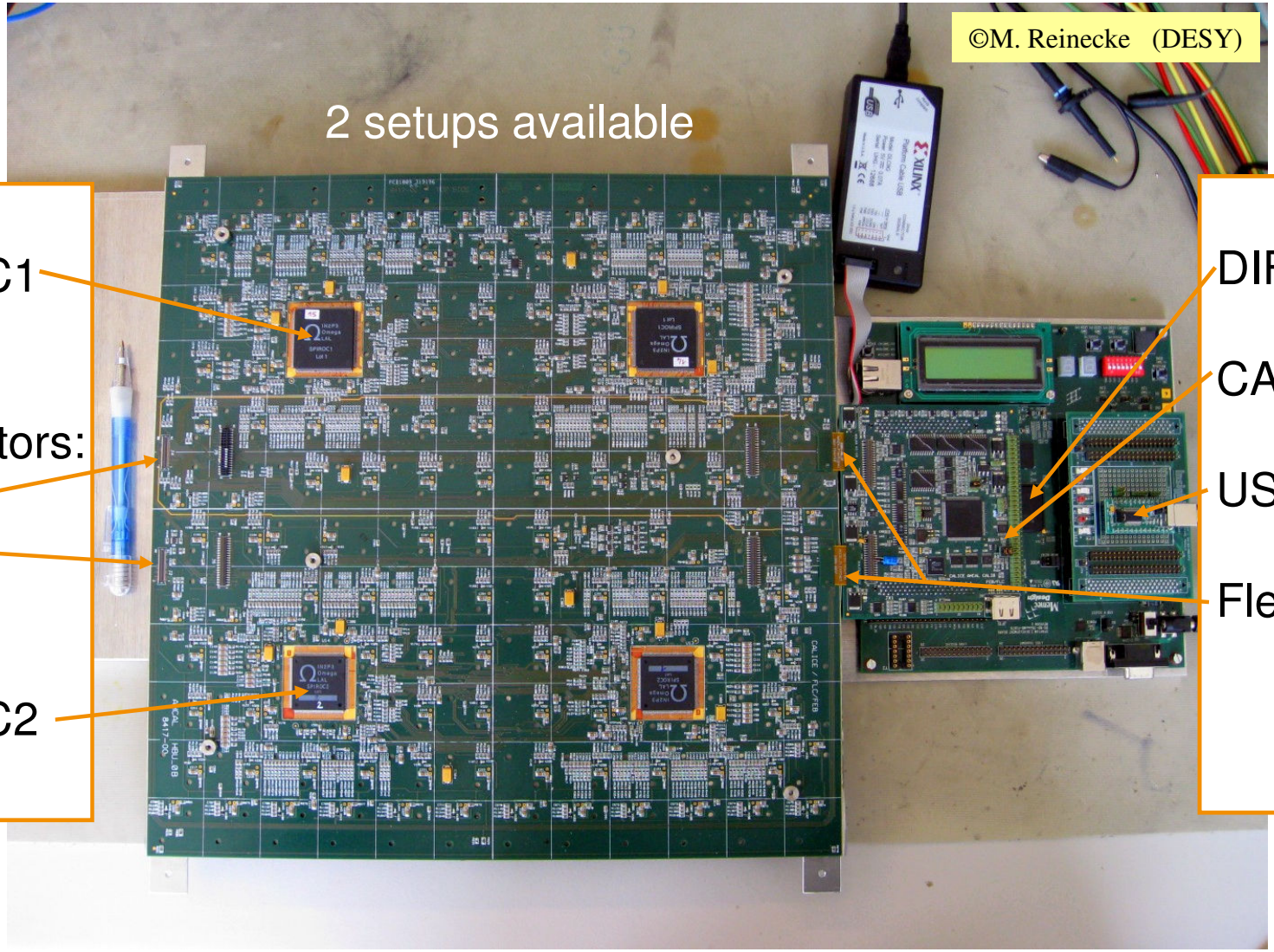






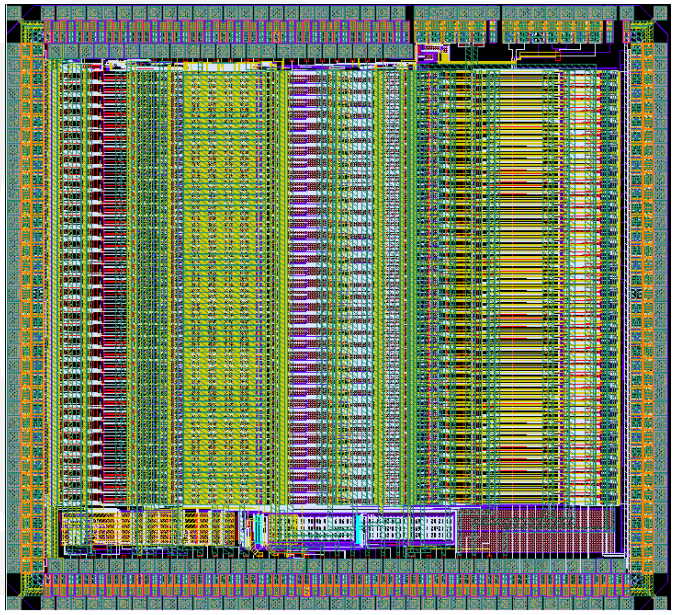


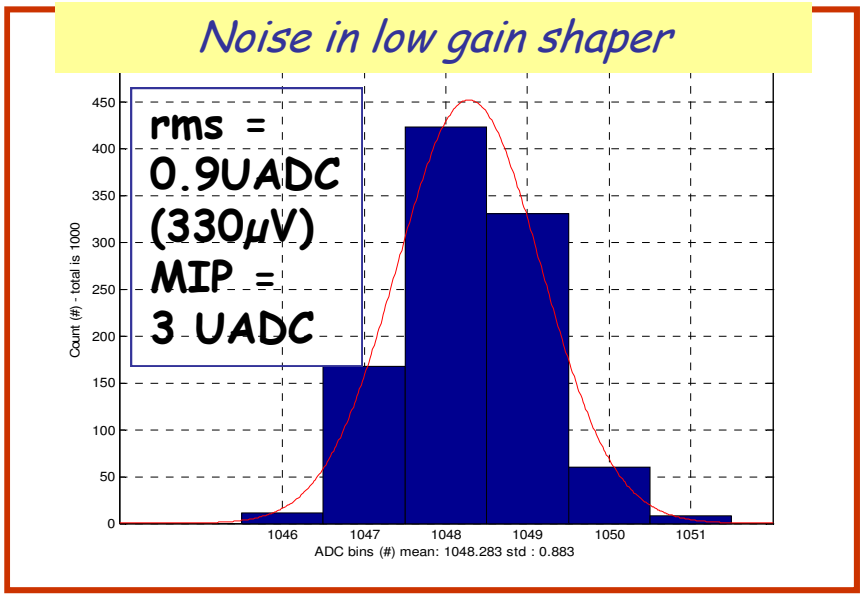
HBU0 status


©M. Reinecke (DESY)
2 setups available
SPIROC1
Connectors:
Signal
Power
SPIROC2
DIF FPGA
CALIB
USB / DAQ
Flexleads

SKIROC for W-Si ECAL

- Silicon Kalorimeter Integrated Read Out Chip (SKIROC1, Nov 06)
  - 36 channels with 15 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility, but cannot be used on an ASU or FEV
  - Collaboration with LPC Clermont





SKIROC status

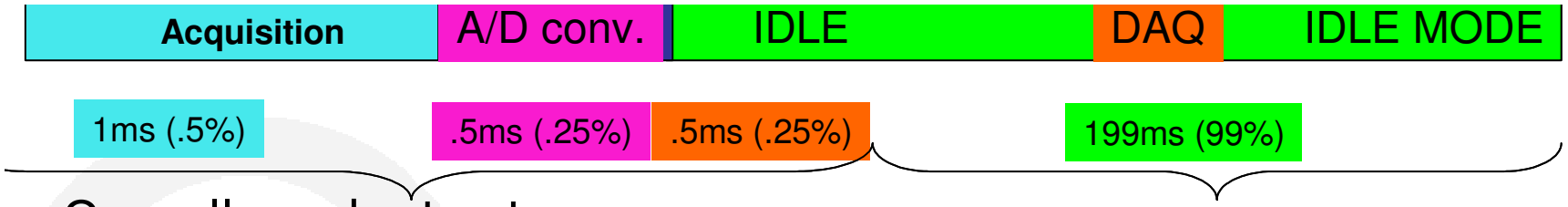
- SKIROC1 useless with detector (no readout)
- SPIROC2 used as SKIROC emulator
  - 95% identical to SKIROC (only preamp differs)
  - 36 channels instead of 64
  - Limited dynamic range (~500 MIPs)
  - Tests starting with FEV7 to address embedding issues
  - Noise tests on testboard proceeding (ENC ~ 1 ke-)
- R&D will continue within CALICE
  - SKIROC2 to be submitted with production run
    - **64 channels**
    - **Very large dynamic range**: HG for 0.5 to 500 MIP, LG for 500 to 3000 Mip
  - Simulations are on going
  - Expensive ASIC (**70 mm2** = 70 k€) => MPW not worth it

ECAL board: FEV7 with SPIROC2

- Version 1: June 2009, with packaged chips (TQFP 208) for the U structure (3mm available for the electronics)
- Version 2: September 2009, with COB
- SPIROC2 used in SKIROC mode

Test beam with technological prototype

- Data rate (Spiroc/Skiroc) : naive estimate
  - Volume : 36ch*16sca*50bits=30 kbit/chip
  - Conversion time : 16*100 µs = 1.6 ms
  - Readout speed 5 MHz (could be increased to 10-20 MHz)
  - 8 chips/DIF line (one FEV only)
  - Total : 1.5ms + 30000*200ns*8 = 50 ms/16 events = 3 ms/evt => 300 Hz during spill



- Overall readout rate
  - « Add » 1-10% power pulsing : 3-30 Hz effective rate
  - Pessimistic as assuming all chips full
  - **interesting tests to be done**

- Note : readout electronics designed for ILC low-occupancy, low rate detector **≠Testbeam** !!

Summary

- 2nd prototypes of HARDROC (DHCAL) and SPIROC (AHCAL+ECAL) submitted in june 08
- DAQ part being validated with HaRDROC
- Power pulsing tests essential now at system level
- Front-end boards first prototypes coming in
- DAQ interface (DIF boards) prototyped

- Tests are very complex and essential
- Still need to validate noise, autotrigger, ADC, power pulsing with detector.

- A nice infrastructure for performing essential I detector tests

Backup slides

Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power