SPIROC Asic: Overview of the Characterisation Measurements

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Measurements presented here done in collaboration with *B. Lutz [DESY]* and *W. Shen [Heidelberg]*

NOTE: In investigating the SPIROC response to signal from SiPMs, devices from MEPhy/Pulsar were used [1x1 mm^2, 1156 pxls, gain: 0.25 - 1.00 $\cdot$ 10^6]

$\Rightarrow$ **same devices used in AHCAL test-beam operations**

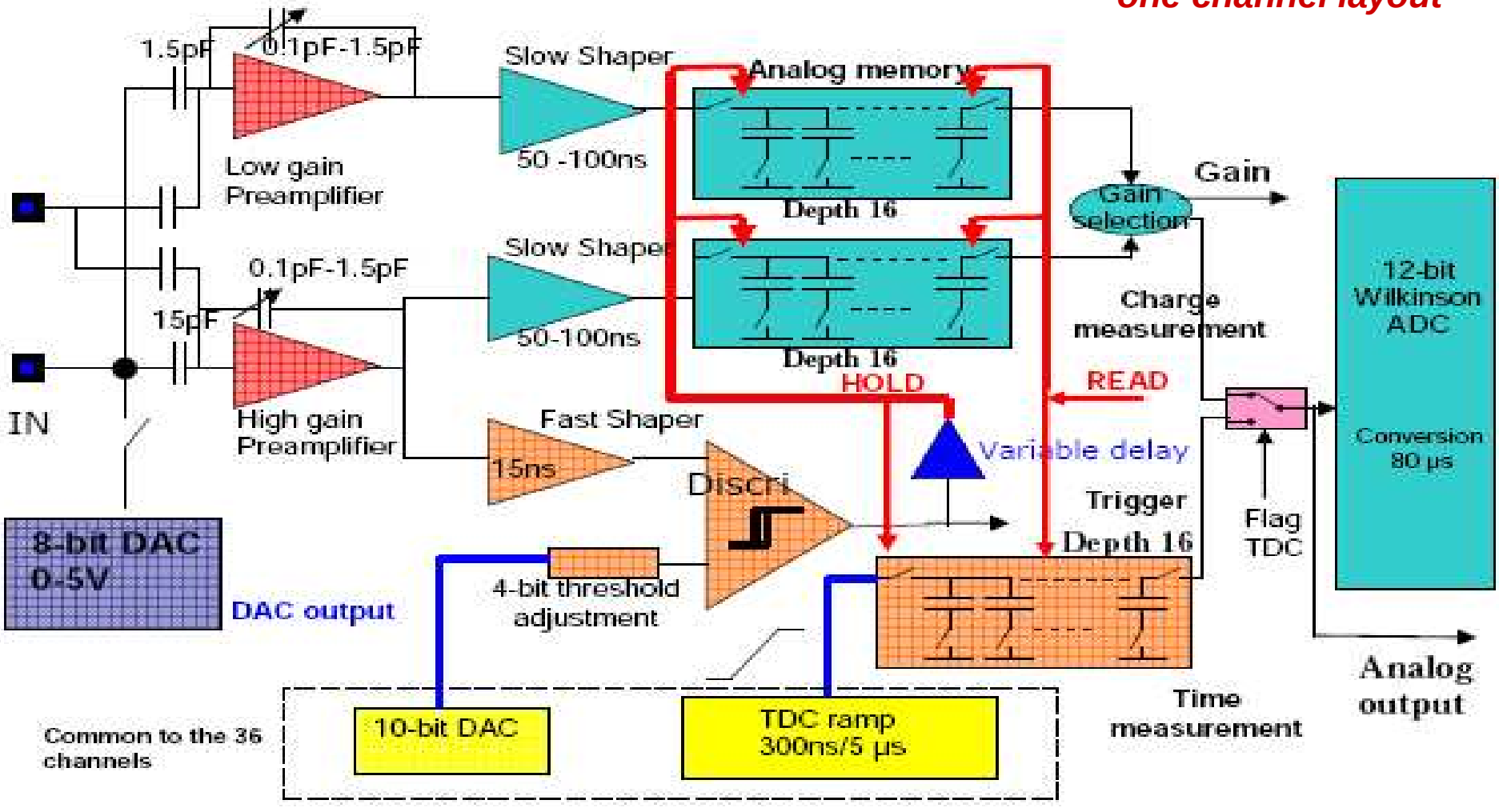
SPIROC ASIC Description and Properties

- **Dedicated front-end electronics for ILC analogue HCAL (AHCAL)**
- **Replacement of ILC-SiPM ASIC currently used in AHCAL prototype**
- **It embeds cutting edge features to fullfil ILC final requirements:**
  - **— low noise**
  - **— low power dissipation (should sit inside the detector)**
  - **— large number of readout (SiPM) channels: 36**
  - **— auto-trigger (according to preselected threshold levels)**
  - **— input signals internally processed (pre-amplification, shaping, ADC)**
  - **— large dynamic range (should allow calibration & cover SiPM range)**
- **Developed by LAL/OMEGA Paris**
- **Commisioning performed (and on-going) mainly at DESY**
- **Measurements presented here concern SPIROC IB version (no digital part)**

SPIROC ASIC Description and Properties

Analogue part:

one channel layout



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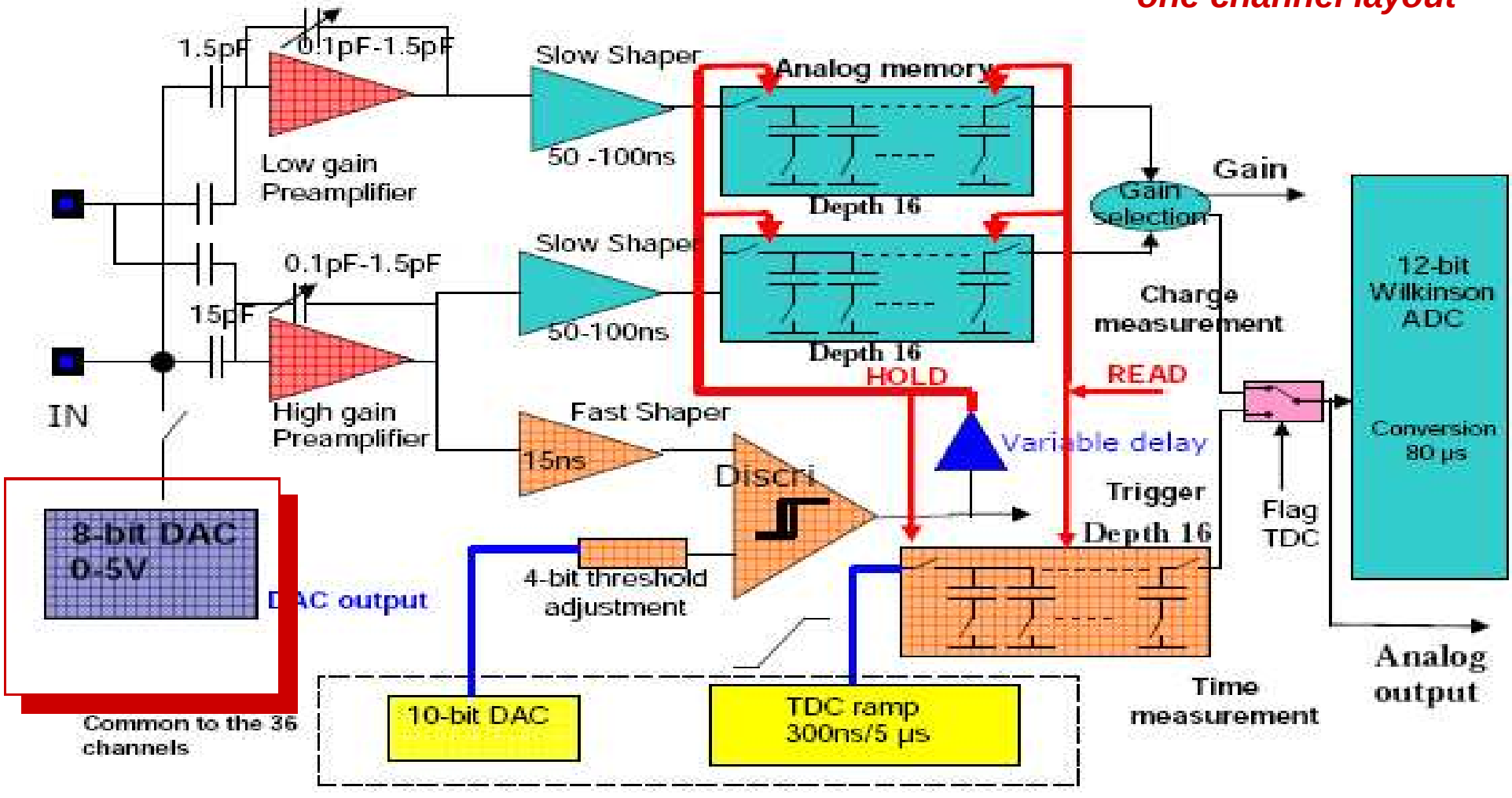
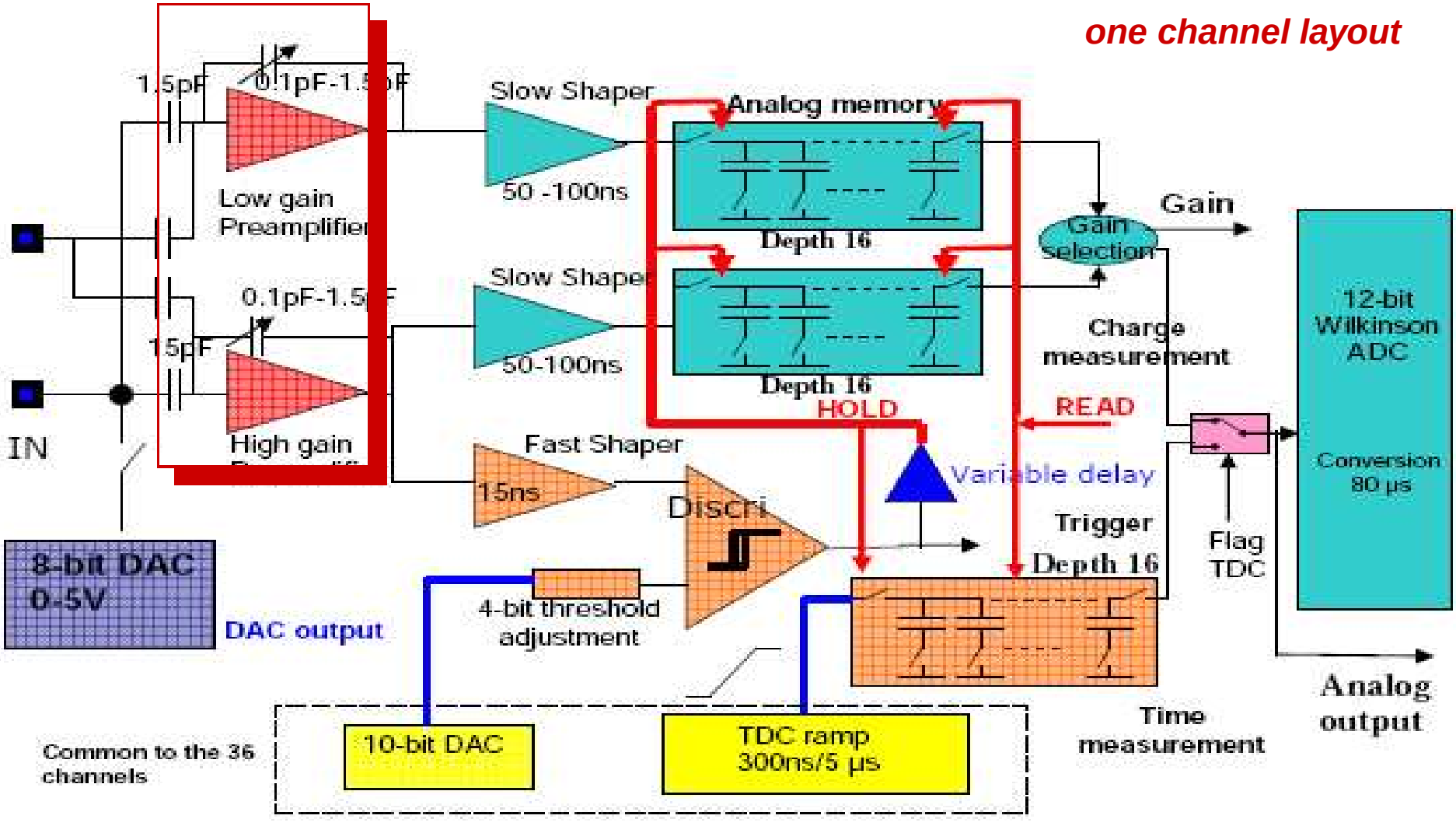


Adjustable bias voltage for each SiPM

SPIROC ASIC Description and Properties

Analogue part:

one channel layout



Separate channels for adjustable pre-amplification in low/high gain mode of input signal

SPIROC ASIC Description and Properties

Analogue part:

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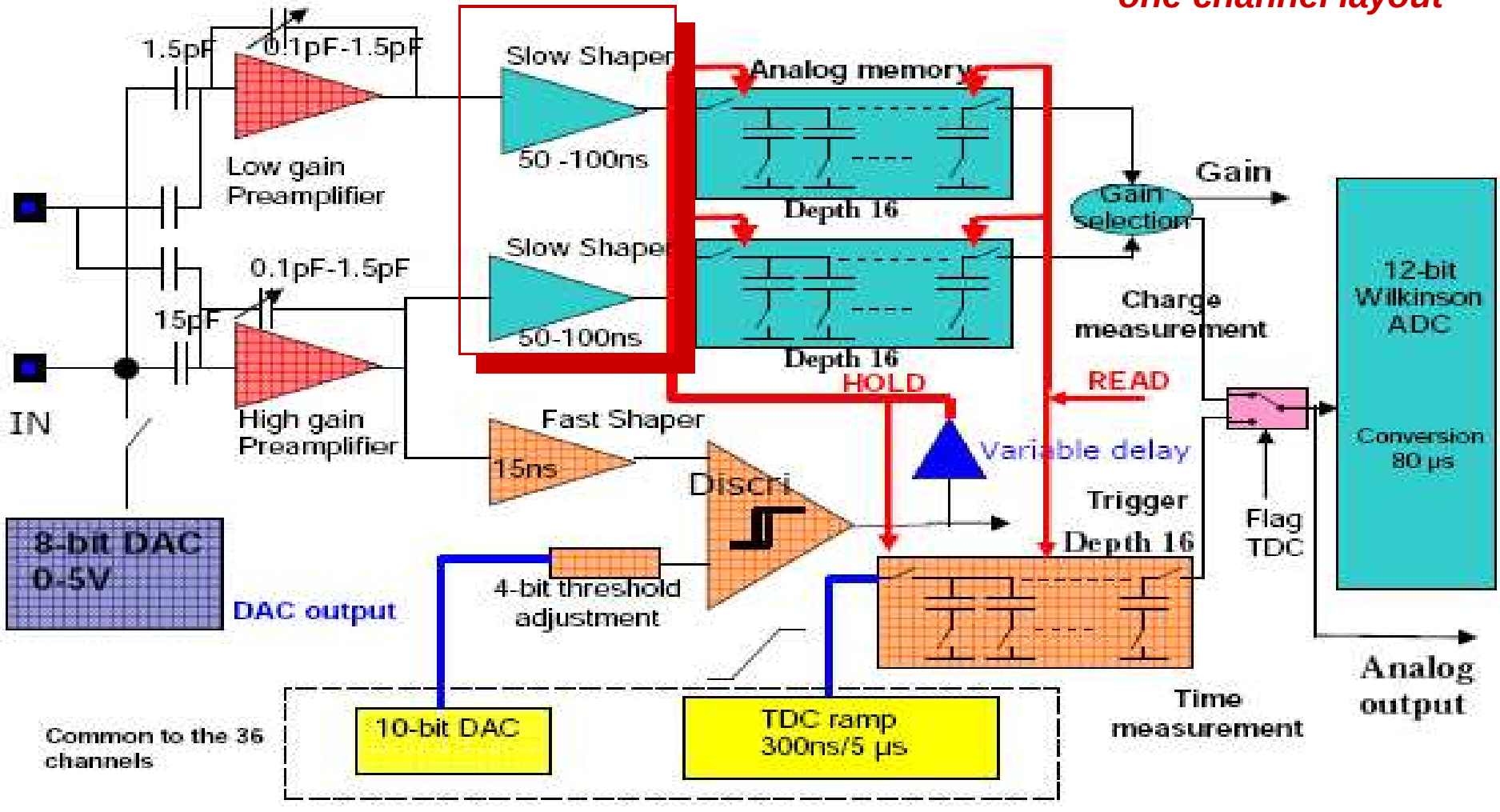

adjustable shaping time

SPIROC ASIC Description and Properties

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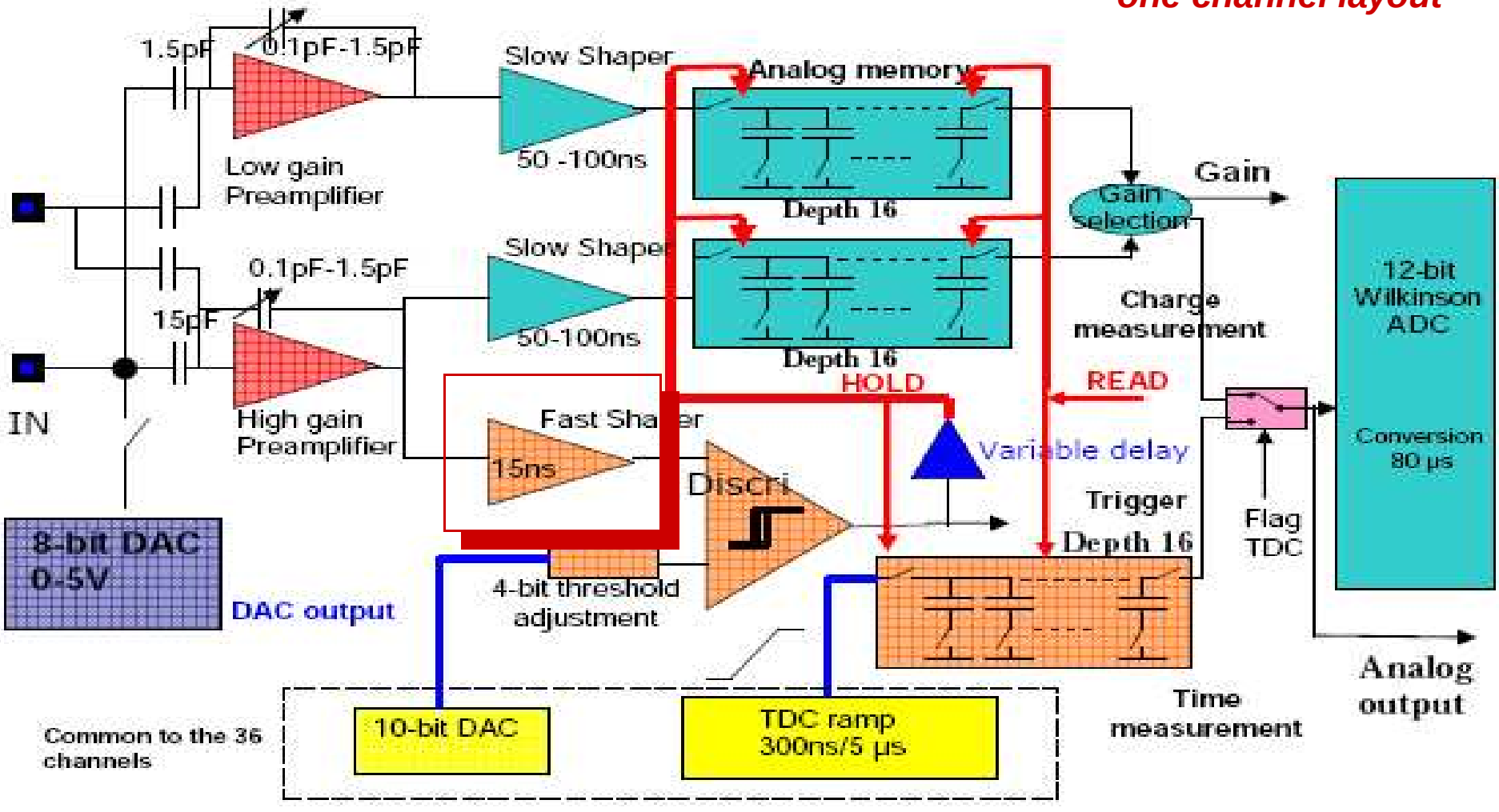

fast shaper for ...

SPIROC ASIC Description and Properties

Analogue part:

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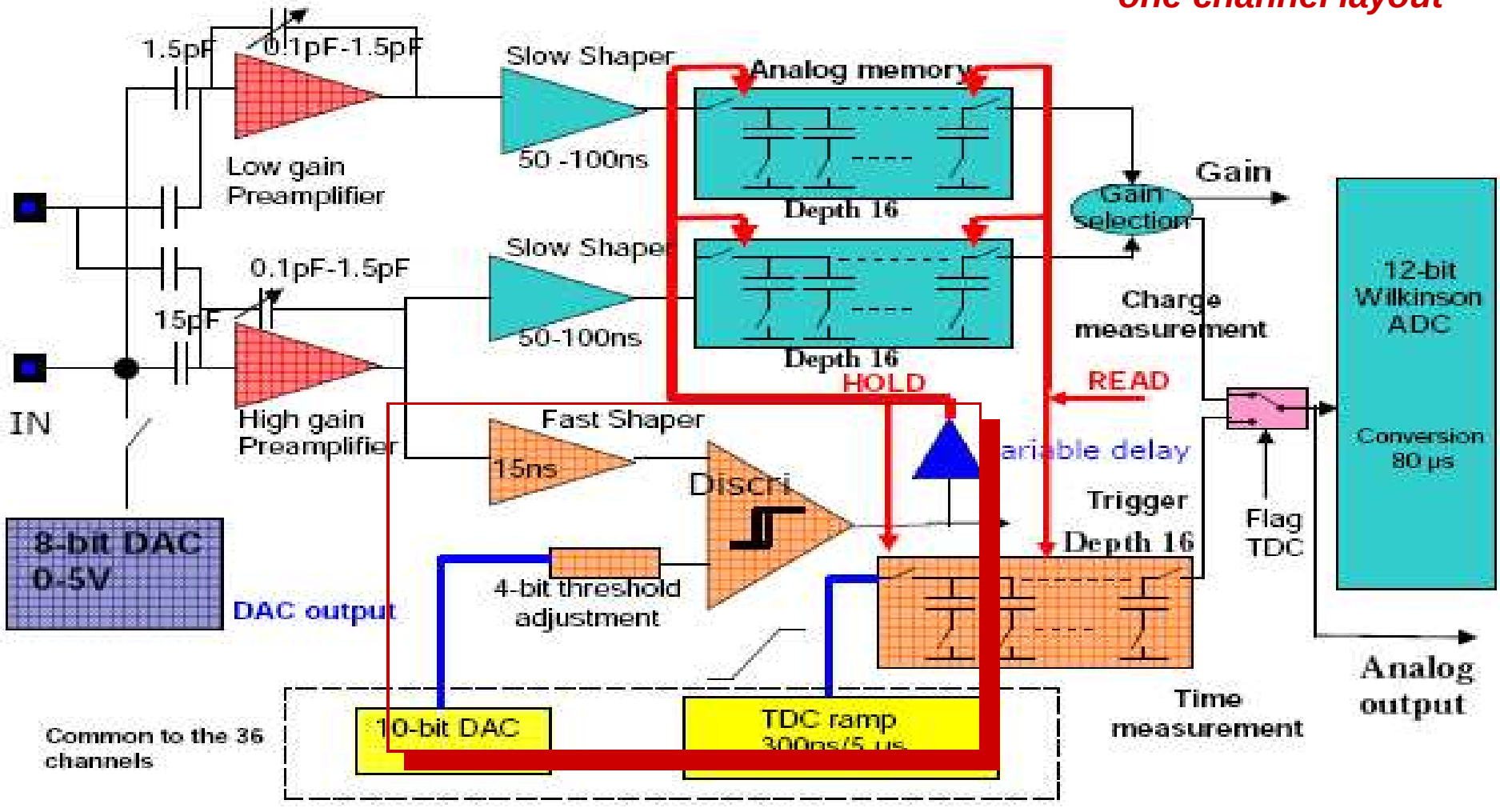
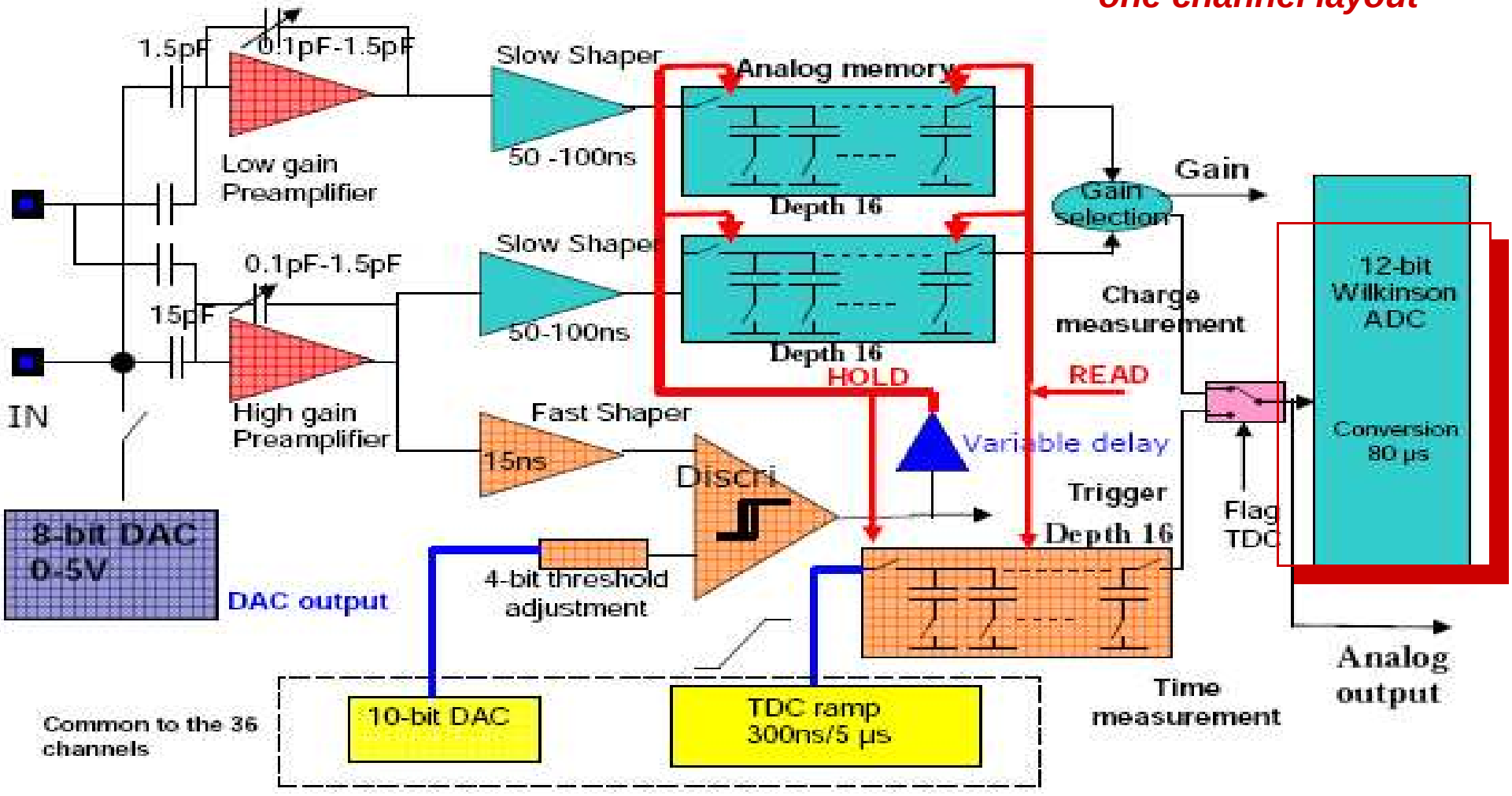


...autotrigger (to eventually hold the analogue shaped signal)

SPIROC ASIC Description and Properties

Analogue part:

one channel layout



Internal ADC to locally digitise signal amplitude

SPIROC ASIC Description and Properties

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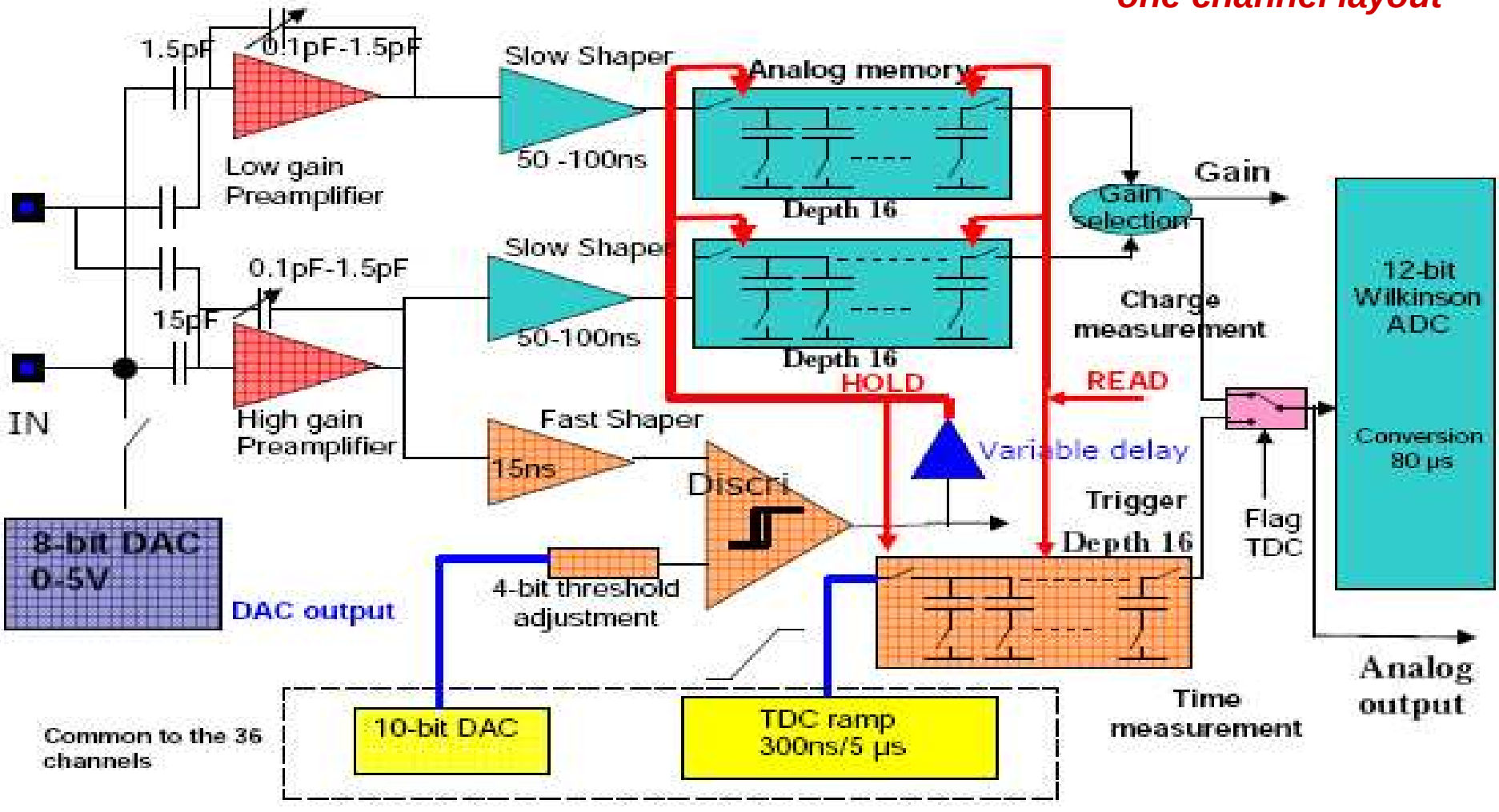
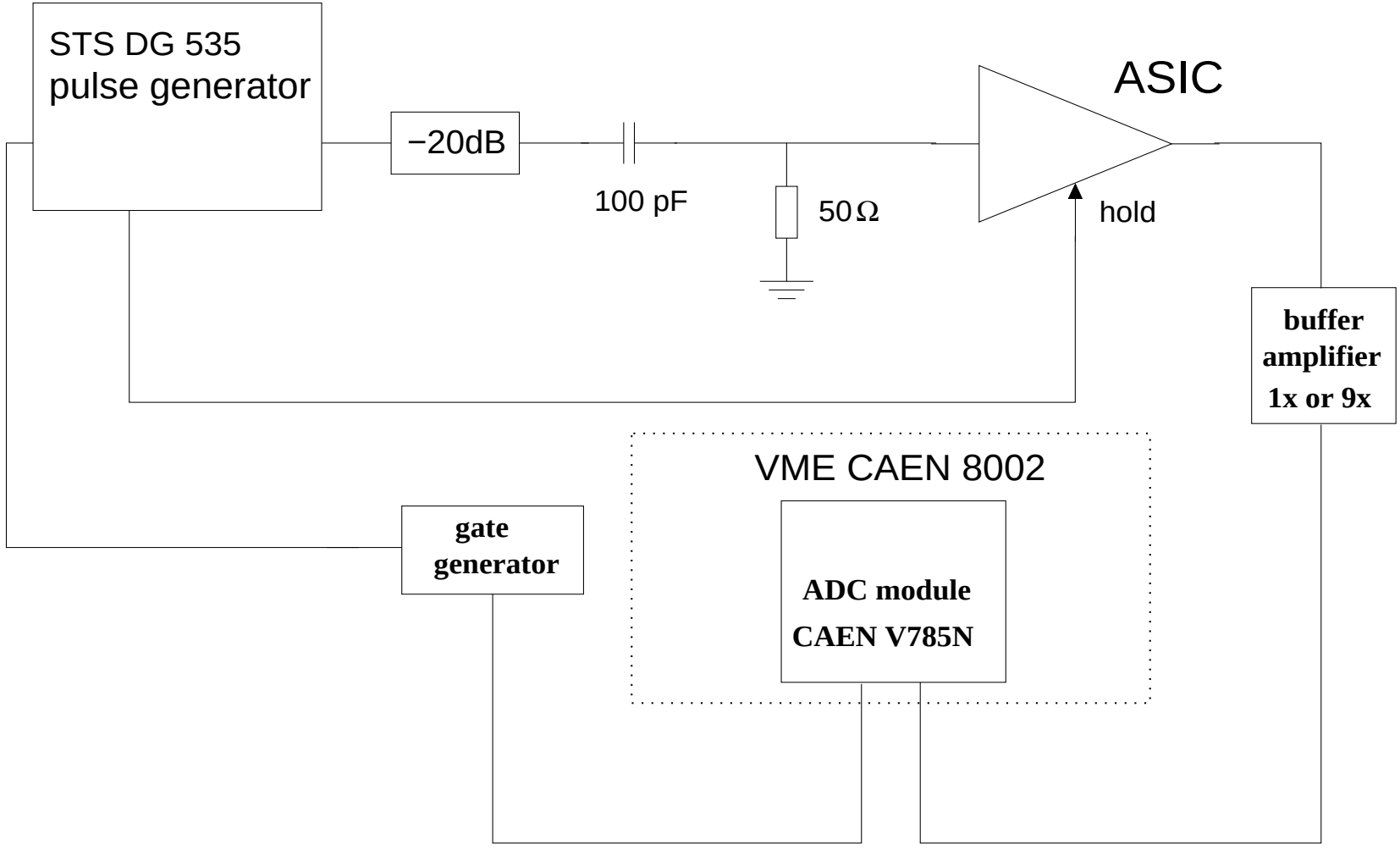
one channel layout



plus digital stage (not shown here) to synchronise acquisition/readout with ILC timing

Test-Bench Description

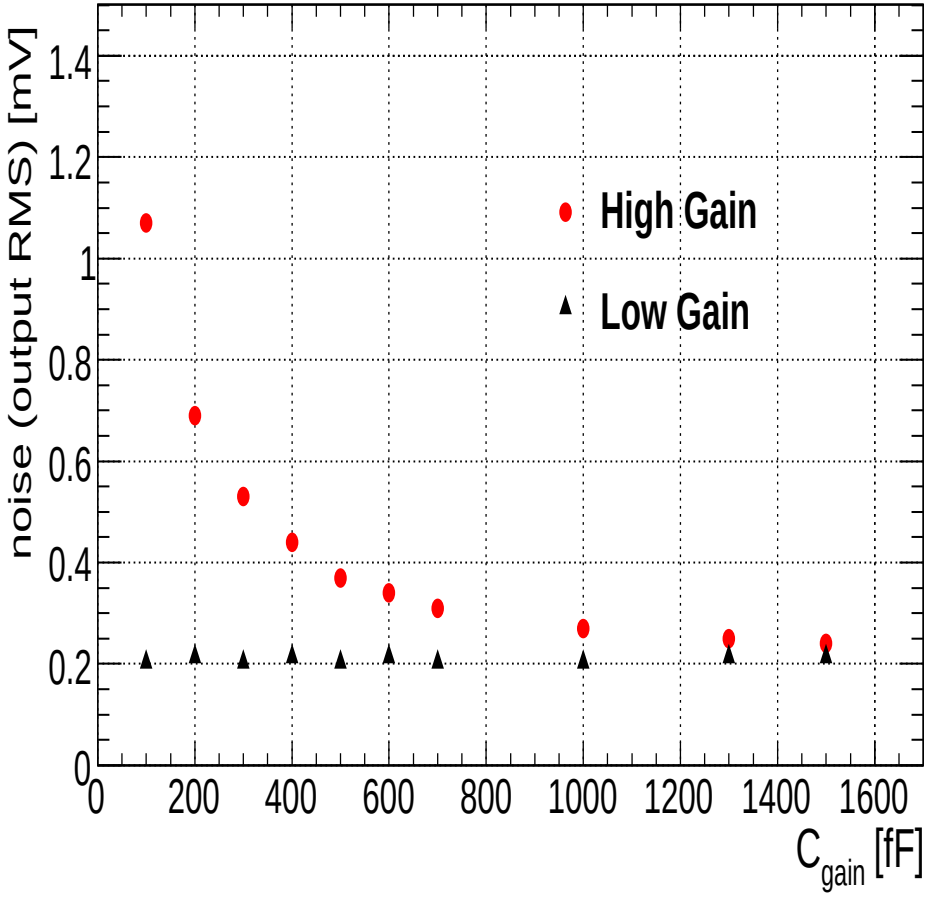


Noise Investigation

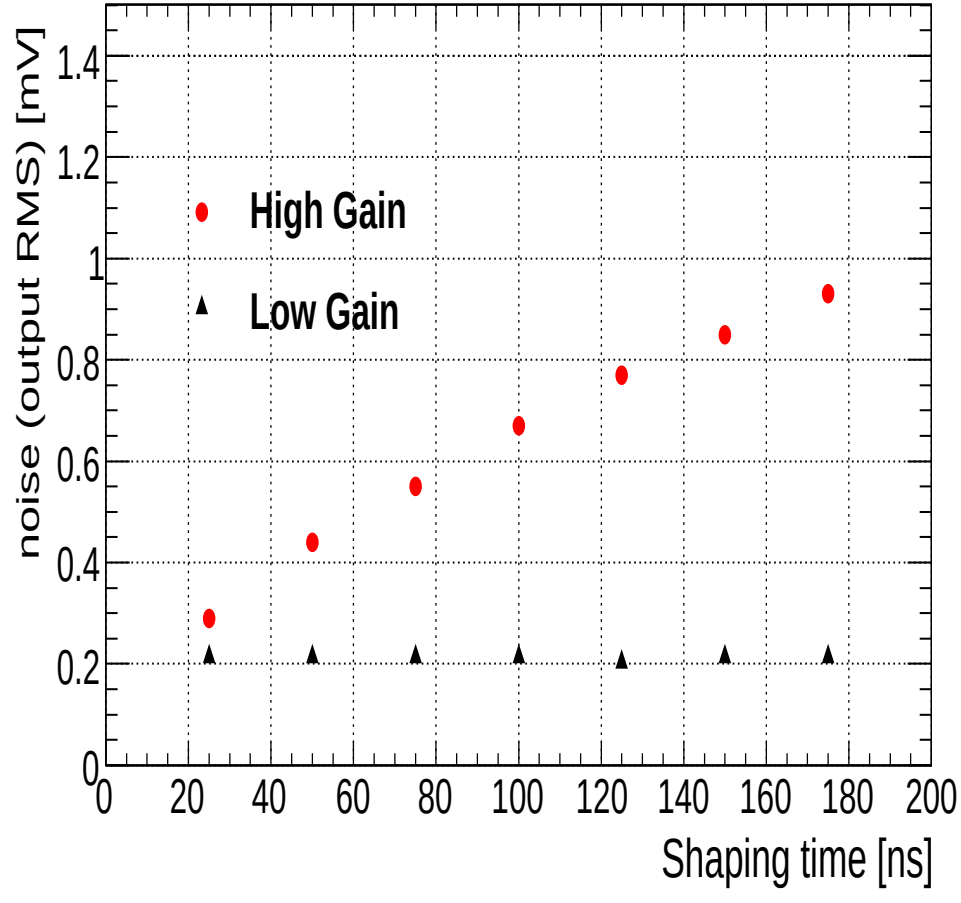
Electrical Noise Investigation

- **Noise affecting processed signal was measured at different working conditions of the chip (no input line connected)**

  $\Longrightarrow$ **uniformity between 36 channels found within fraction of millivolt**



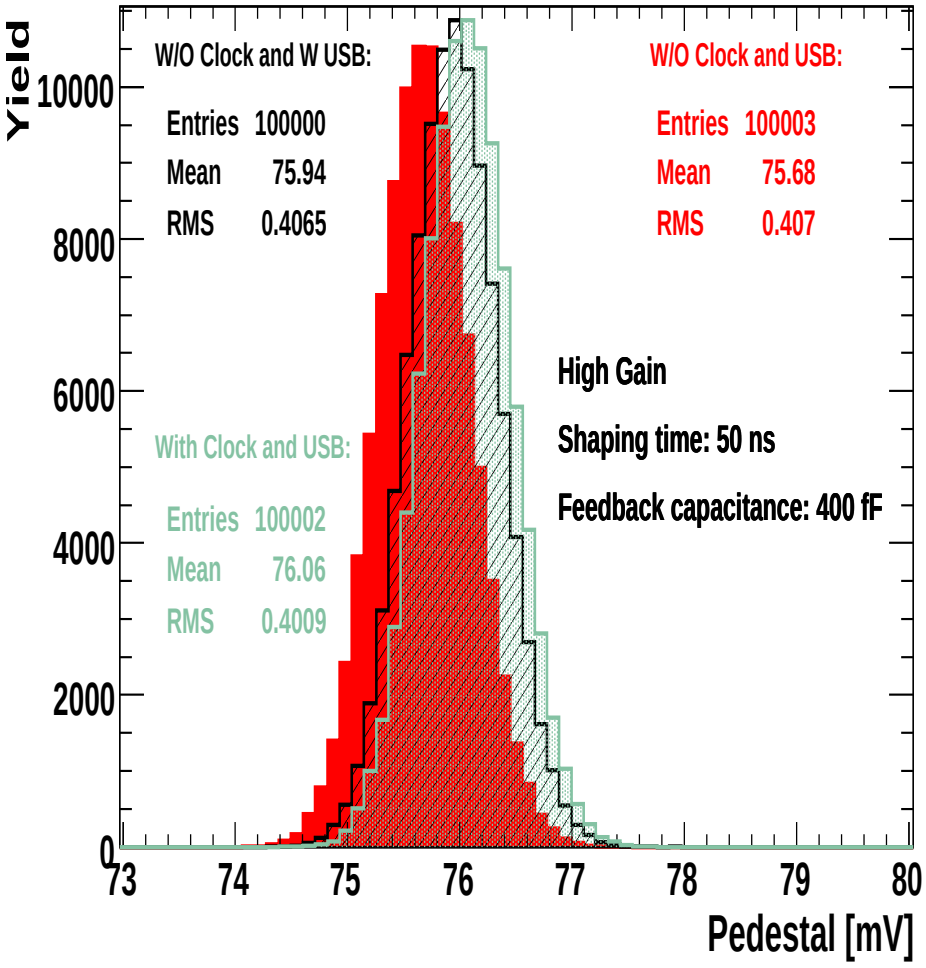
$\Uparrow$ **for 50 ns shaping time** $\Uparrow$

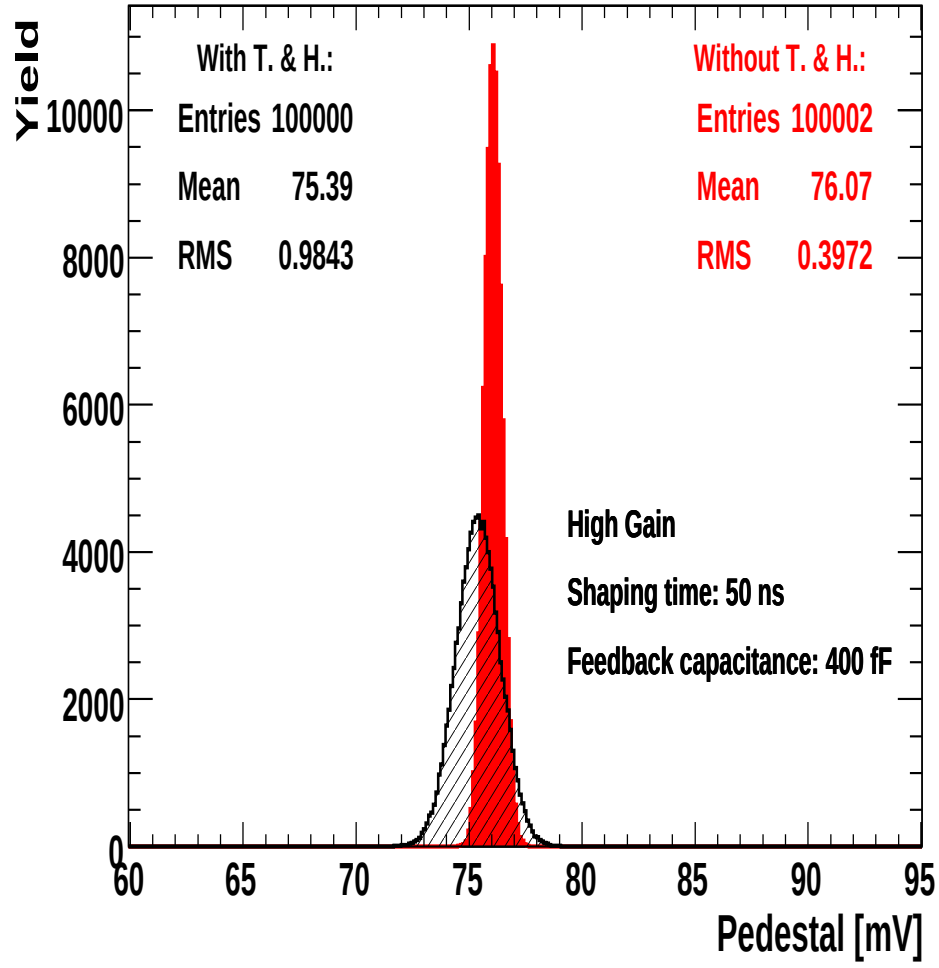


$\Uparrow$ **for 400 fF variable capacitance** $\Uparrow$

Additional Sources to Noise

- **Additional source can affect signal (no input line connected)**





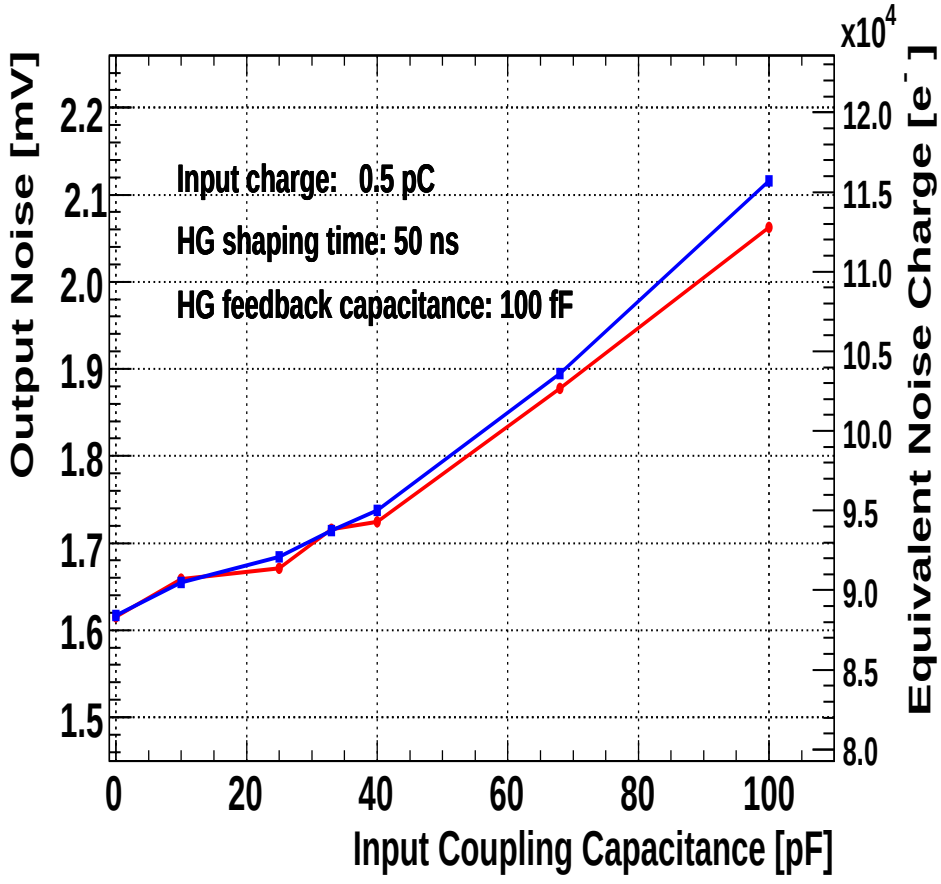
Negligible effect from swithing on clock and plugging in USB

Sizable effect from Track and Hold switch

ENC and Input Detector Capacitance

- **Connecting a SiPM expected to increase noise depending on coupling capacitance (CC**

  $\Rightarrow$ **important to quantify noise sensitivity to external variable capacitance (SiPM)**



According to measurements:

S/N achievable by the chip ranges

between 4.7 and 3.6

20% effects in the 0-100 pF range

Trigger Studies

Auto-Trigger Mode Operation Principles

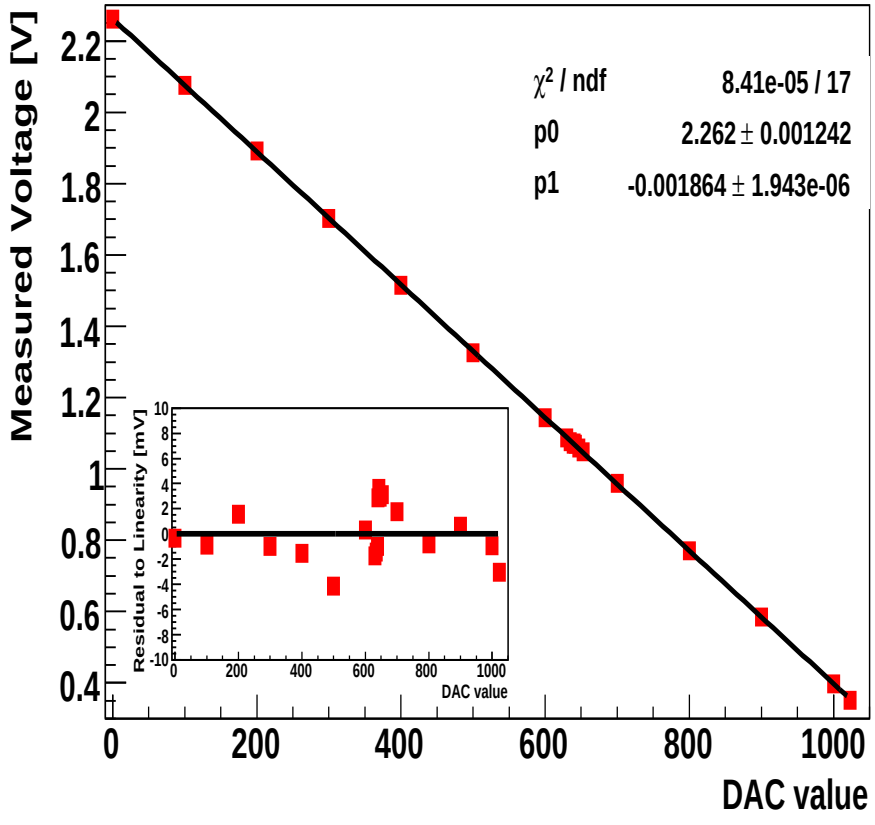
- **Chip designed to operate in 'auto-trigger' mode**
- **Signal from 15 ns fast shaping line enters an adjustable discriminator**
  - **— 10 bits DAC common to all channels**
  - **— Threshold for each channel individually adjustable by 4 bits DAC**
- **If signal overshoots threshold, trigger is generated to hold signal at its peaking amplitude and store in analogue memory**
- **Important to investigate trigger efficiency and homogeneity for 36 channels**
- **Uncertainty on trigger timing should be studied**

Common Threshold Level (10 bits DAC)

Calibration:

— Change DAC via LabView GUI

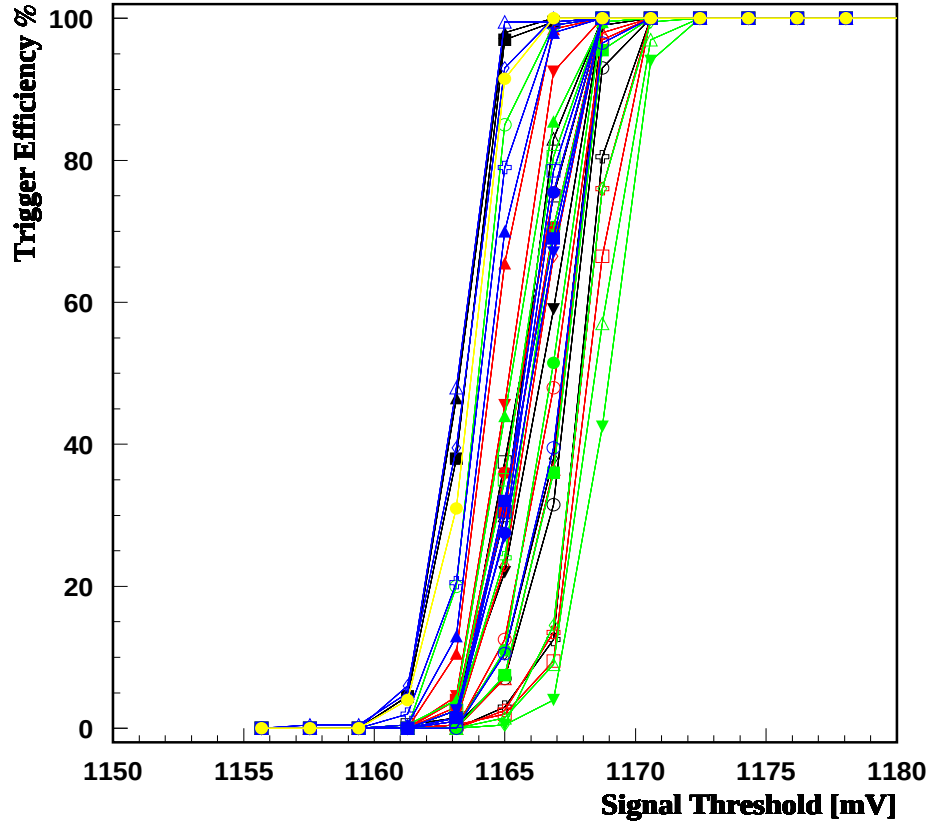
— Measure voltage on board with voltmeter



Trigger Efficiency (for pedestal):

— Increase DAC via LabView GUI:

— Count generated triggers

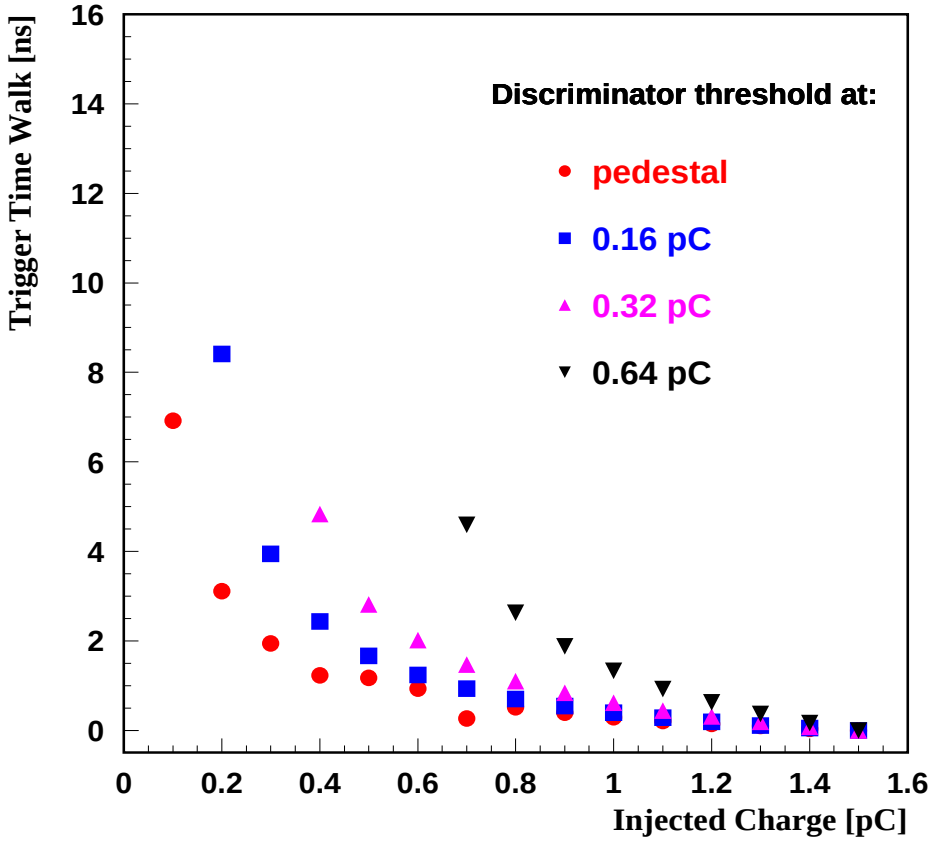


⇑ measured noise: ≈ 2-3 mV ⇑

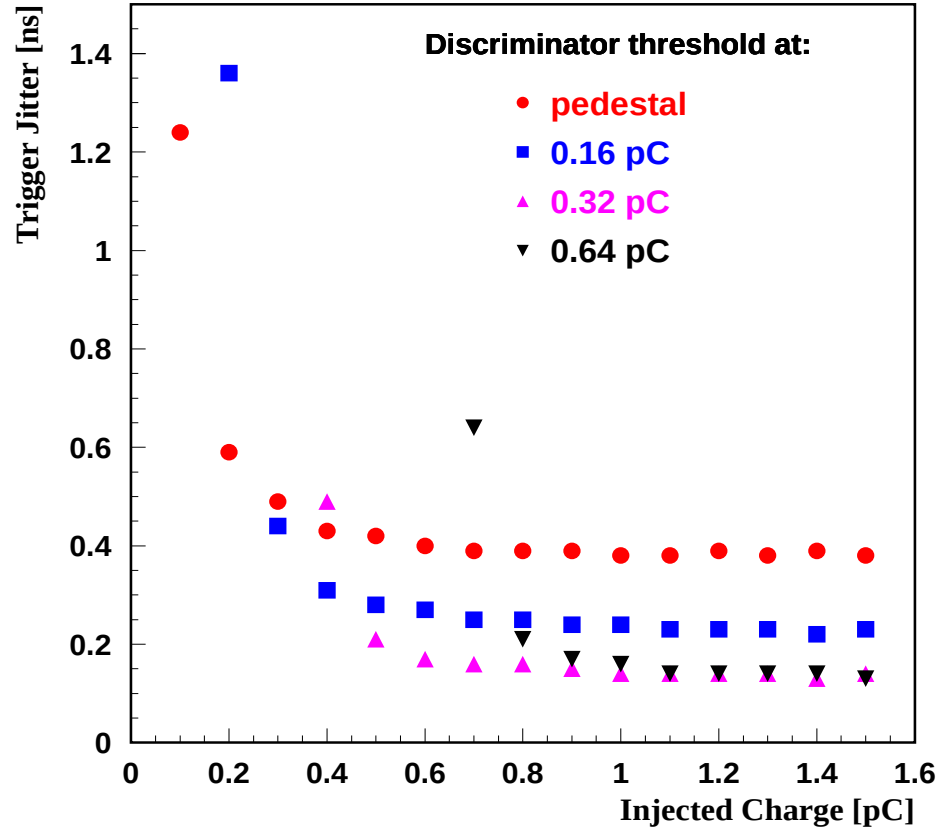
channel to channel spread: 8 mV

Trigger Time Walk and Jitter

Time Walk:



Jitter:



Time walk typically large only when close to threshold

$\Rightarrow$ **Potential auto-trigger operation for calibrations (it was not forseen!)**

$\Rightarrow$ **No problems for physics mode (threshold at $1/2$ mip)**

Dynamic Range, Linearity, and Gain of the ASIC

Track and Hold Switch

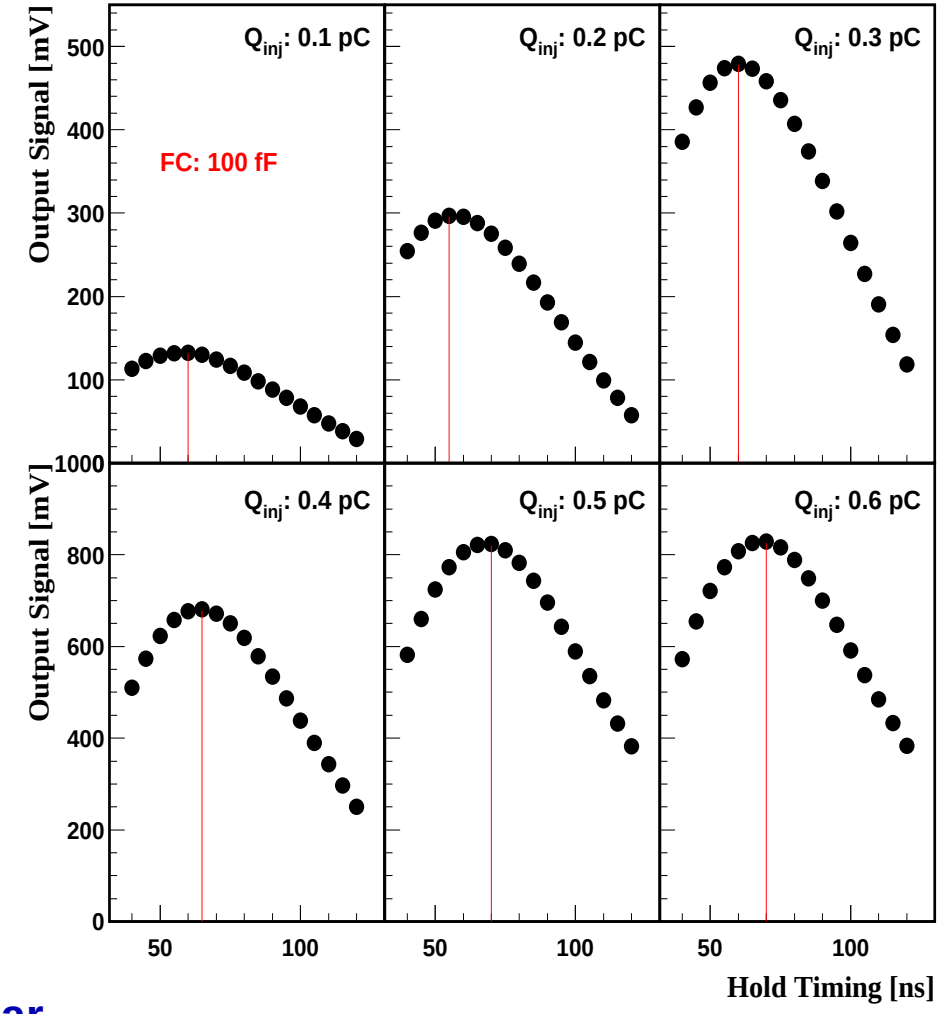
- Processed signal forseen to be held at peaking amplitude by track and hold switch

- Peaking amplitude reconstructed using T&H found to be:
  - — charge dependent
  - — larger than w/o using T&H

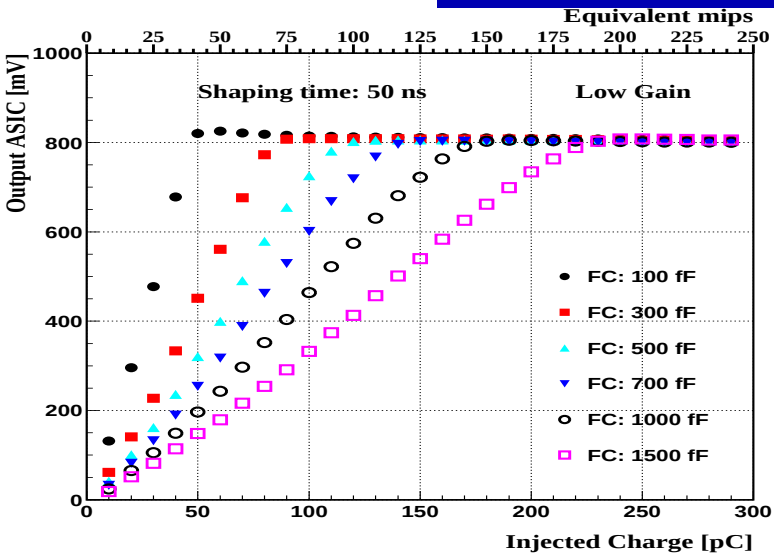
- Using T&H switch is necessary for extensive systematical measurements

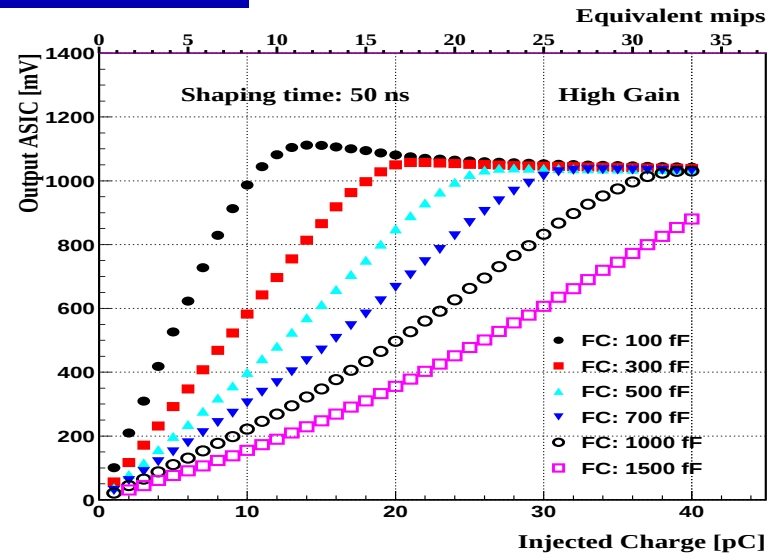
- T&H switch forseen in ILC data taking
  - ⇒ used for presented measurements
  - ⇒ possible effects on measurements

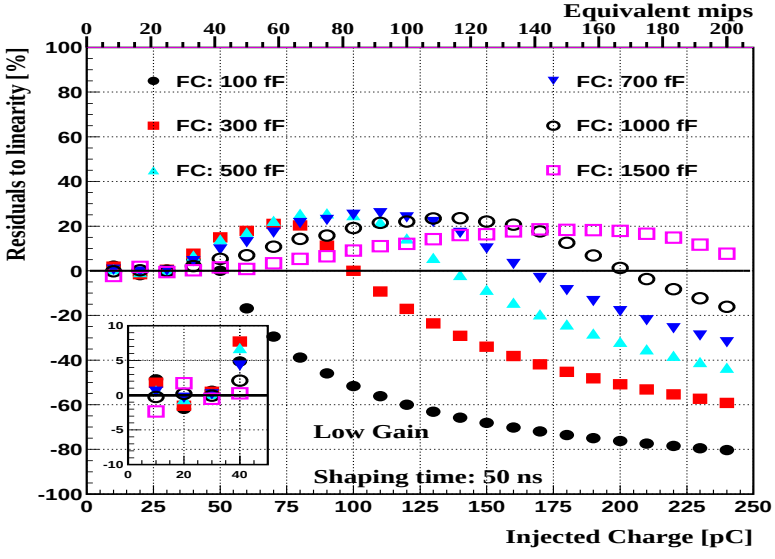
- W/O T&H peaking amplitude appears linear

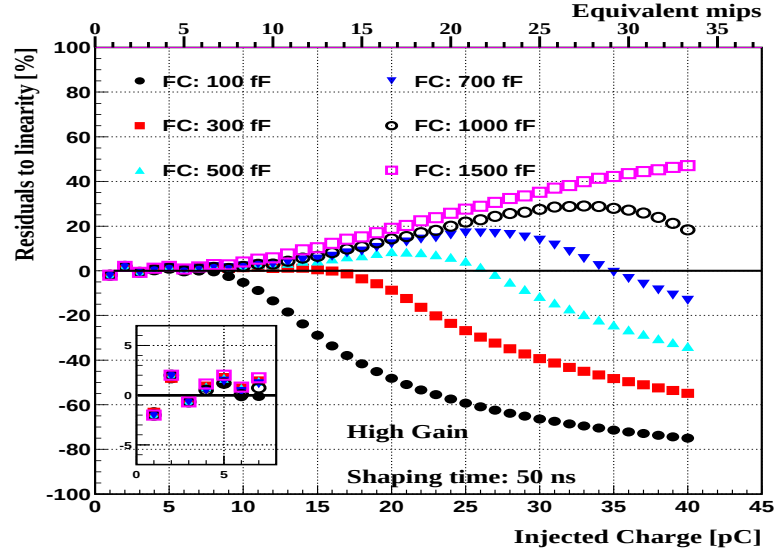


Linearity Measurements









1 pxl
=
$5 \cdot 10^5$ **e**
$\approx$
0.08 pC

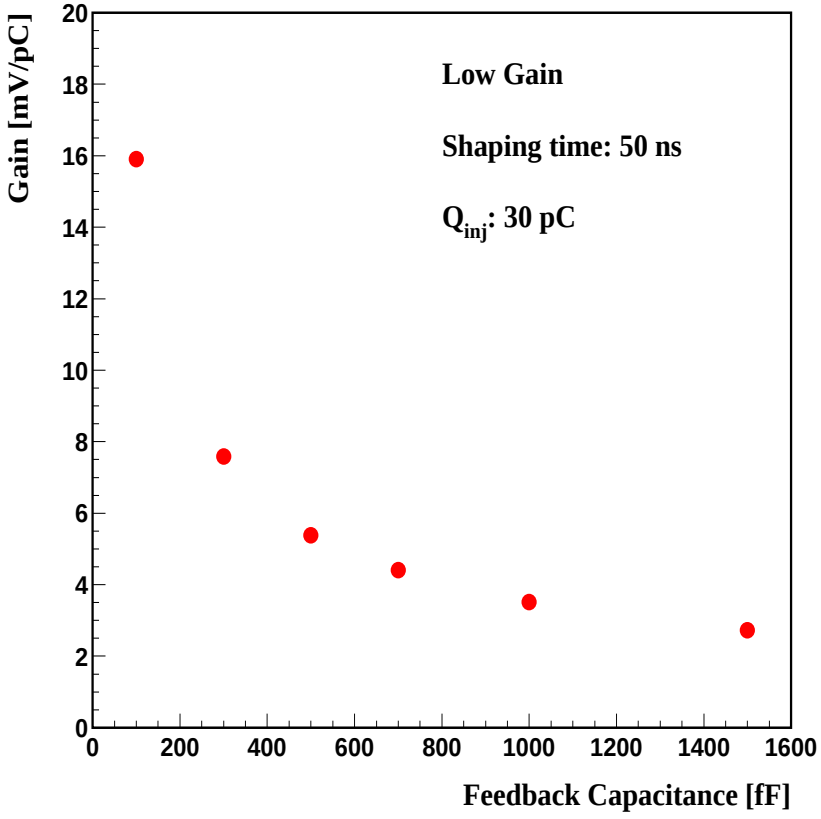
- **SiPM dynamic range up to ≈ 77 mips (1156 pxl / 15 pxl per mip) ≈ 92 pC**

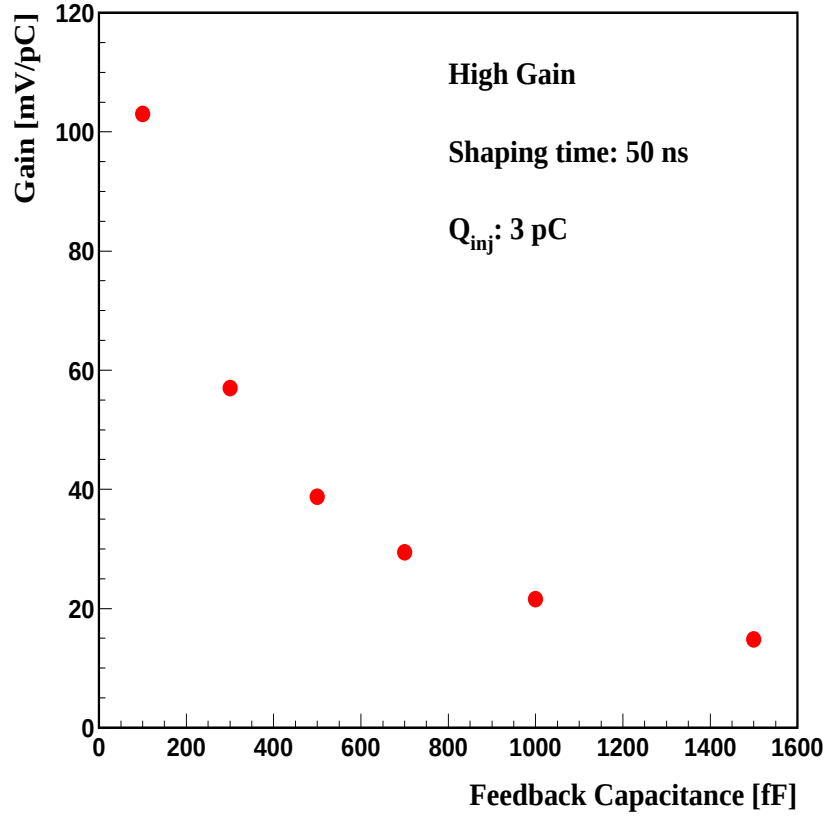
  $\Rightarrow$ **covered for FC ≥ 400 fF (physics mode) [calibration OK for > 100 fF] at $5 \cdot 10^5$ gain**

  $\Rightarrow$ **strong non-linearity due to T&H switch (possibly understood by Orsay group)**

Gain Measurements

- **Gain calculated as** $G_{ASIC} = \frac{V_{output}}{Q_{input}} [\frac{mV}{pC}]$





$\Rightarrow$ **Expected behaviour** $1/C_{FC}$ **observed**

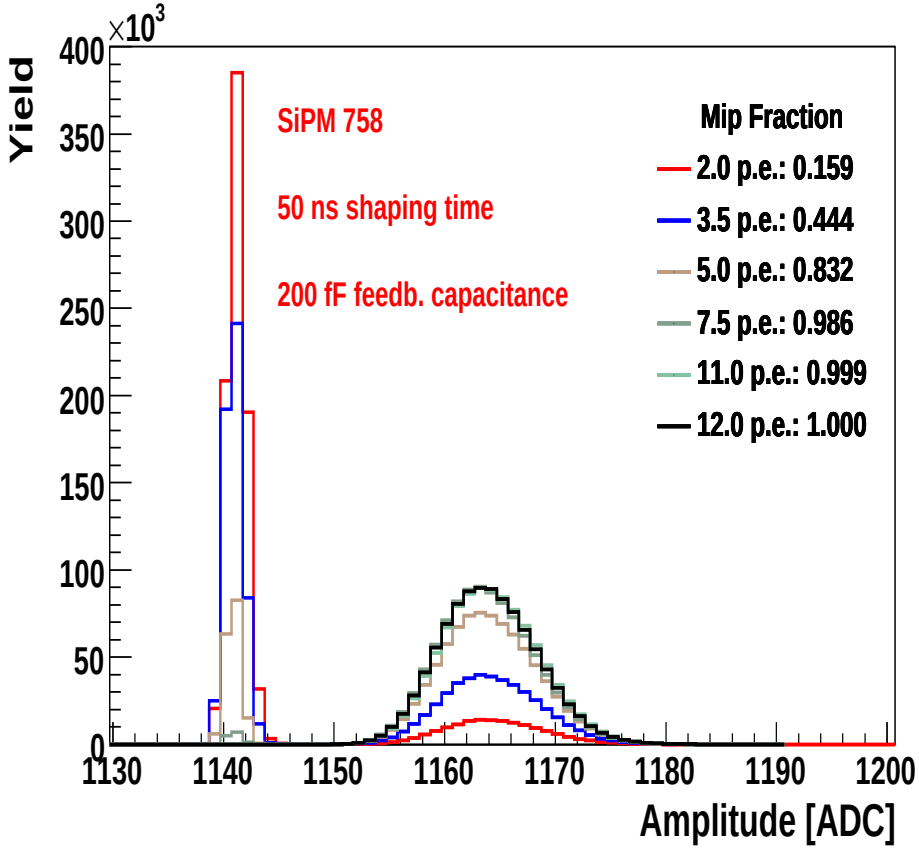
$\Rightarrow$ **Qualitative agreement with Orsay measurements**

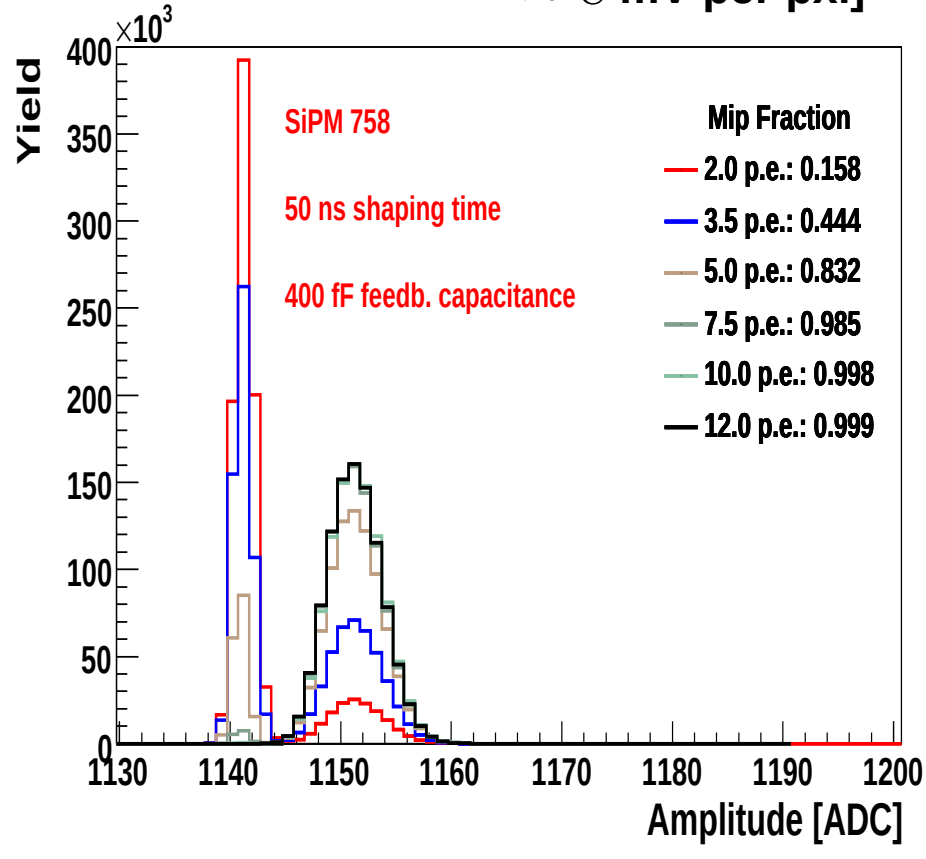
Simulating Real Data Taking Conditions

Data Taking in Physics Mode

- We want a proof of principle that chip can operate in auto-trigger mode (1/2 mip cut)
- Process signal from LED-flashed SiPM

$\Rightarrow$ LED amplitude tuned to generate one mip-like signal [maximum around 15 pxls; ≈ 8 mV per pxl]



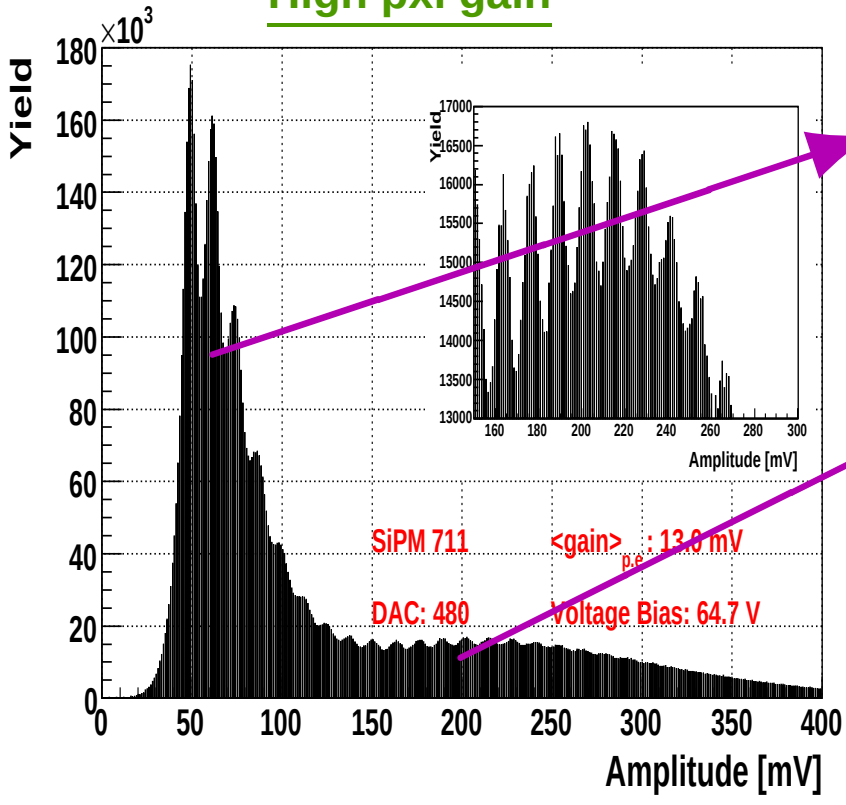


$\Rightarrow$ Almost 100% signal induced triggers at $1/2$ mip threshold cut (proof of principle)

Single-Pixel Spectra

- How are SiPM calibrations forseen? $\Longrightarrow$ Process signal from SiPM flashed by LED
- What about auto-trigger mode for thermal noise?

High pxl gain



thermal noise

LED-induced signal

Dominating thermal noise:

can be fitted

Single-Pixel Spectra

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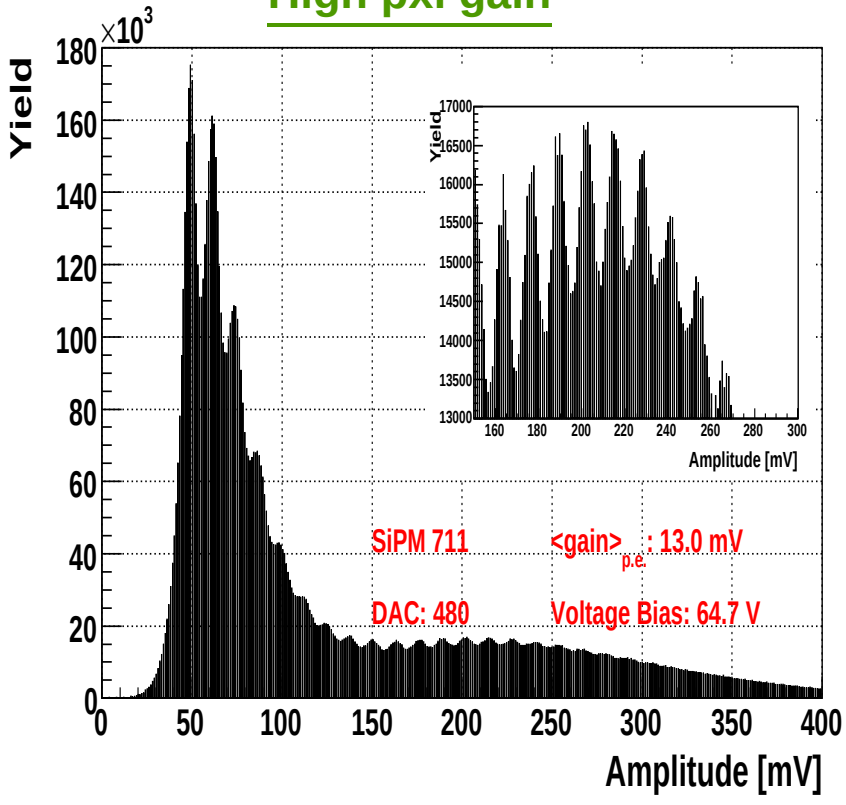
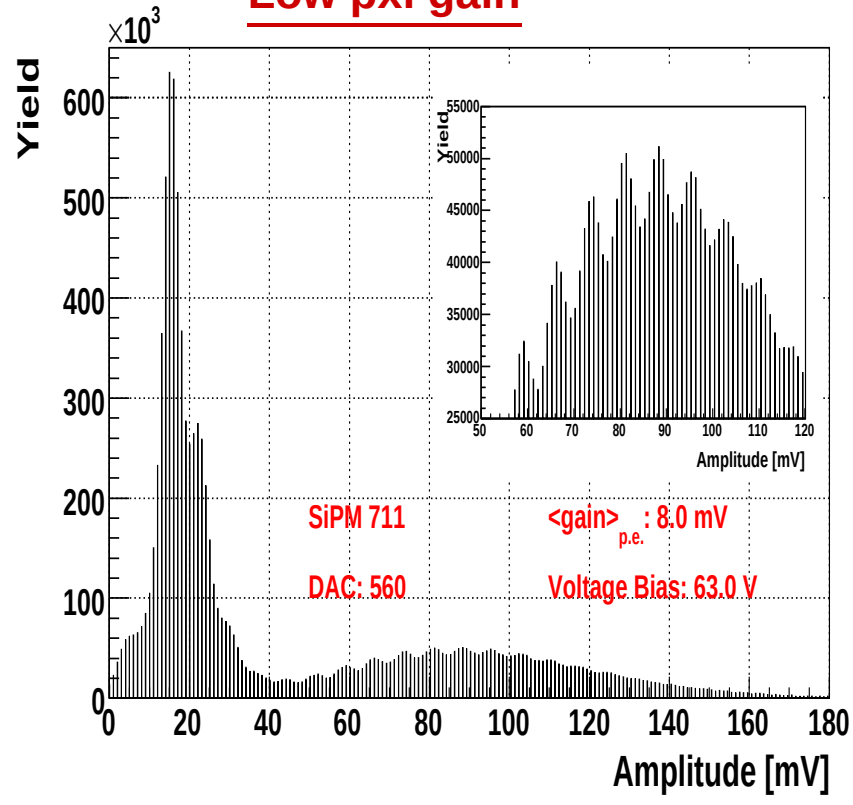
High pxl gain



Low pxl gain



Dominating thermal noise:

can be fitted $\longleftrightarrow$ **cannot be fitted**

Single-Pixel Spectra

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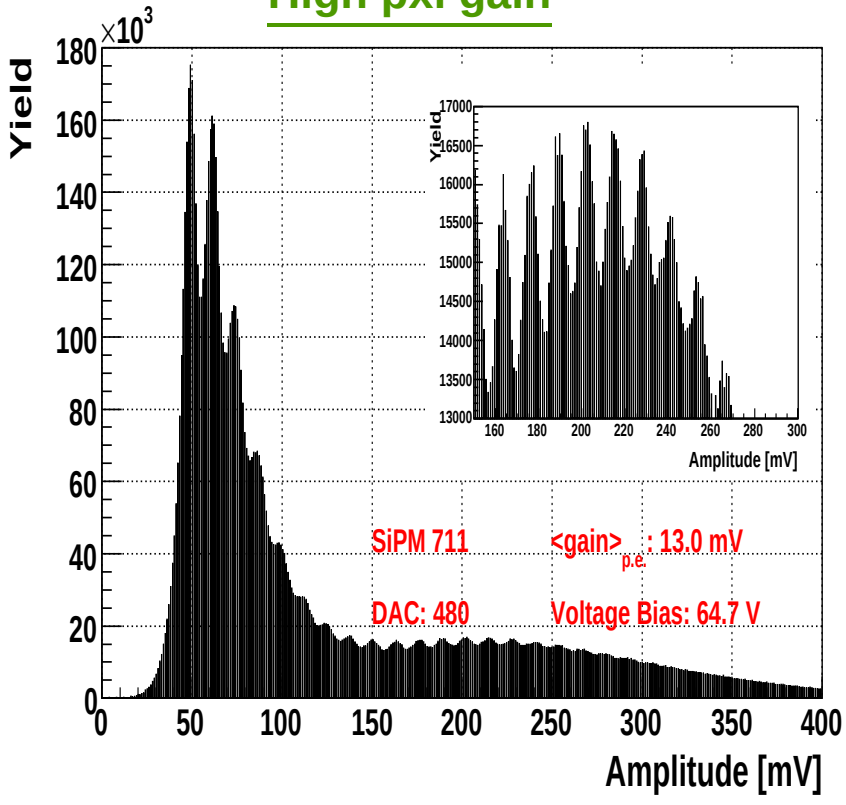
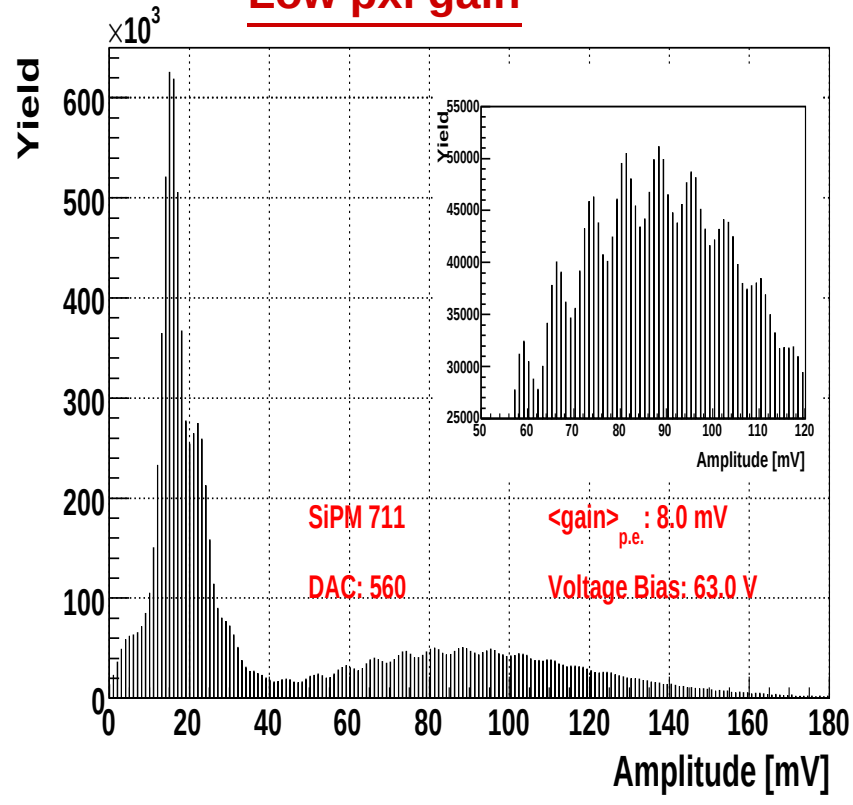
High pxl gain



Low pxl gain



Dominating thermal noise:

can be fitted $\longleftrightarrow$ **cannot be fitted**

$\Rightarrow$ **Potentiality to calibrate photodetector in auto-trigger: with SiPMs with large pxl gain!**

Summary and Outlook

- Analogue component of SPIROC ASIC extensively investigated
  - ☞ measurements presented for SPIROC IB chip version
- Dynamic range for physics/calibration modes possibly covered
  - ☞ depends on pixel gain of SiPM to be used
- ASIC can operate in auto-trigger mode
- Low noise measured
- Gain as expected
- Low cross-talk
- Potentiality to calibrate in auto-trigger
- Residuals to linearity of HV DAC adjustment sizable
  - ☞ reproducible; we can correct for it via calibration!
- Track and Hold switch strongly affects (linearity) the measurements
- As further steps:
  - ☞ proceed with SPIROC II
  - ☞ timing measurements
  - ☞ power pulsing

LC Internal Report ready

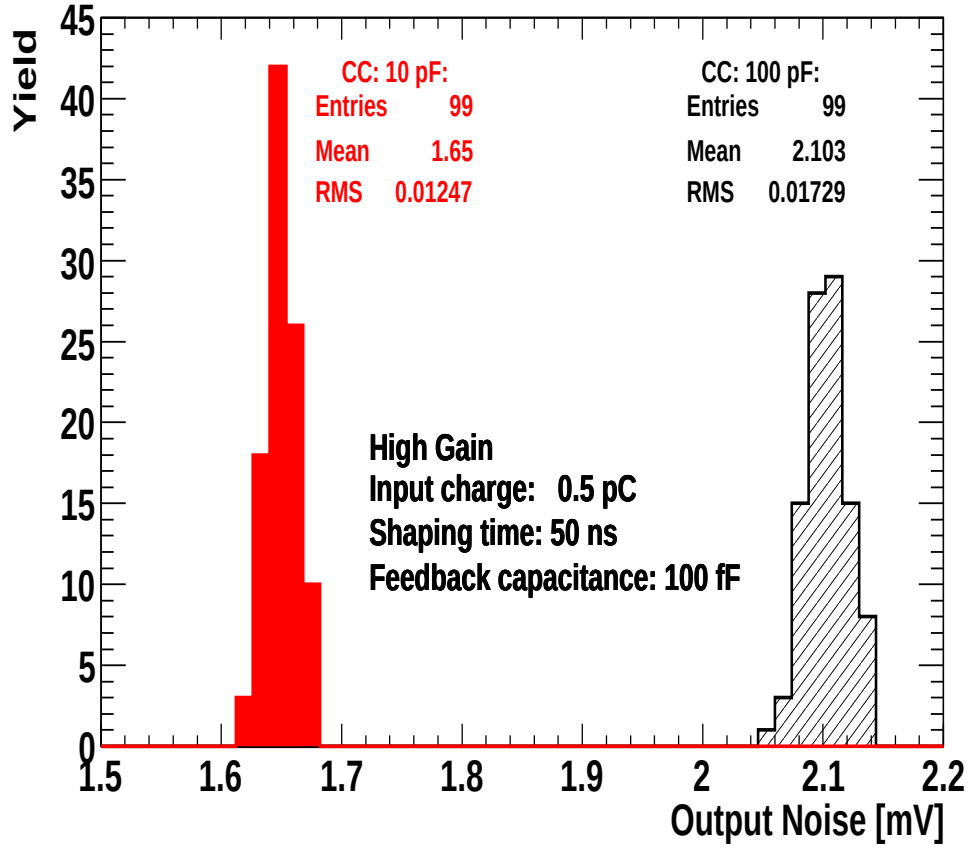
Backup Slides

ENC and Input Detector Capacitance

- **Connecting a SiPM expected to increase noise depending on coupling capacitance (CC**

  ⇒ **observed non-reproducibility**

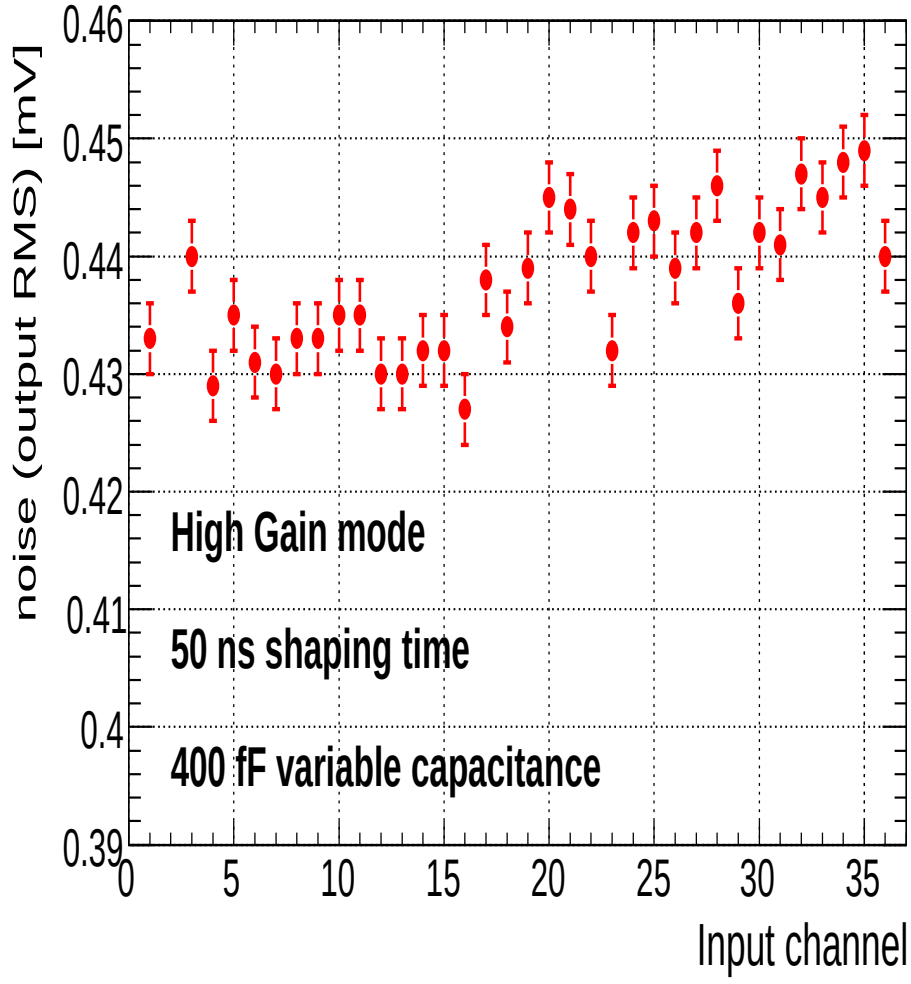
Reiterate measurements:



⇒ **non-reproducibility possibly due to experimental setup**

Noise Uniformity

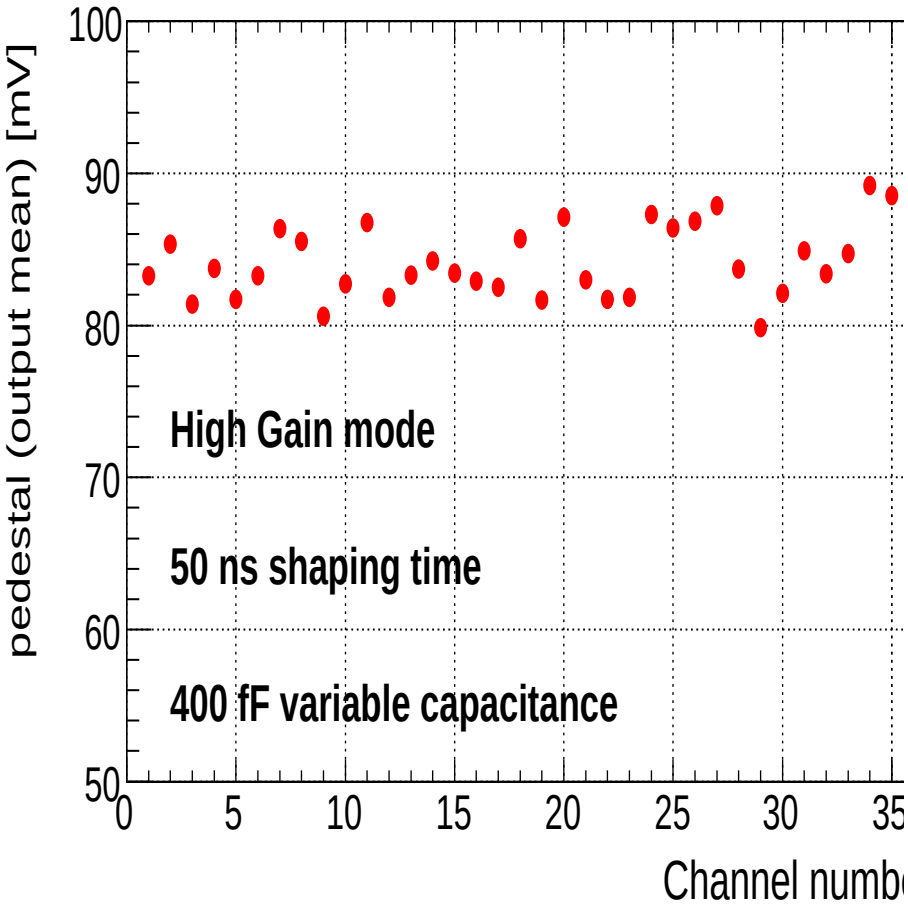
- **Noise measured for all 36 channels (no input line connected)**

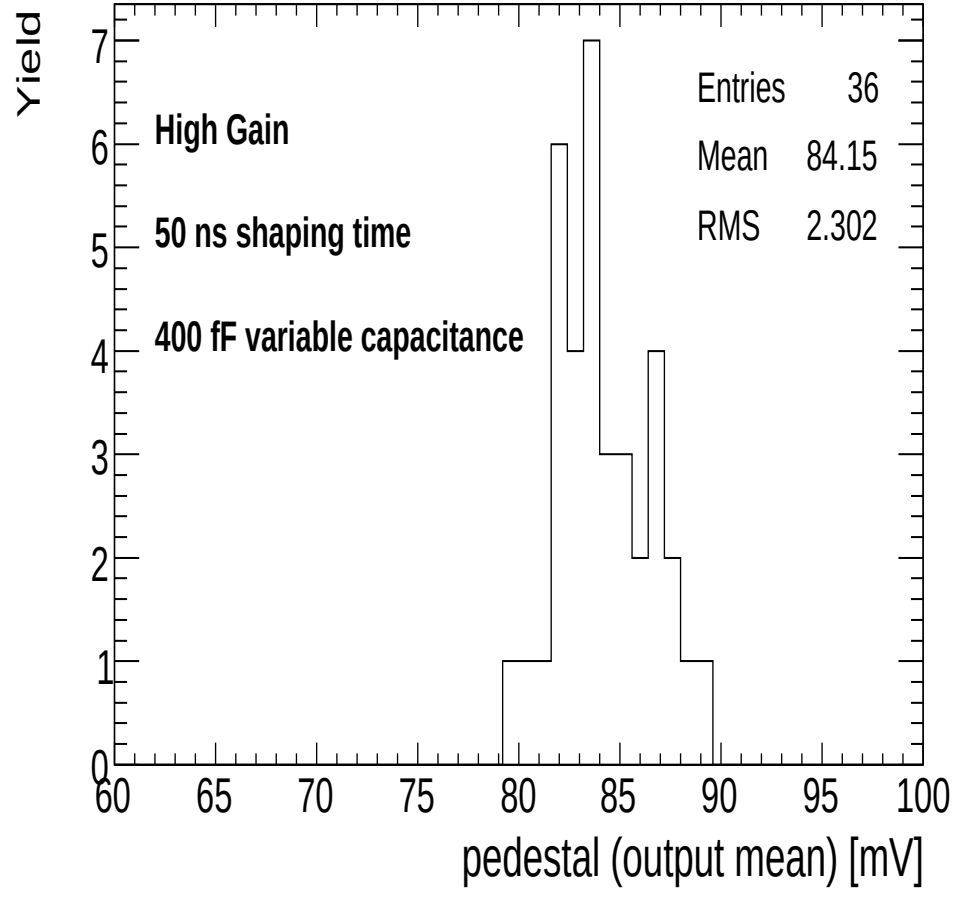


Non uniformity is negligible

Pedestals Uniformity

- **Pedestal measured in all 36 channels (input lines not connected)**



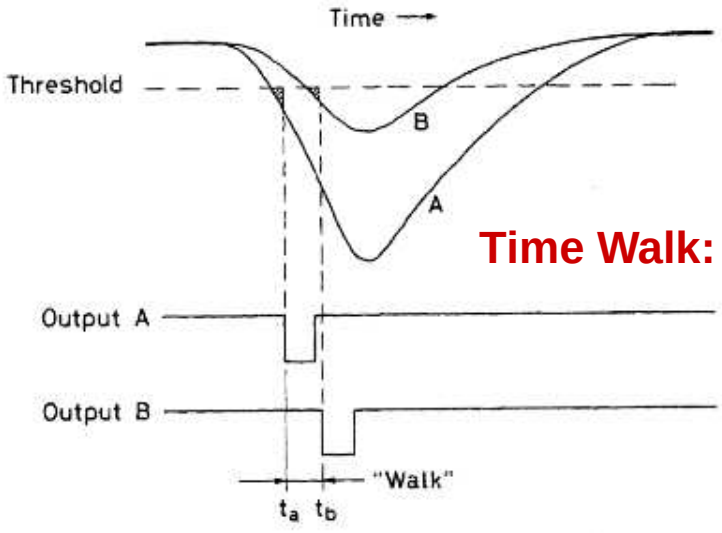


Spread slightly larger than what reported by Orsay group

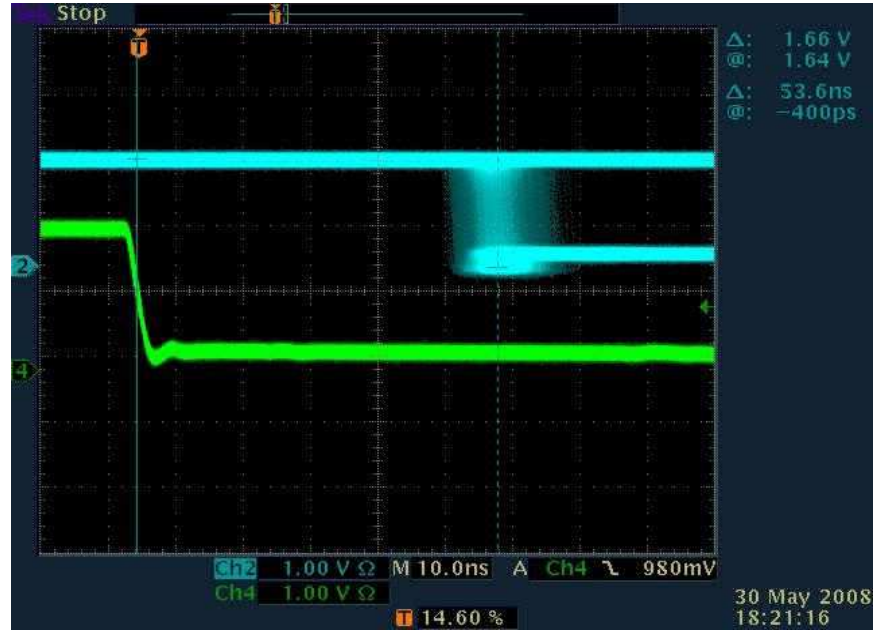
Trigger Time Walk and Jitter

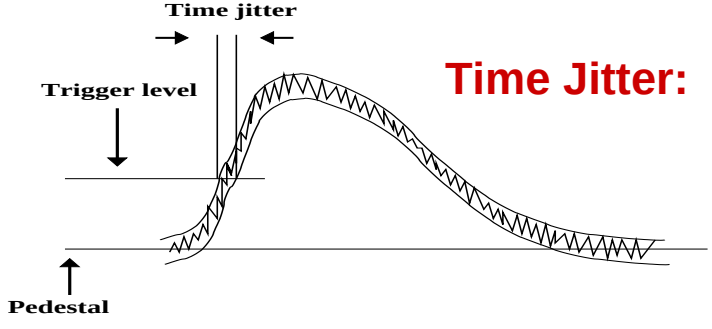
- **Main uncertainty of trigger timing:**

  amplitude dependence



Time Walk: ⇒ **Mean**



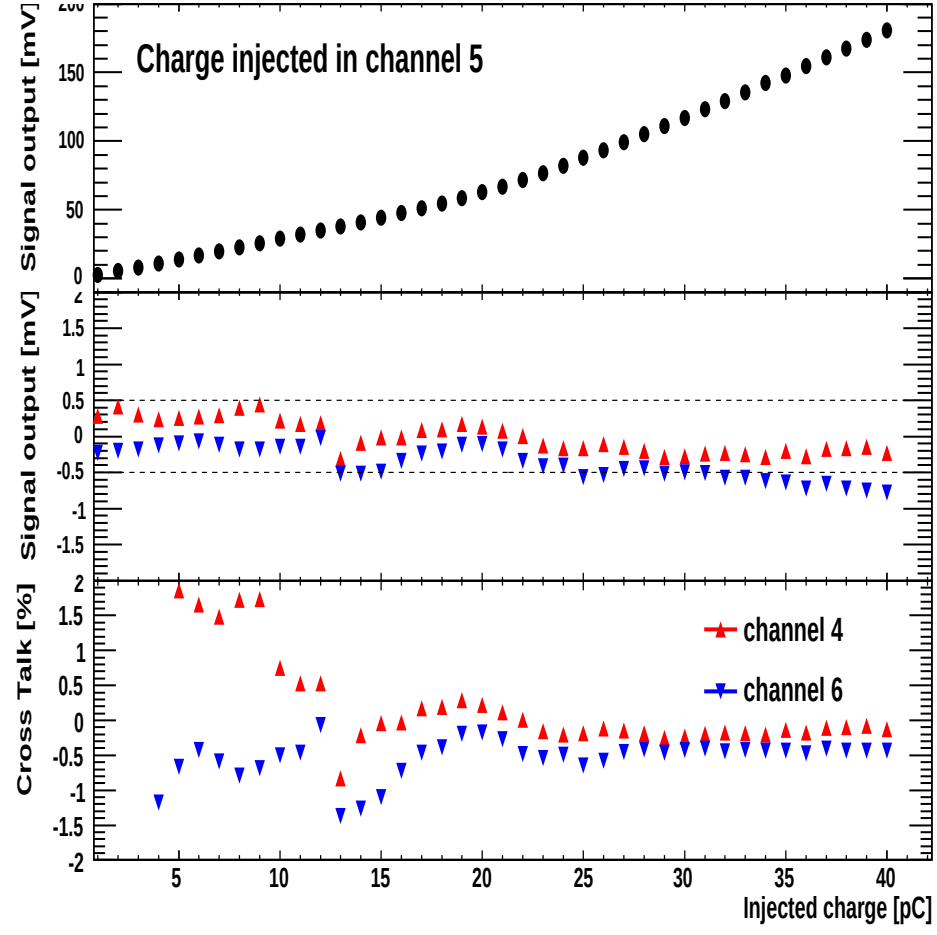


Time Jitter: ⇒ **RMS**

noise dependence

Cross-Talk between Input Channels

- **ASIC should handle 36 input lines**
- **Orsay measurements presented for low injected charge values**
  - **— estimated cross-talk: $\approx 0.3\%$ at $Q_{inj} = 15$ pC**
- **Extend measurements to wider input charge range (up to ≈ 33 mips)**



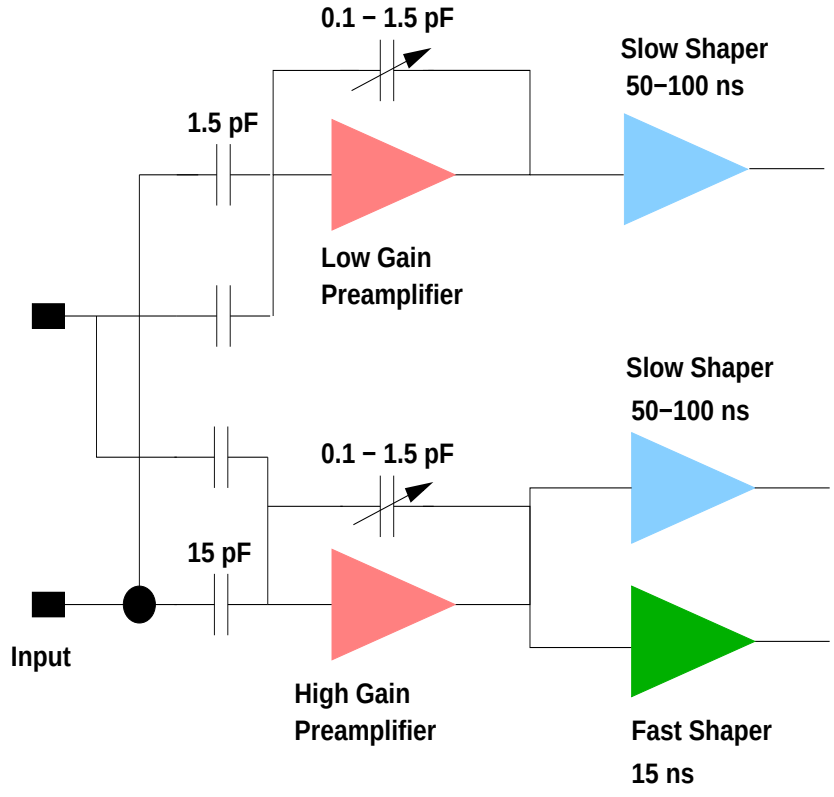
⇒ Pedestal variation within $\approx \pm 0.5\%$ mV

⇒ Result close to previous measurement

- **— within systematics (fluctuations)**
- **— fluctuations given by setup/analysis ?**

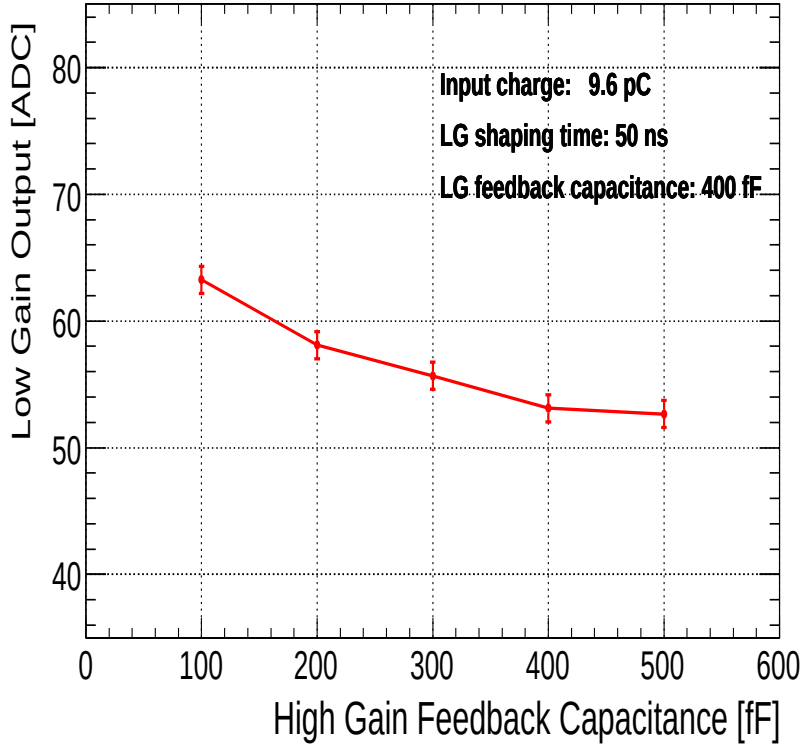
Low Gain - High Gain Coupling

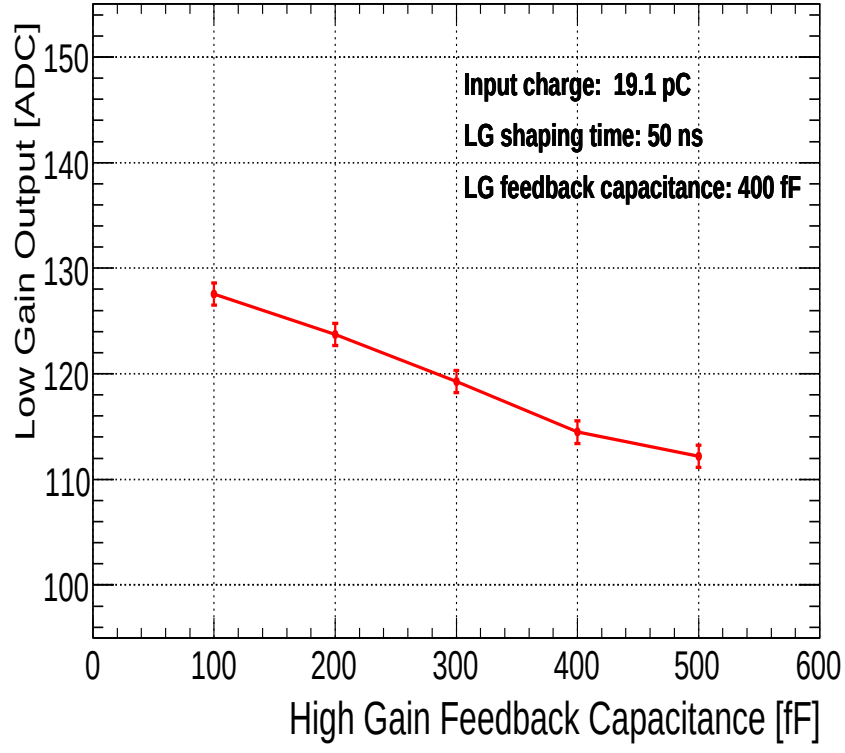
- **Low and high gain paths are electrically coupled**
  - **— charge sharing between paths influenced by preamplifier gain**



Low Gain - High Gain Coupling

- Low and high gain paths are electrically coupled
  — charge sharing between paths influenced by preamplifier gain
- Negligible effect in high gain path by LG preamplification

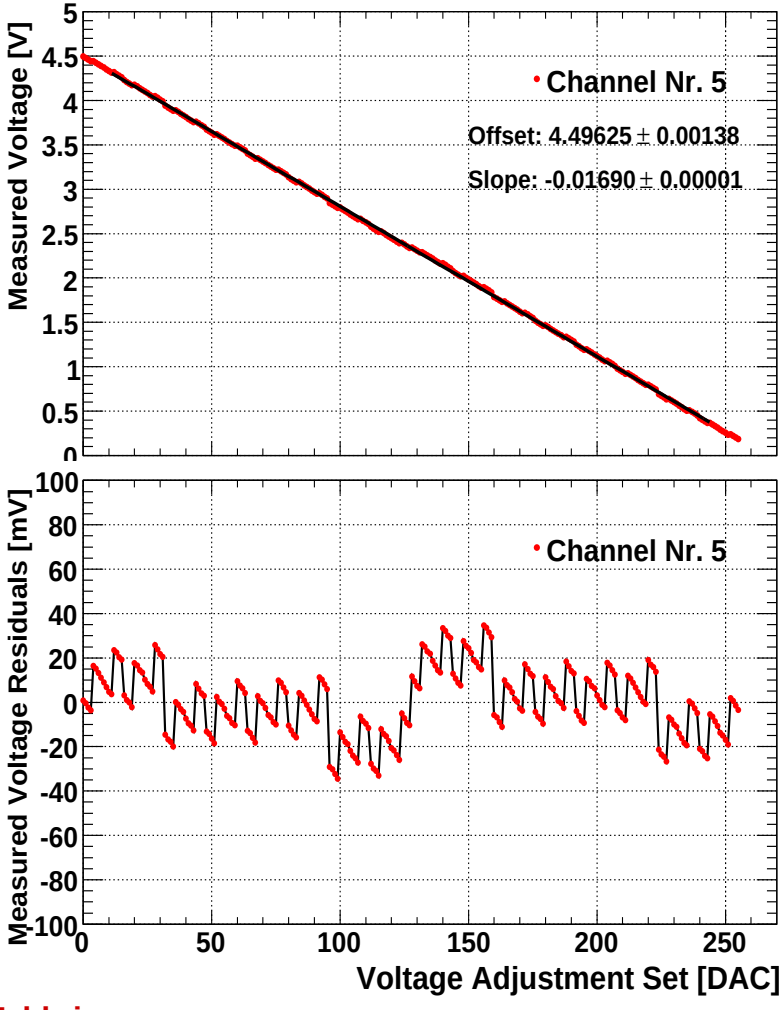


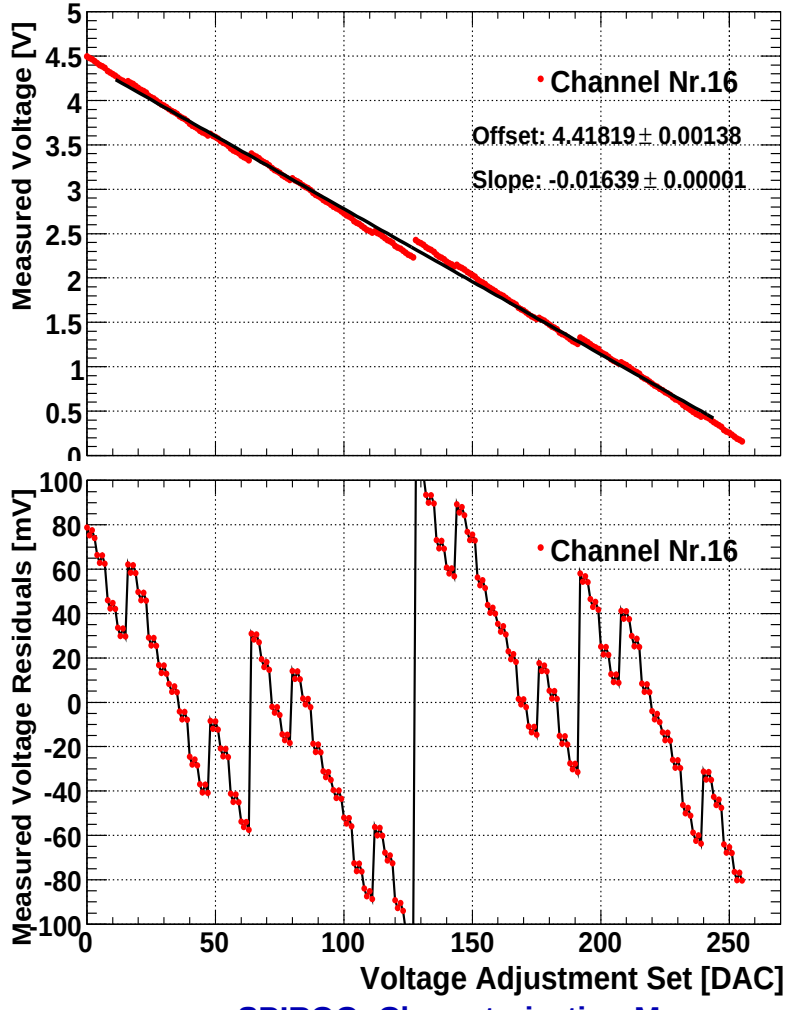


- Up to 10% effect in low gain path by HG preamplification

SiPM Voltage Adjustment

- ASIC forseen to provide common forward voltage to 36 connected SiPMs
- Single channel voltage tuning provided by dedicated 8 bit DAC adjustment
- Calibration of DAC to HV performed via dedicated LabView routines



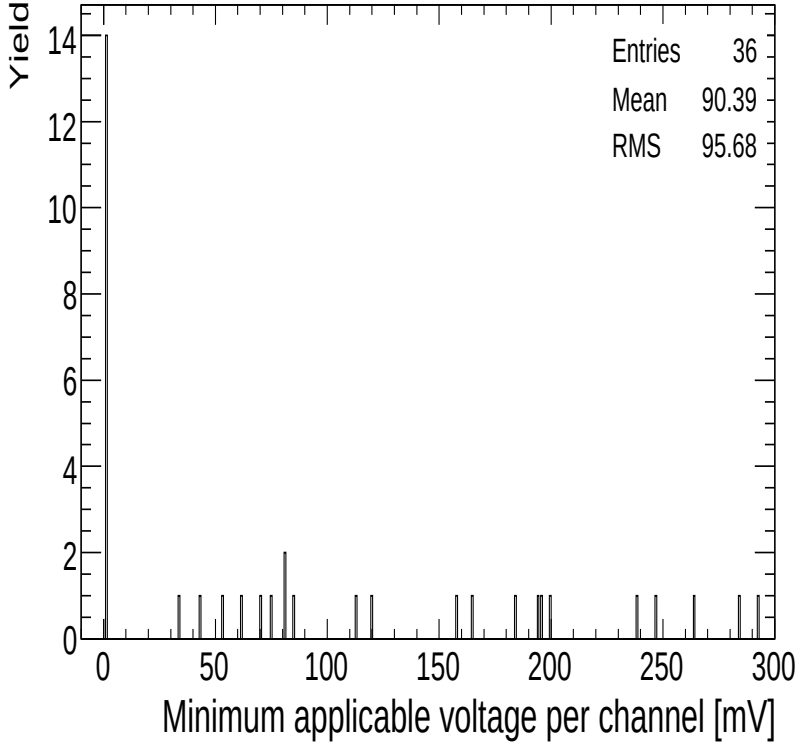


SiPM Voltage Adjustment

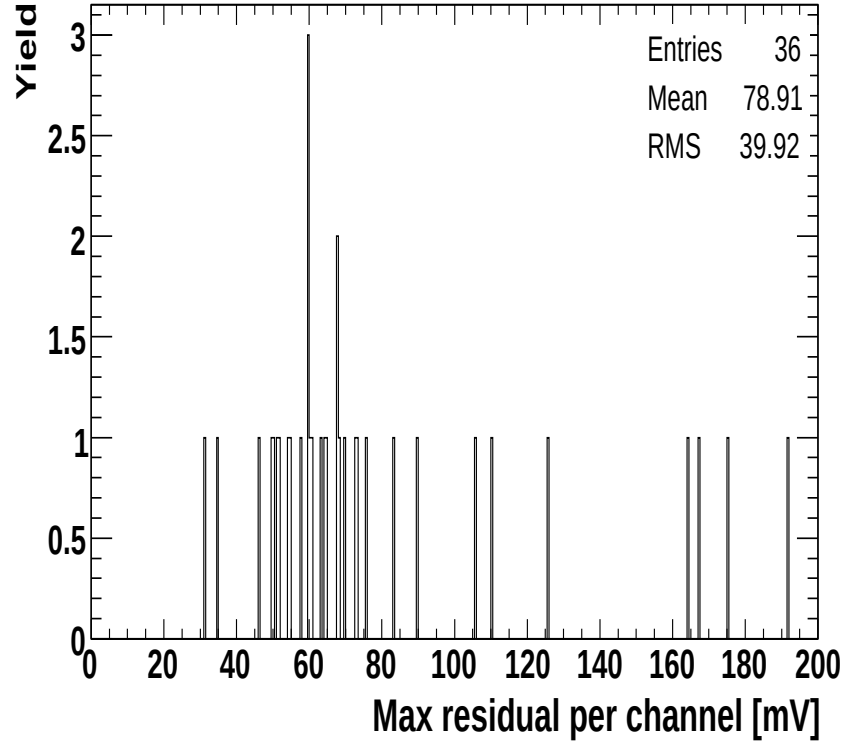
Applied voltage ranges approximately between 0.0 and 4.5 V

- **Possible Problems:**

Ranges differ channel by channel



Residuals up to 200 mV



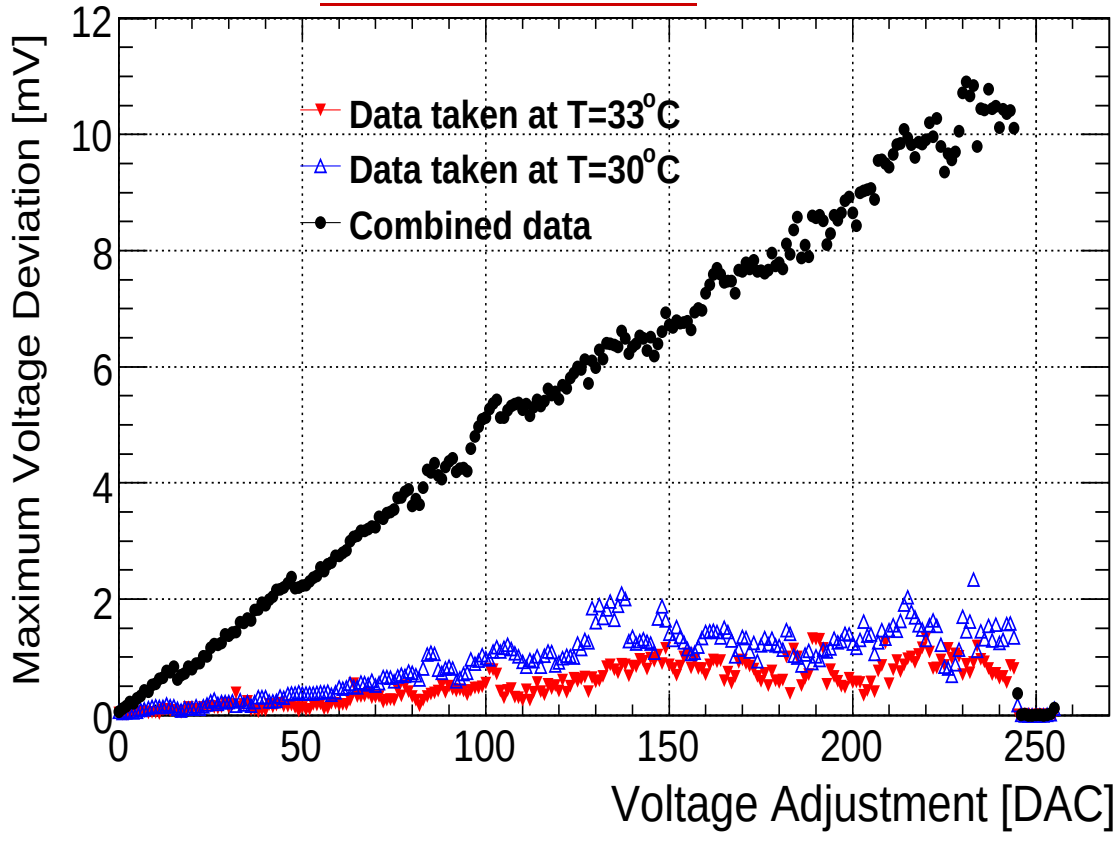
$\Rightarrow$ **Relative gain change of $\approx 5.2\%$ due to large residuals ($\frac{\Delta G}{G \Delta V} \approx \frac{2.6\%}{100mV}$)?**

$\Rightarrow$ **Systematical uncertainty to energy calibration?**

SiPM Voltage Adjustment

- **Although residuals in HV DAC scan sizable, they are reproducible!**

Two sets of scan:

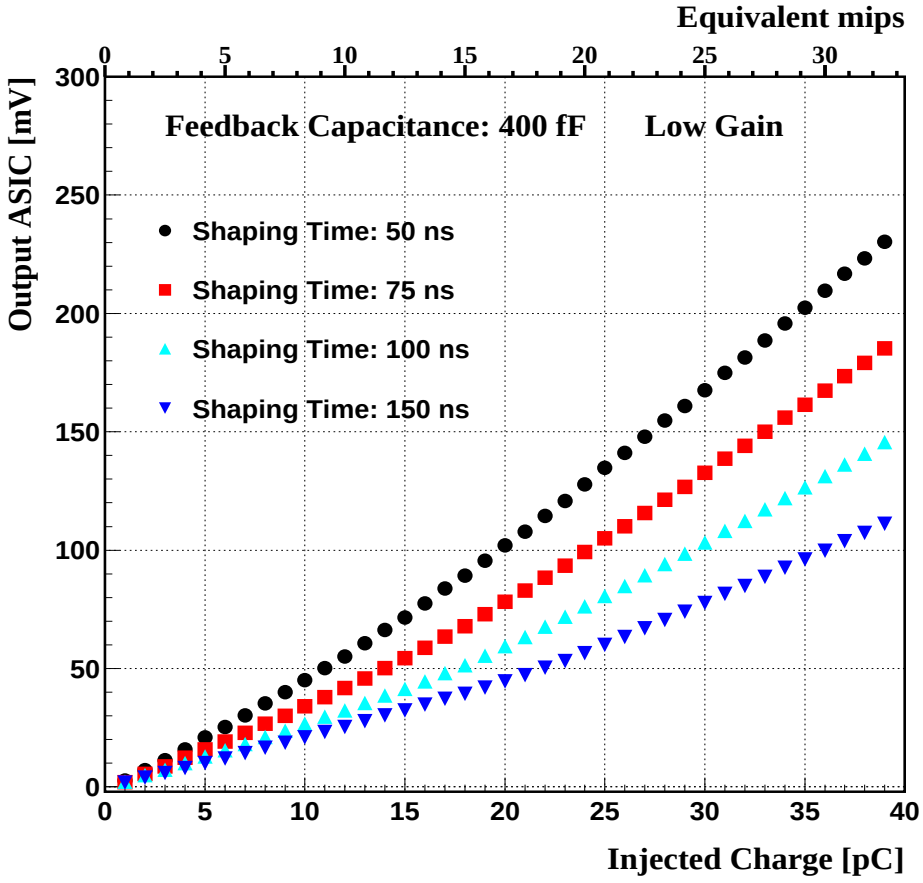


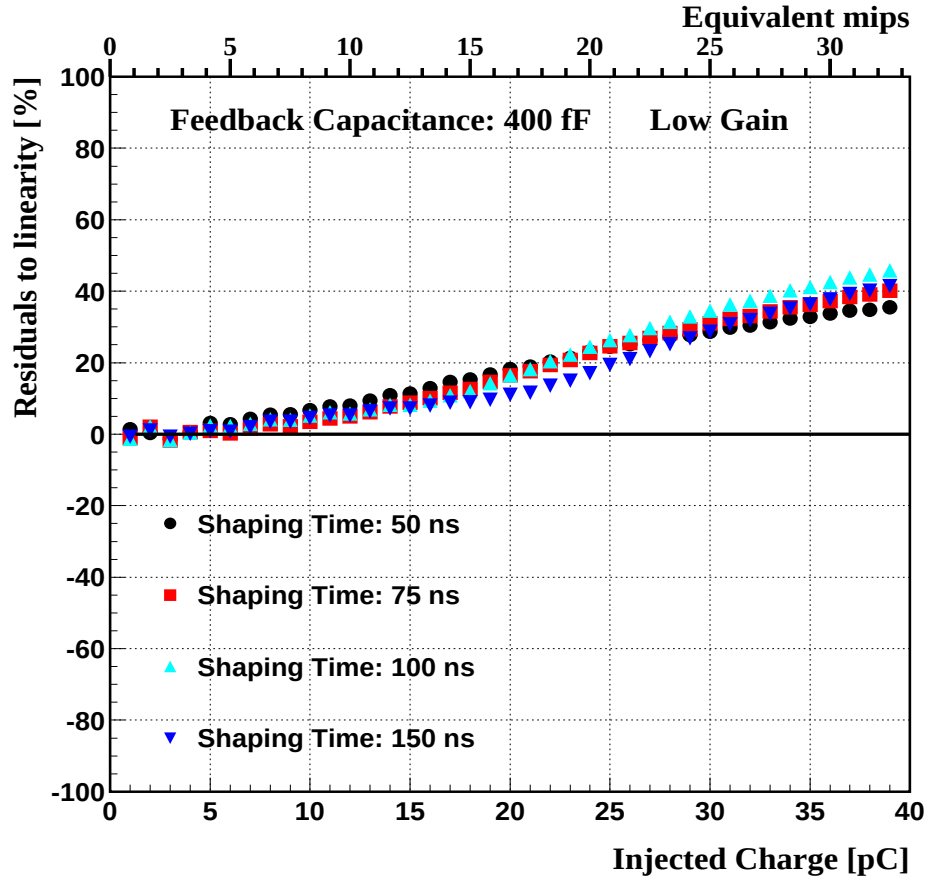
⇒ **Negligible effects observed within each measurement set**

⇒ **Effects from temperature can be corrected for via calibrations**

Dependence on Shaping Time

- **Hold signal timing kept fixed during input charge scan**
  - **— take mean peaking time during scan**
- **Hold signal timing changed according to shaping time**

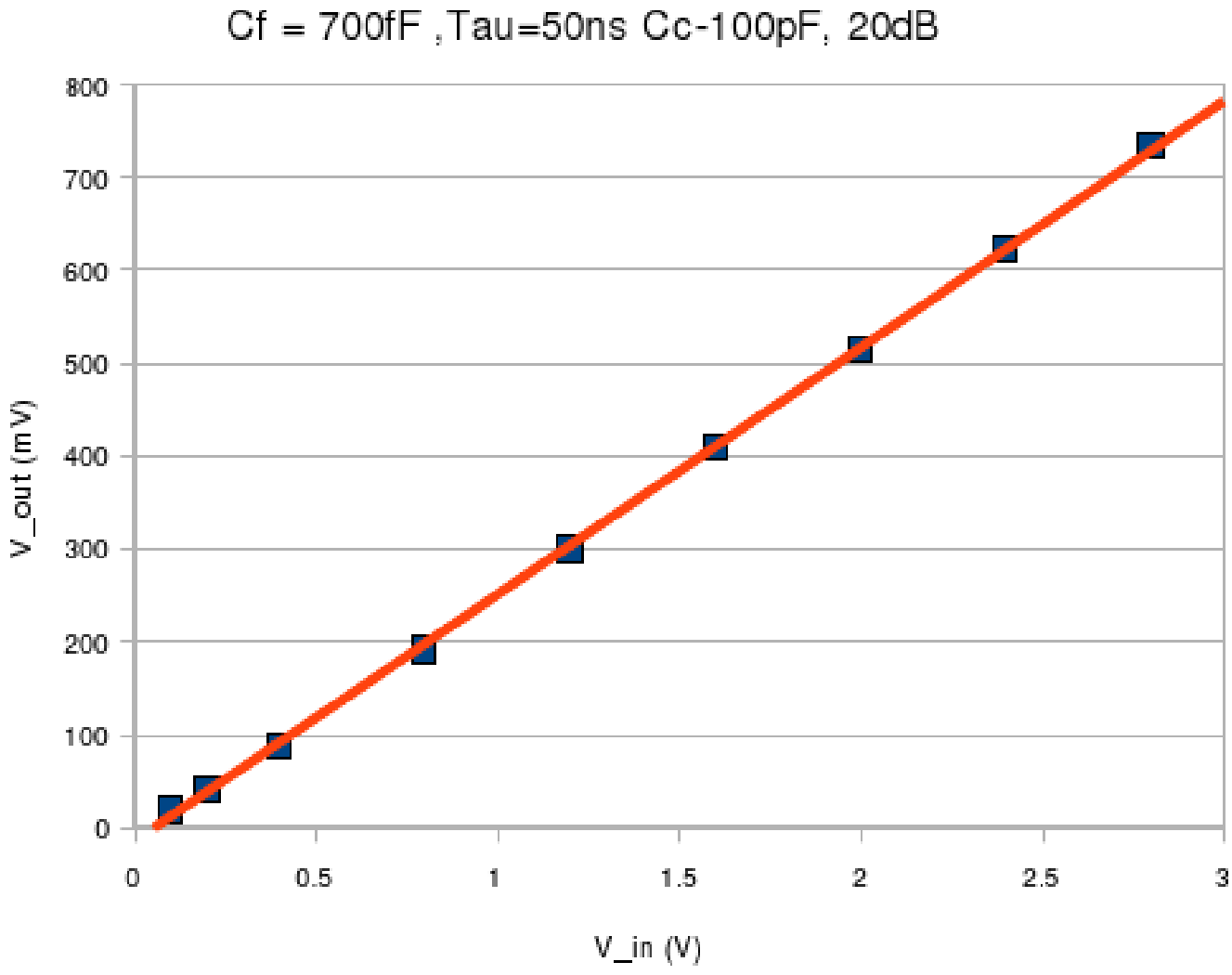




⇒ **In agreement with simulations**

Peaking Amplitude Linearity W/O T&H

- **The peaking amplitude was measured at the oscilloscope (w/o track and hold switch)**



Data Taking in Physics Mode

- **We want a proof of principle that chip can operate in auto-trigger mode (1/2 mip cut)**

  — need to know first where threshold is applied / mip amplitude

Strategy:

- **Process signal from SiPM (LED fired) at different threshold values**

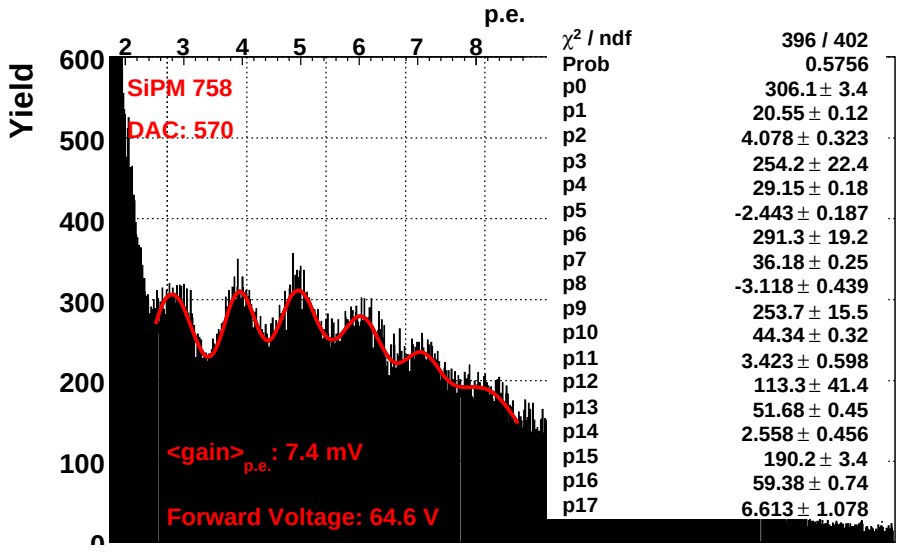
$\Rightarrow$ **Considering entire DAC scan, on average additional 20 DAC units suppress one peak**

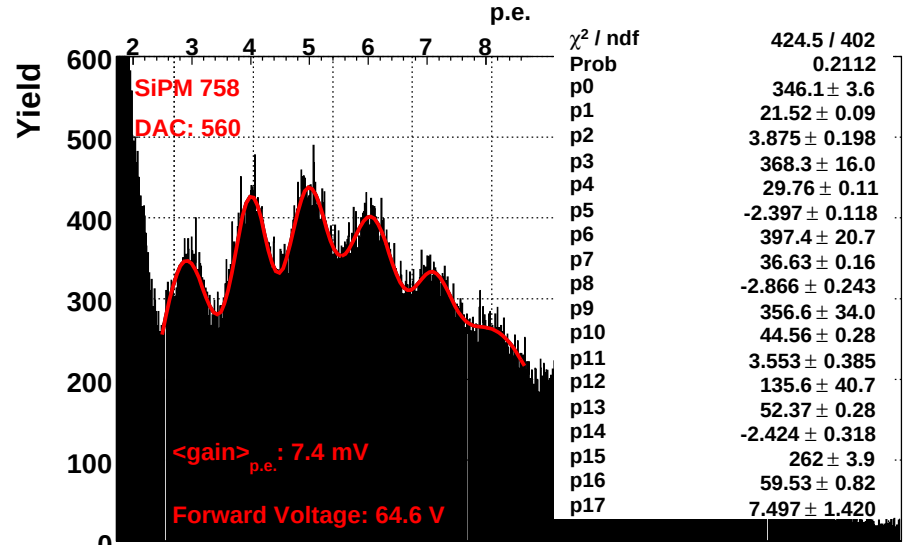
DAC value	Suppressed peak number
530	3
510	4
490	5
470	6
450	7
430	8
410	9
390	10

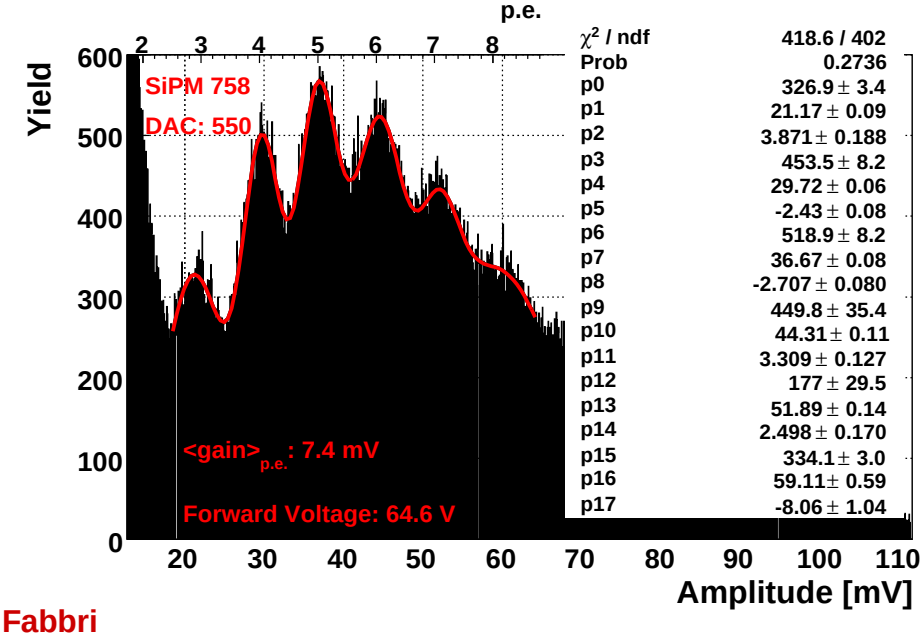
$\Rightarrow$ **LED amplitude tuned to generate one mip signal (maximum around 15 pxls)**

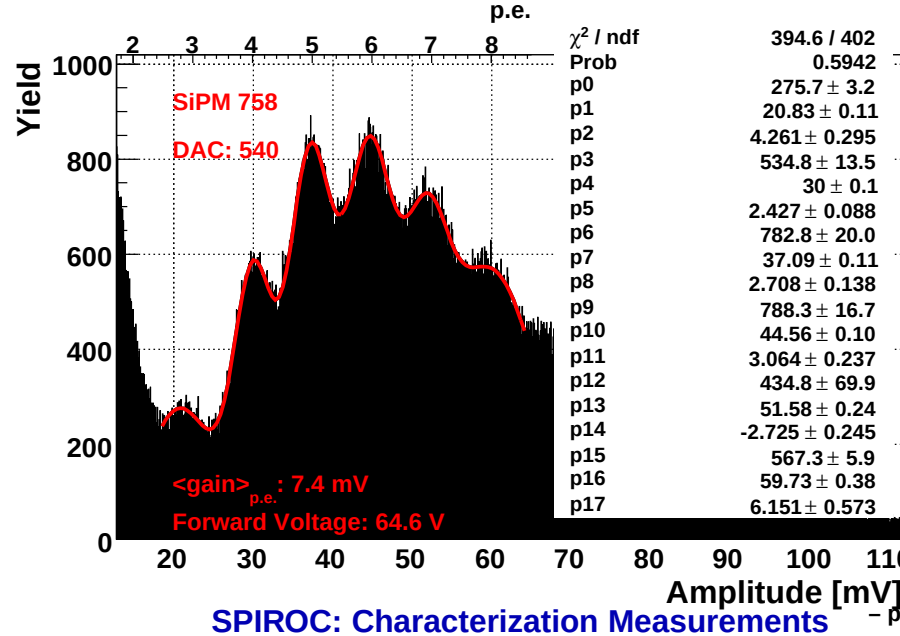
Determination of Trigger Threshold and SiPM Gain

SiPM signal for increasing values of DAC threshold



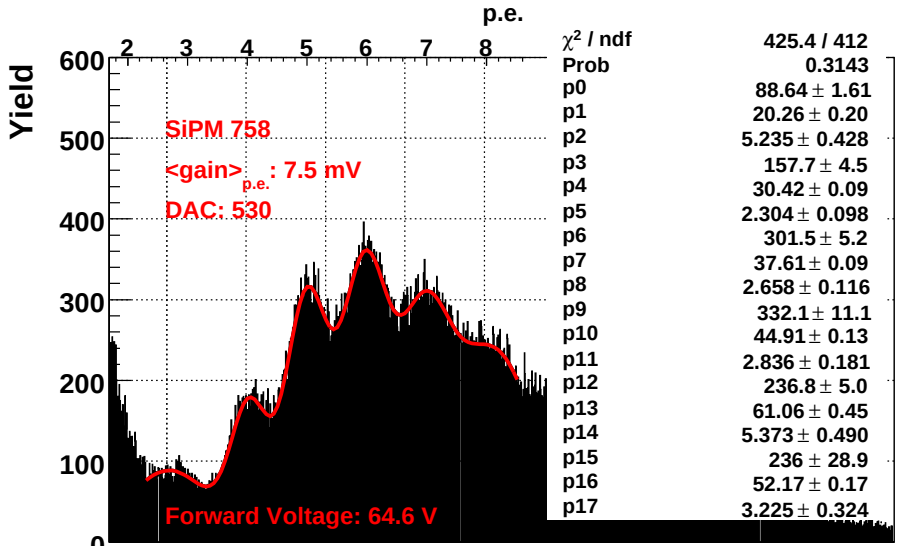


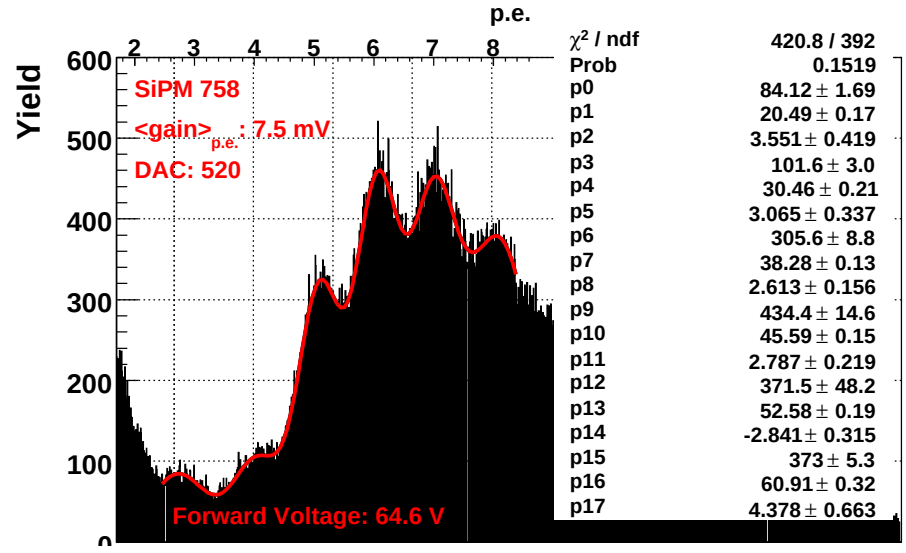


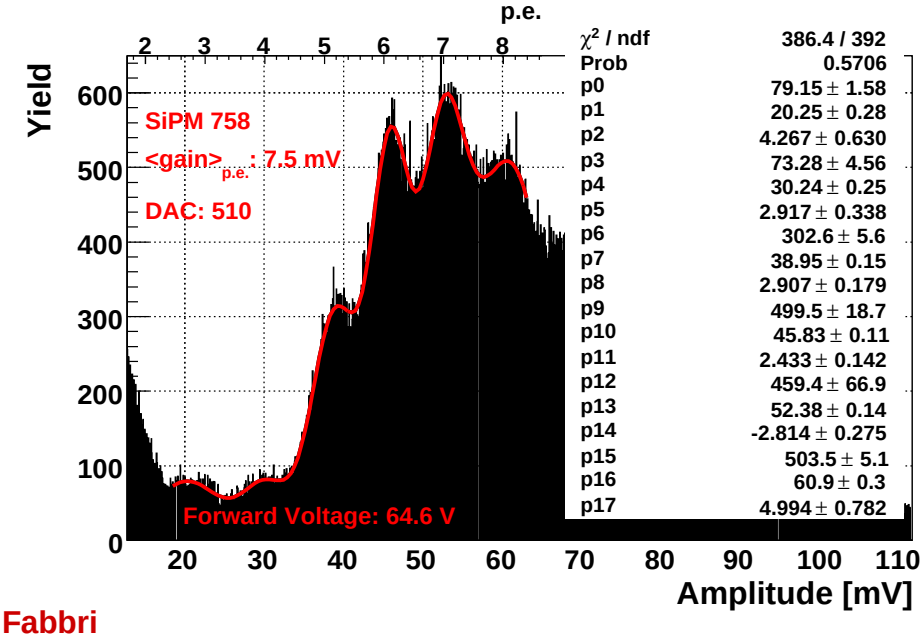


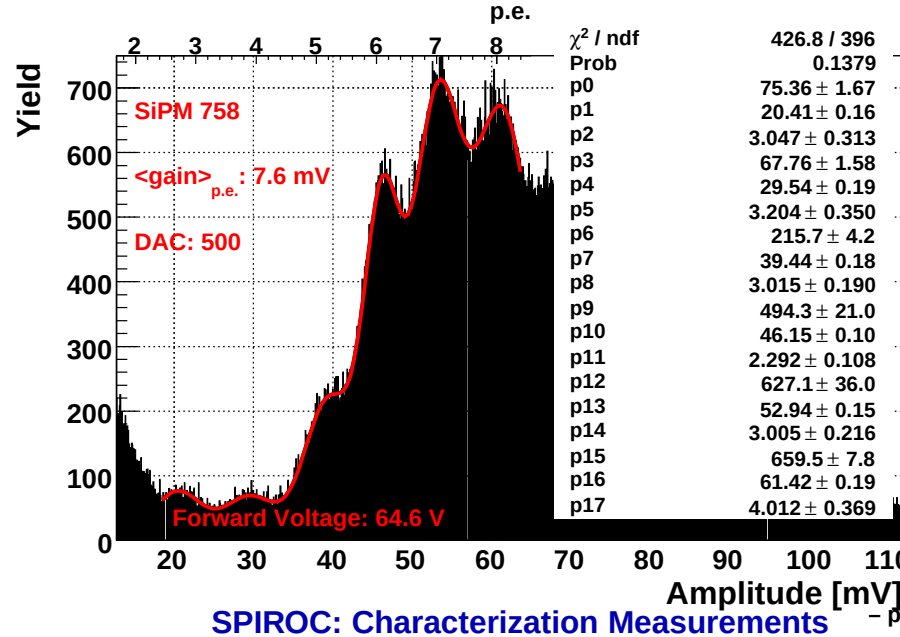
Determination of Trigger Threshold and SiPM Gain

SiPM signal for increasing values of DAC threshold



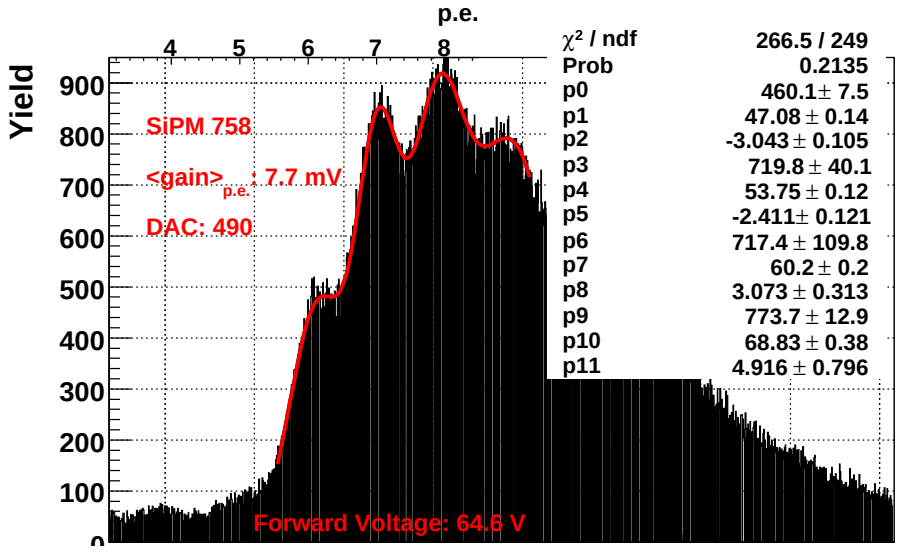


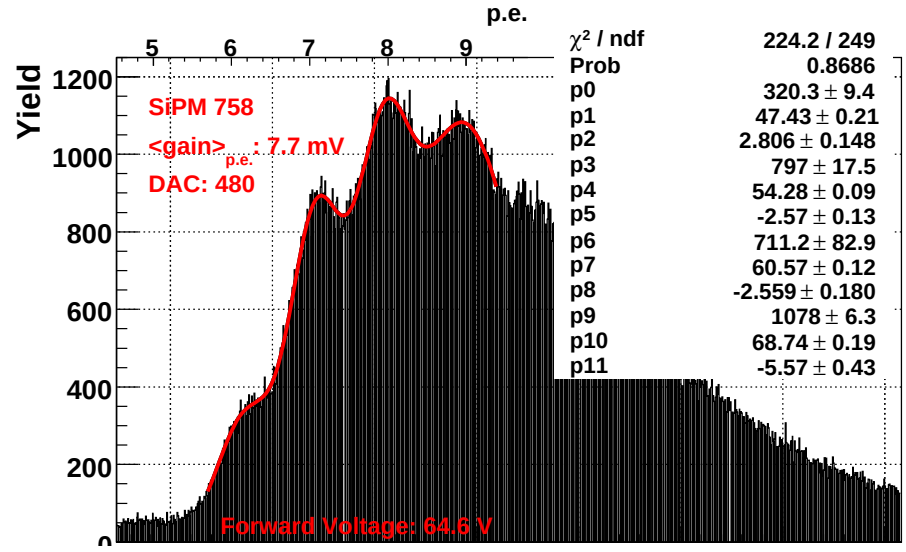


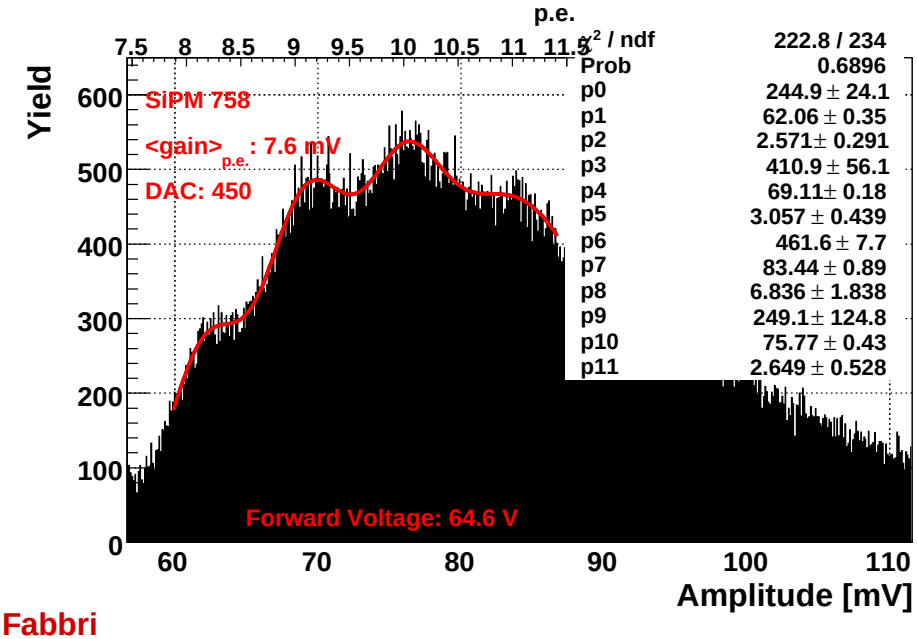


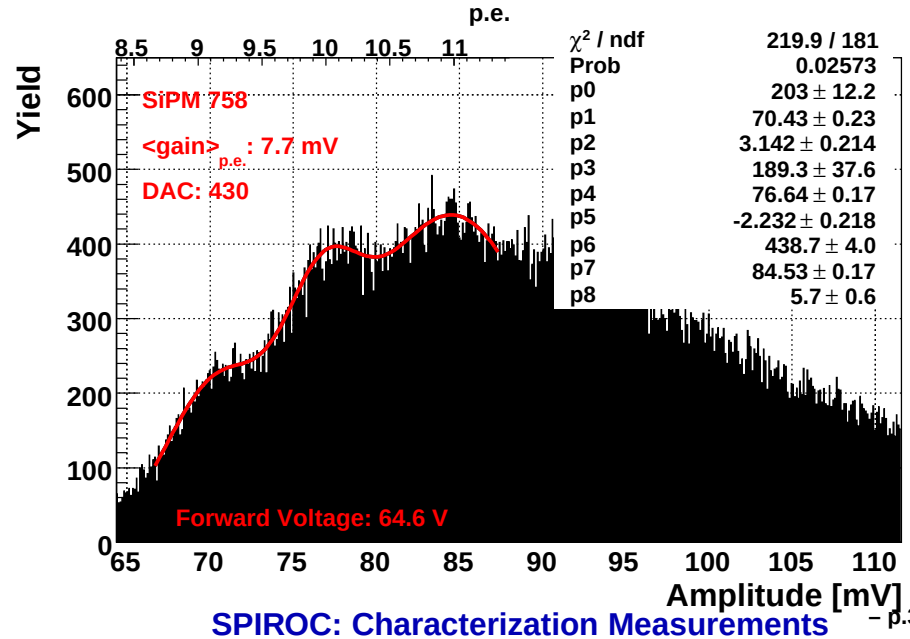
Determination of Trigger Threshold and SiPM Gain

SiPM signal for increasing values of DAC threshold



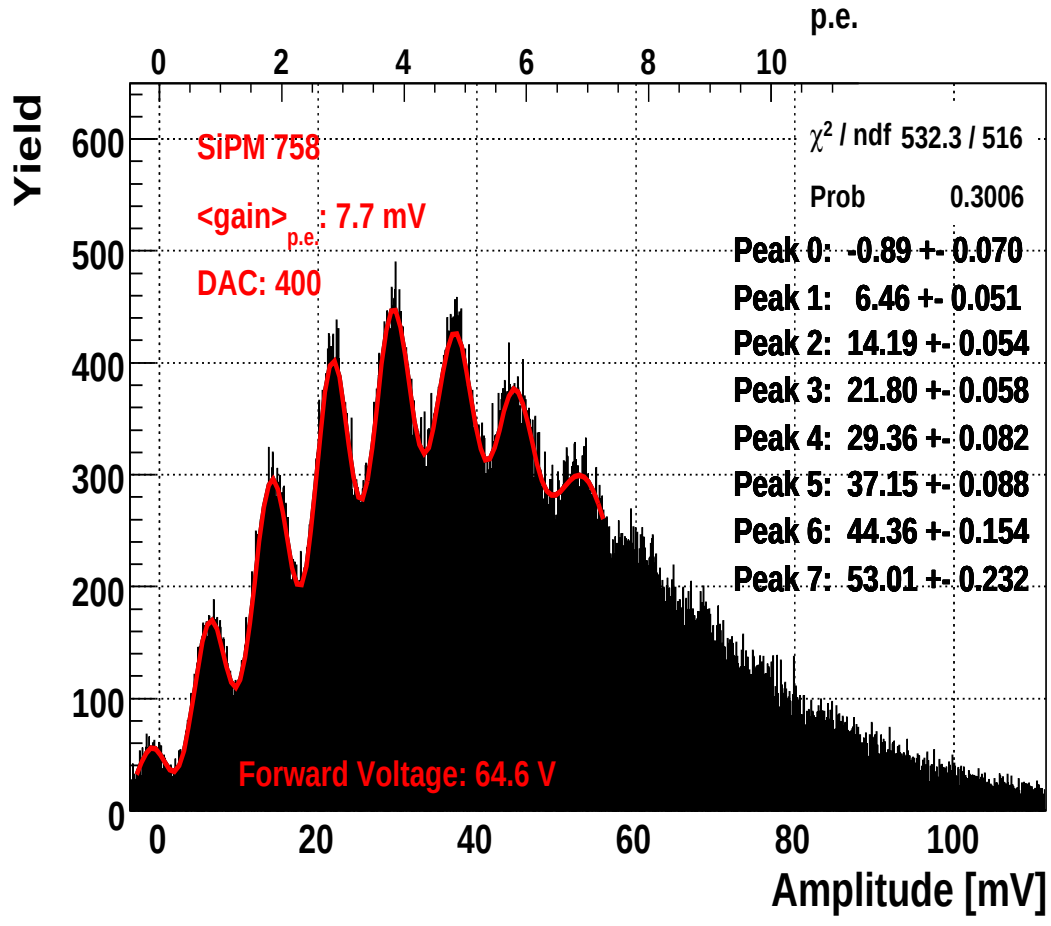






Determination of Trigger Threshold and SiPM Gain

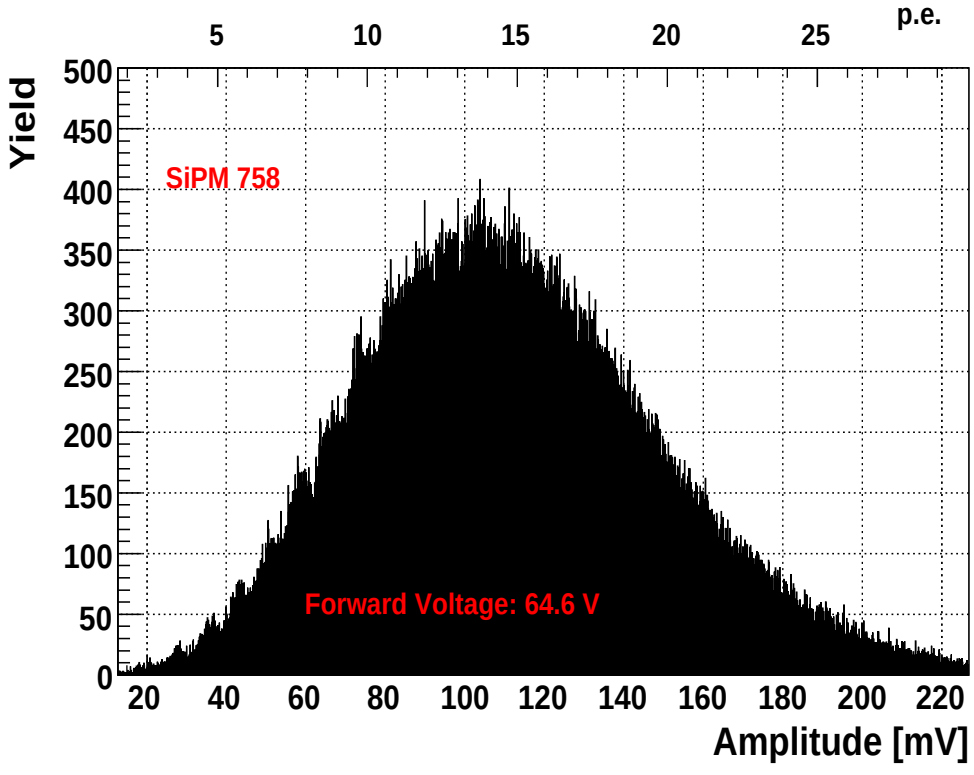
- **SiPM signal with external trigger (for ADC gate and HOLD)**



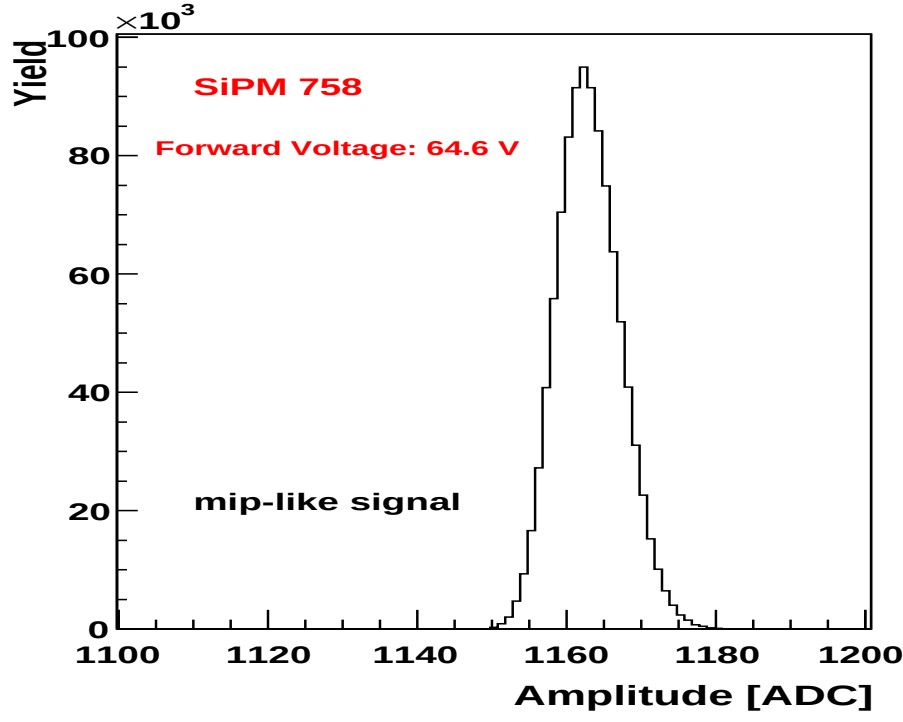
Mip SiPM Signal in High and Low Gain Modes

- **SiPM signal with external trigger (for ADC gate and HOLD)**

High Gain



Low Gain

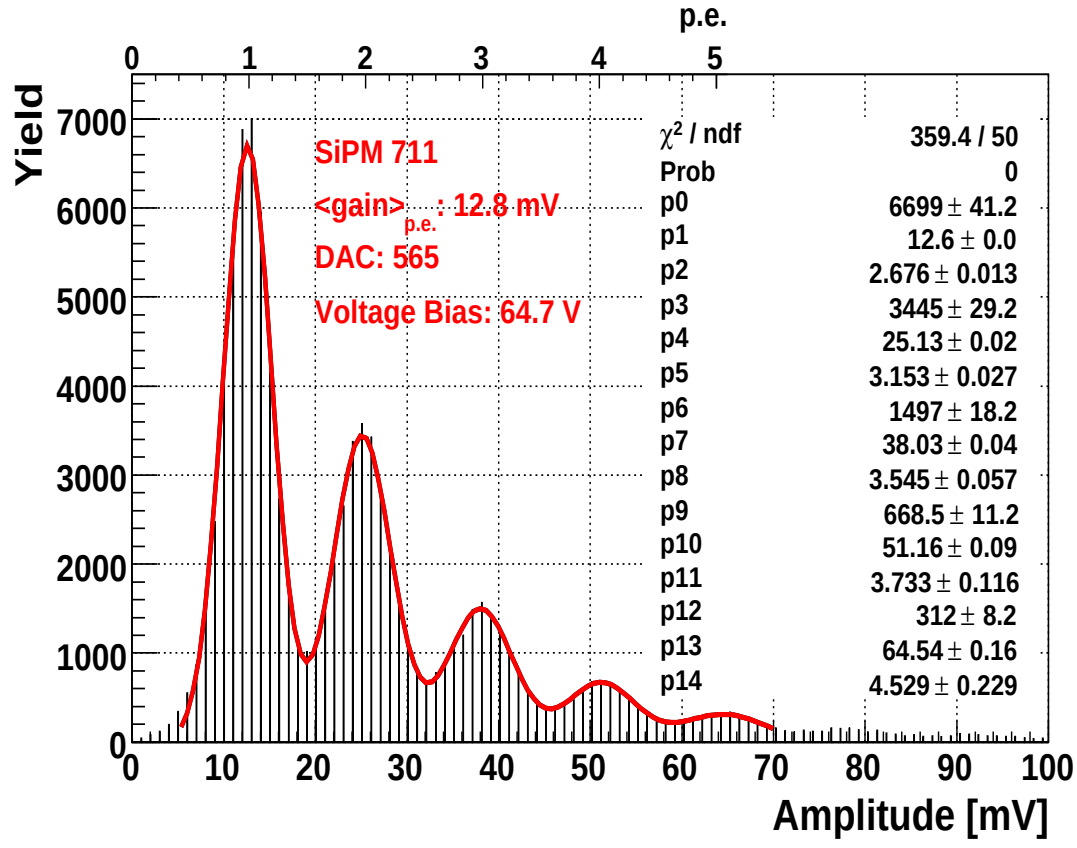


Single-Pixel Spectra

- Run SPIROC in auto-trigger mode
- Set discriminator threshold approximately above pedestal

  ⇒ LED can be also off due to overwhelming thermal noise

High pxl gain



⇒ Dominating thermal noise can be fitted

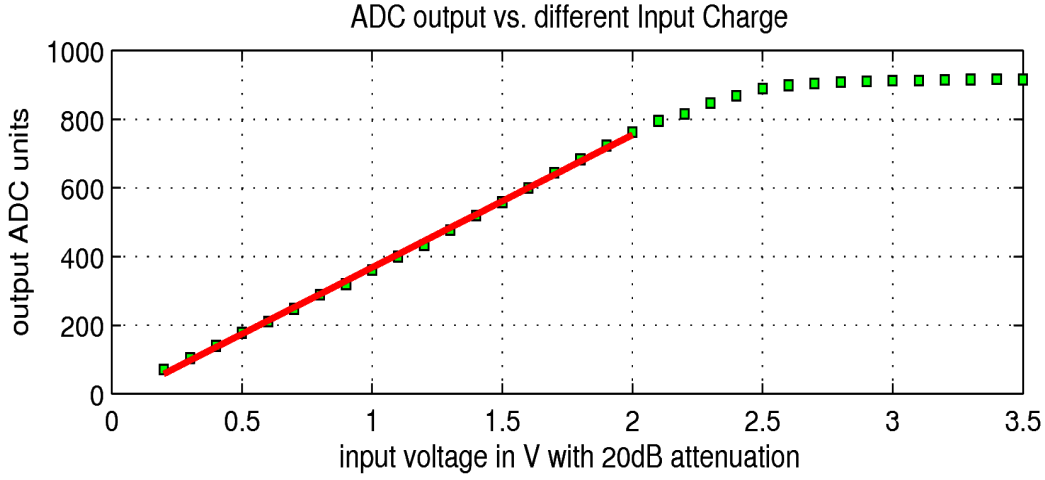
SPIROC II: Outlook

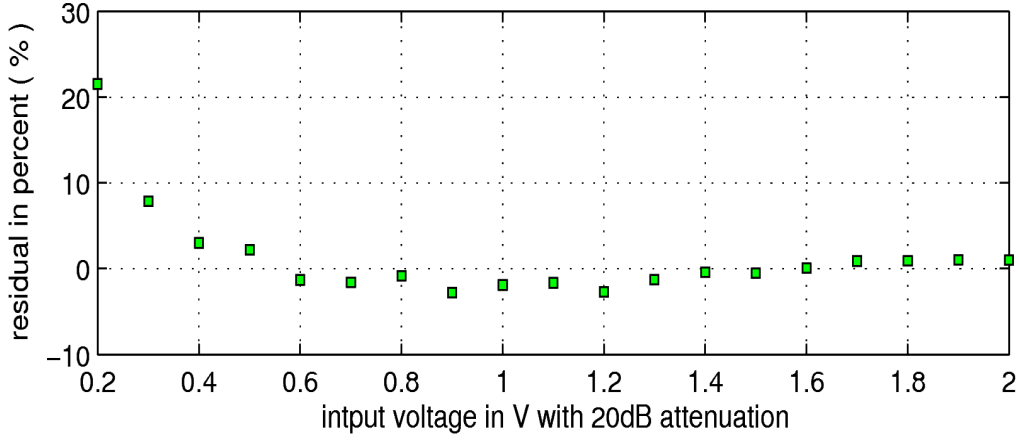
Analysis on going

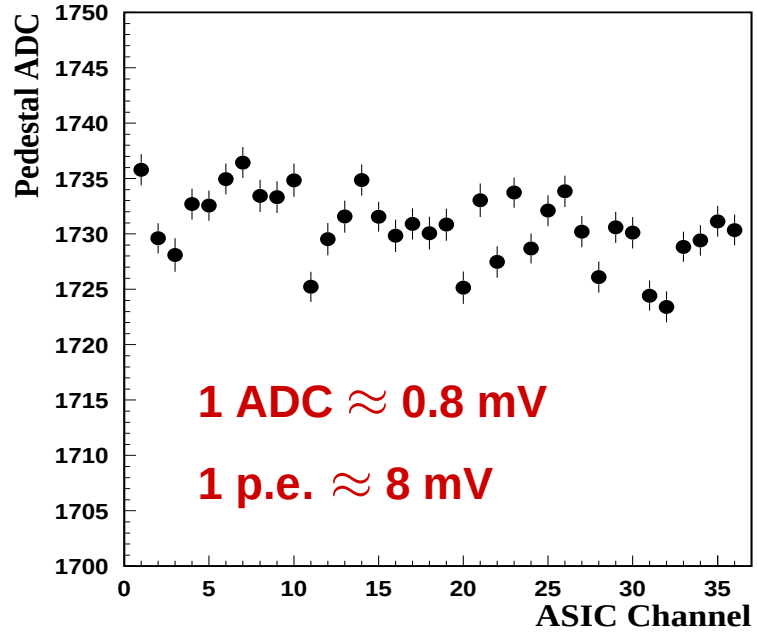
- **Digital part (Internal ADC) not usable in SPIROC I**

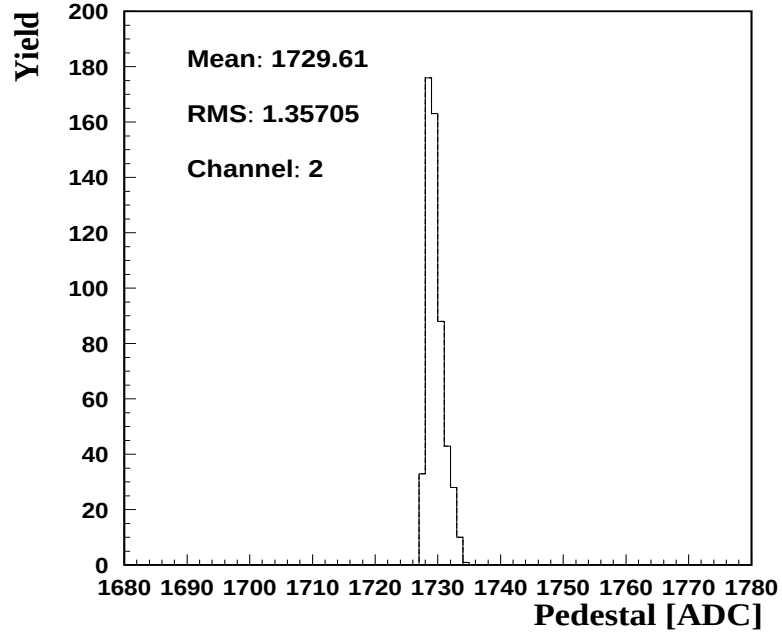
  — now fixed in SPIROC II

- **Linearity of Wilkinson ADC can be investigated**









⇒ Similar behaviour observed with ext ADC