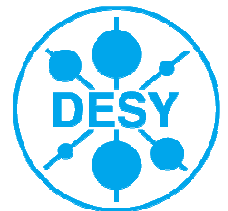


AHCAL Integration (JRA3).

Status and Outlook

Mathias Reinecke
for the AHCAL developers
EUDET annual meeting
Geneva, Oct. 19th – 21st, 2009



Outline

> JRA3 Hardware Developments at DESY

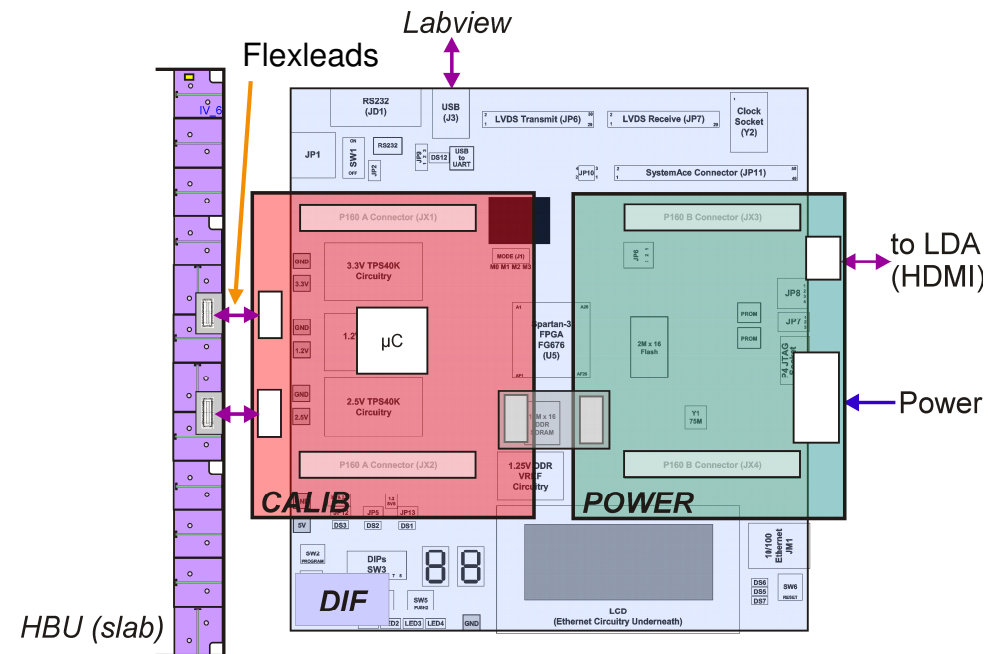
- CALIB, POWER, Flexleads
- HBU0
- DIF0 and DAQ interface (USB)
- Tiles integration

> System Commissioning

> The Next Generation

> Conclusions and Outlook

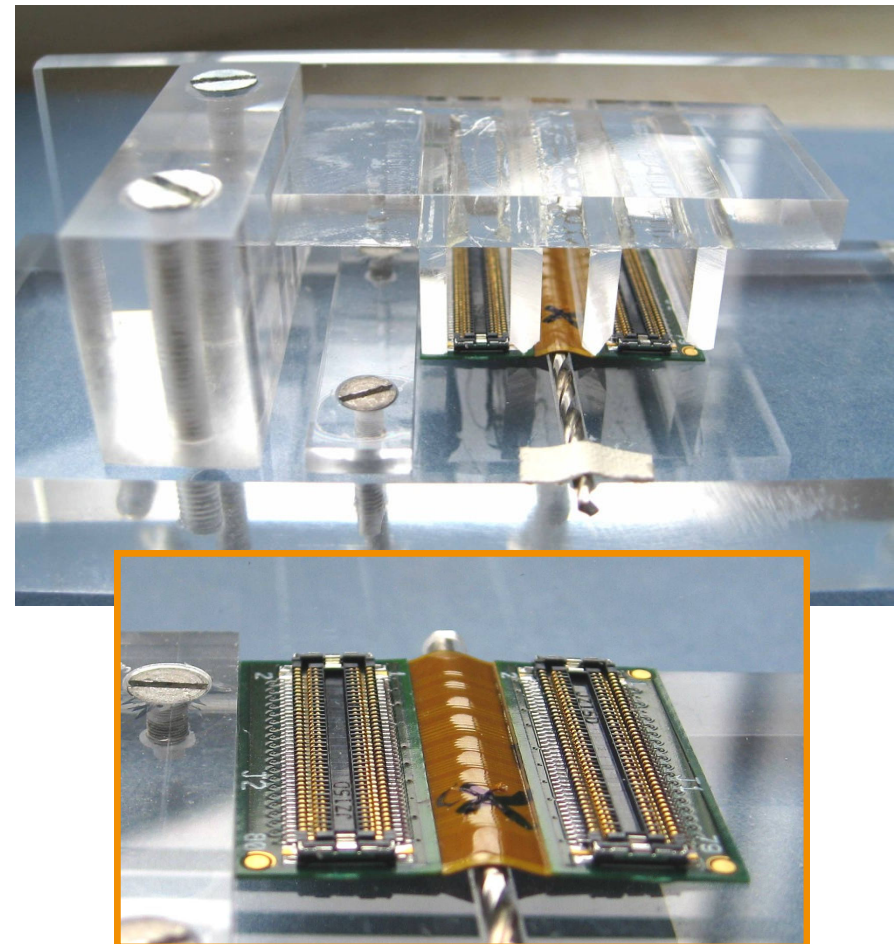
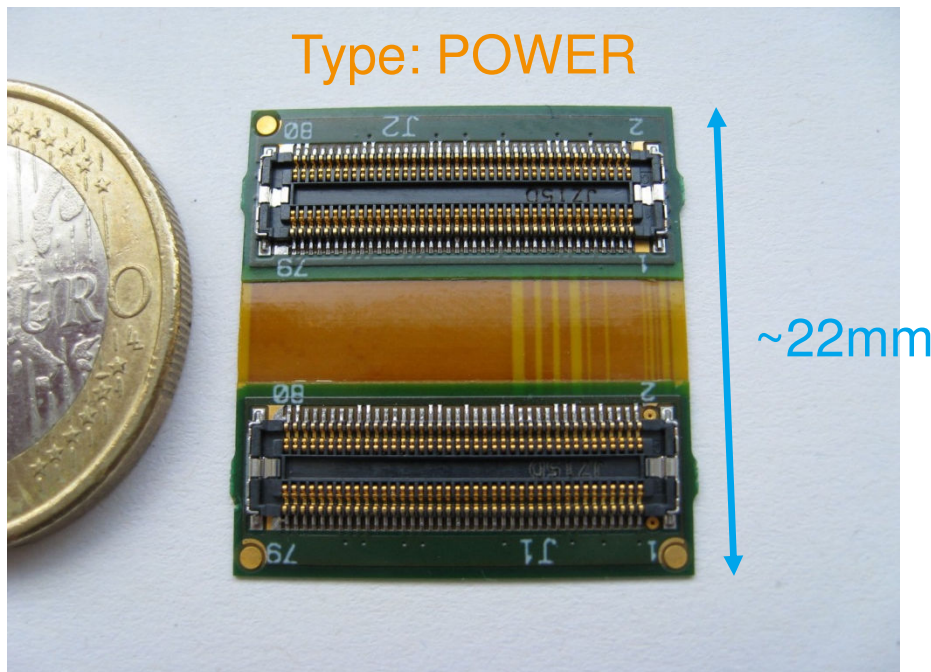
'old-fashioned overview'



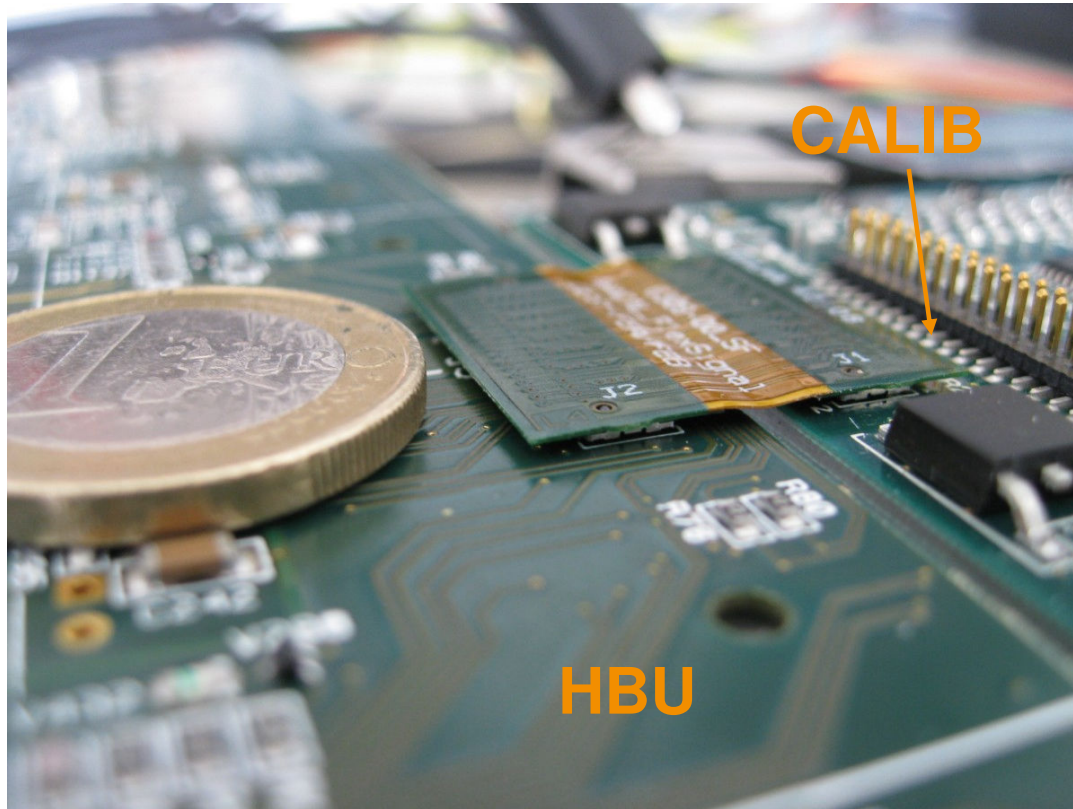
Flexleads – SIGNAL and POWER

- 20 pieces of each type finished.
- Pre-bending procedure ok.

Flexlead Pre-Bending:



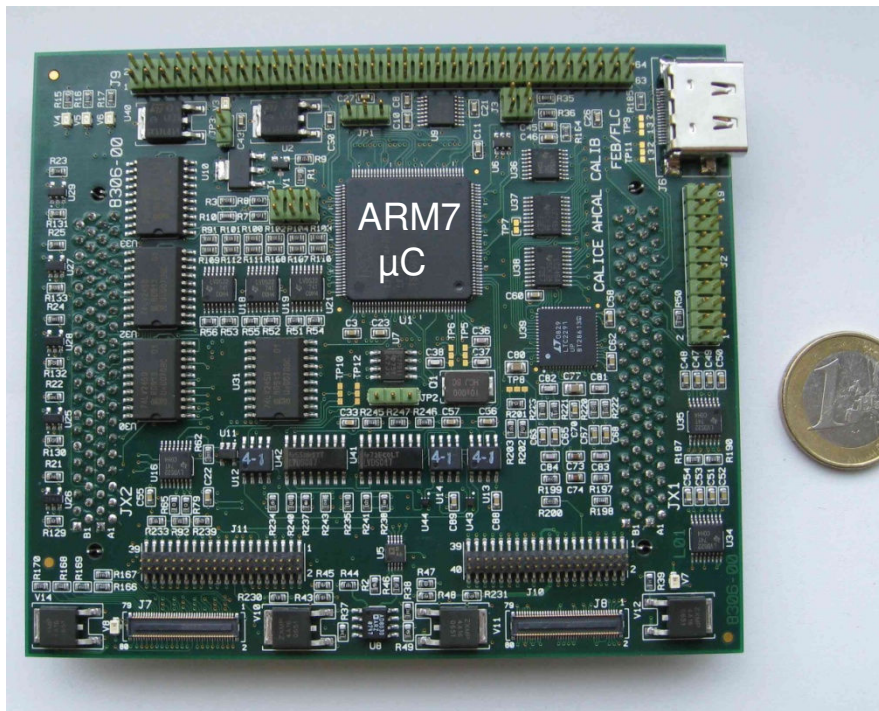
Flexleads – SIGNAL and POWER



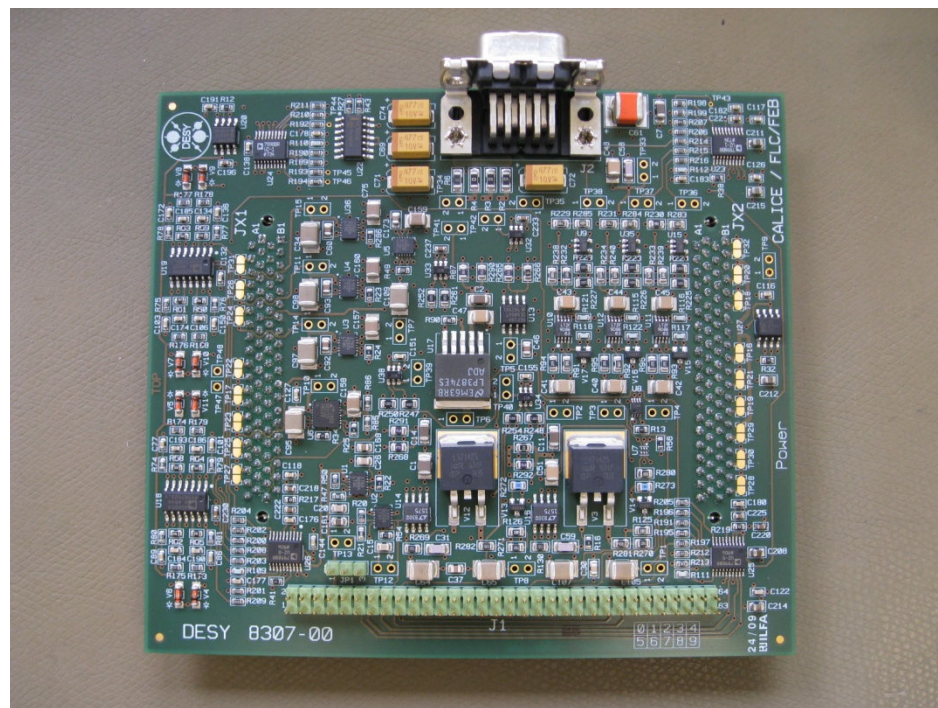
- > About 80 connection cycles up to now - still ok.
- > Compensate HBU misalignments in distance.
- > Fulfill AHCAL height requirements.
- > Tests ok concerning:
 - Signal allocation
 - Signal quality
 - Resistance for power

CALIB and POWER Modules

CALIB module: 11 x 10 cm²



POWER module: 12.5 x 11 cm²



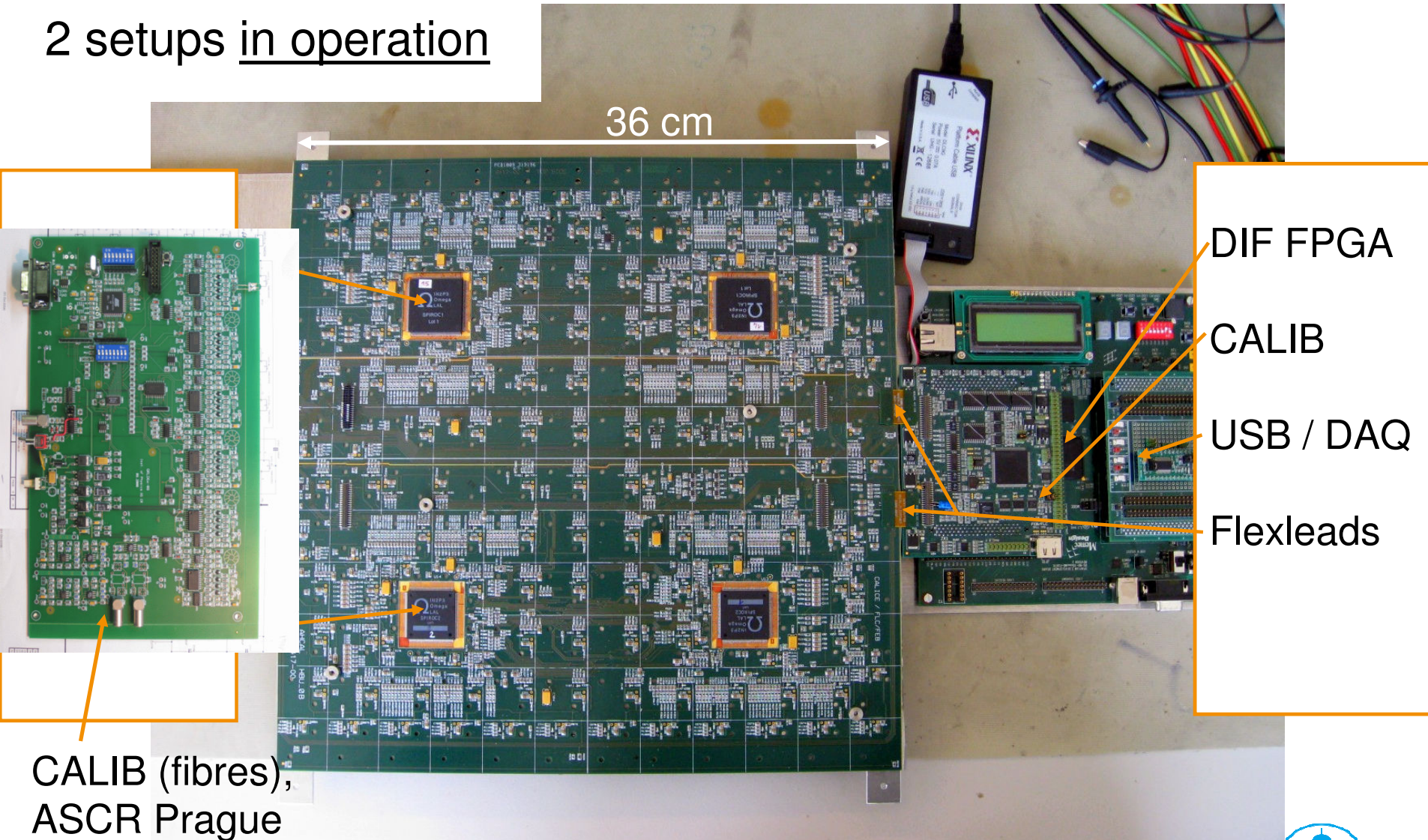
- 4 Modules of both types finished, in operation.
- First tests successful.

Sizes and heights: To be adapted to ILC mechanics later.

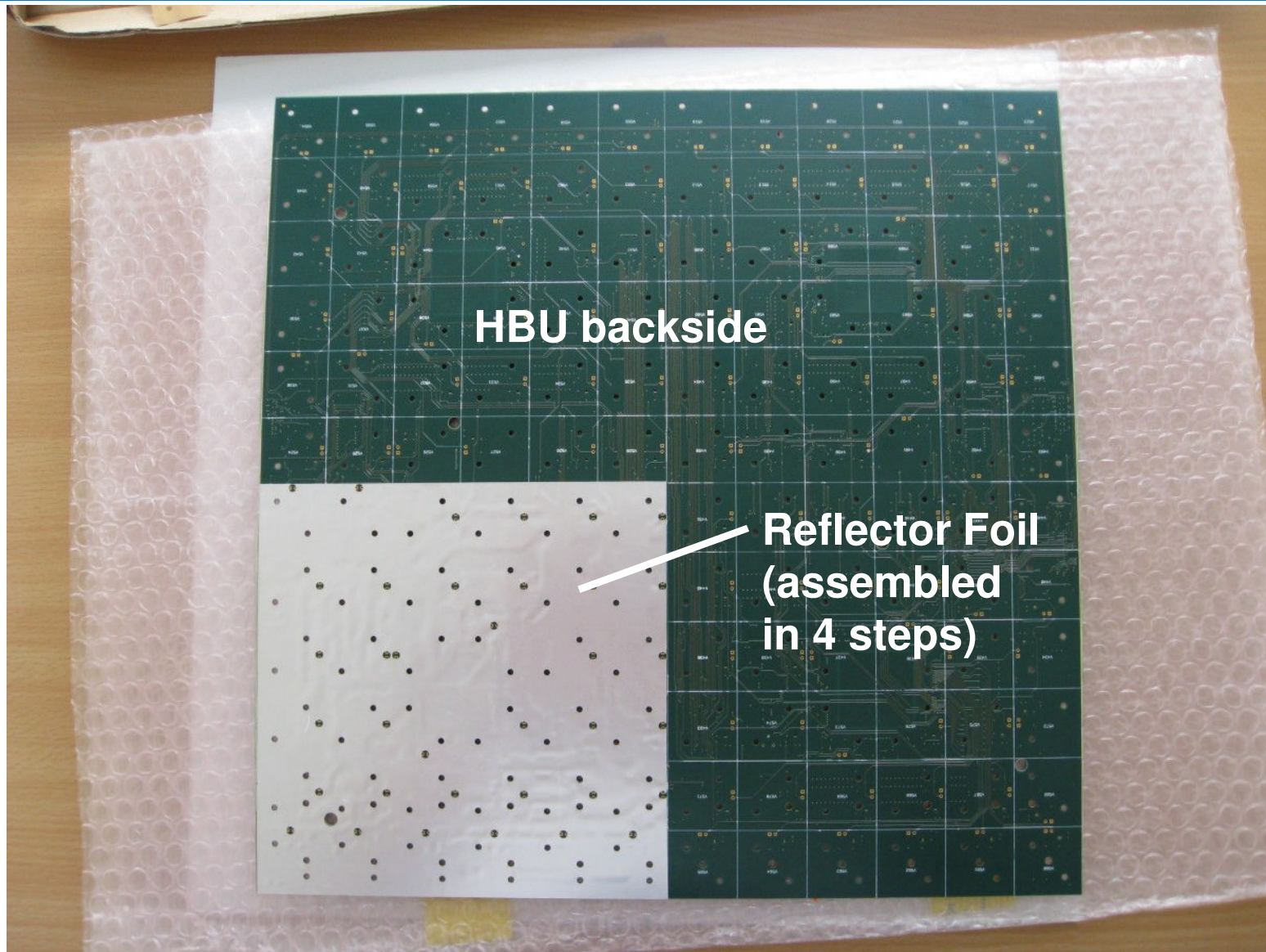


HCAL Base Unit (HBU) setup

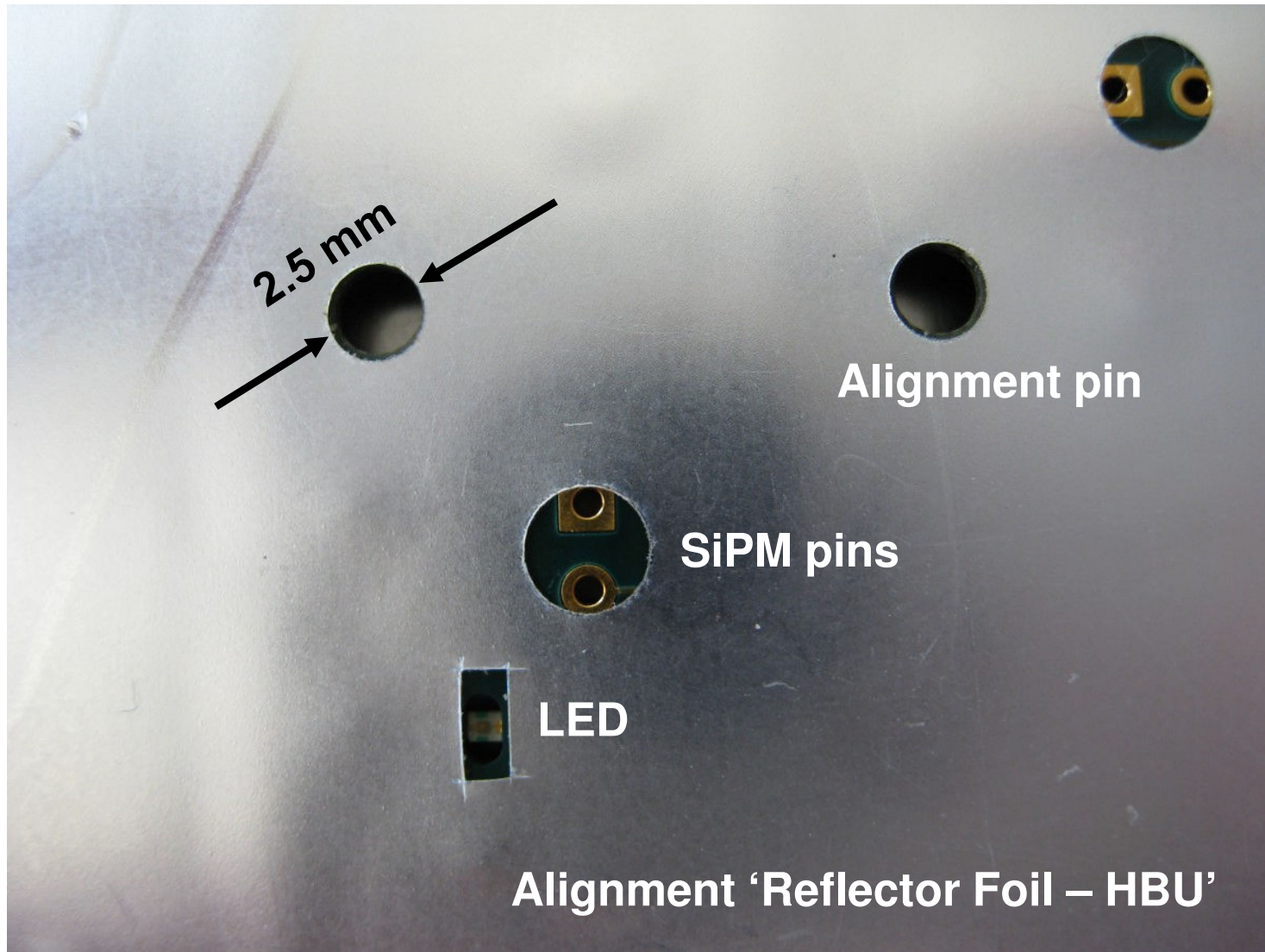
2 setups in operation



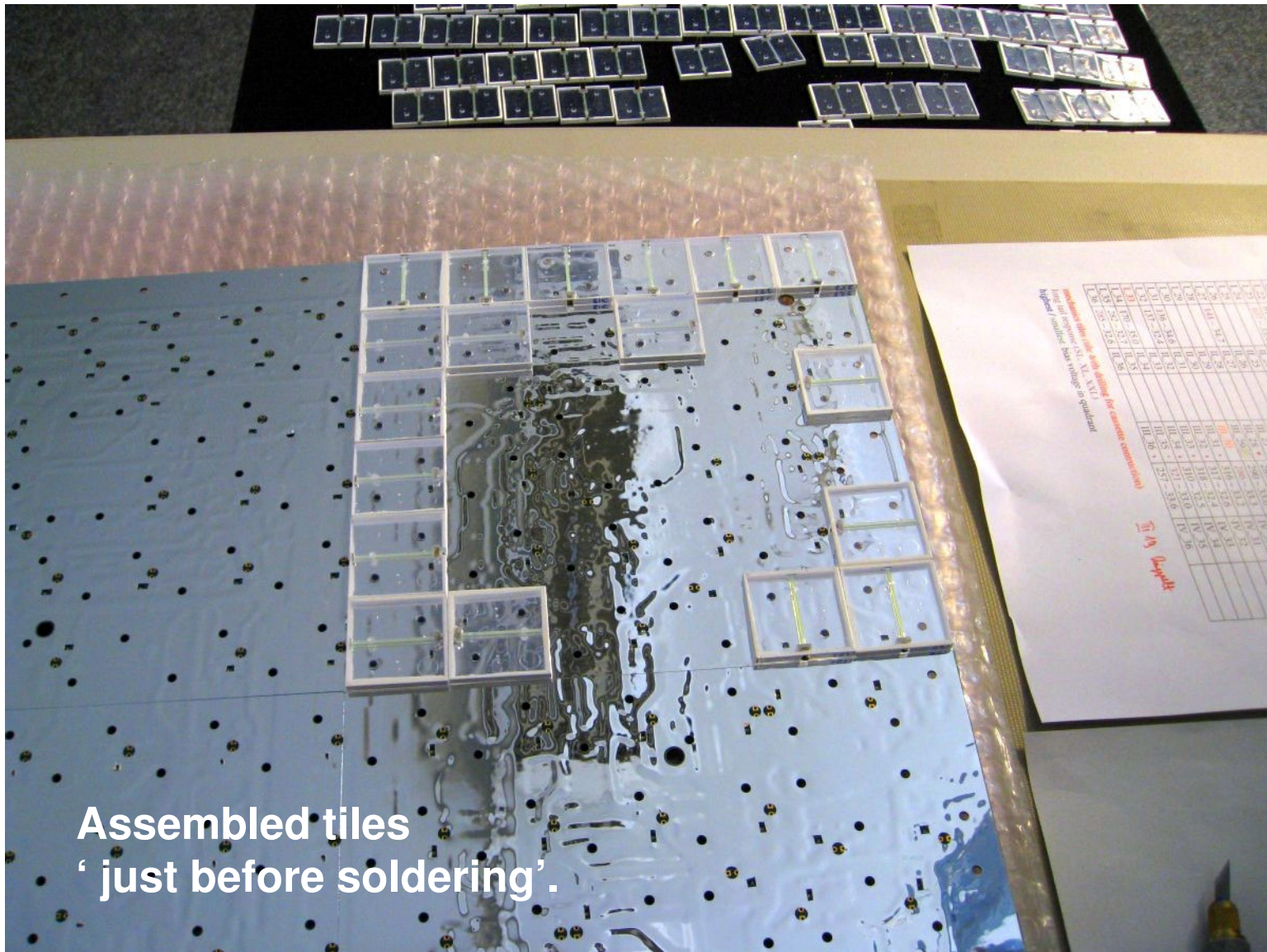
Reflector Foil Assembly



Reflector Foil Assembly



Tile Assembly (the first 18)



Tile Map

Module HBU0_II

file: calibration

II_6	II_5	II_4	II_3	II_2	Pos.	Tile – Bias [V]	Pos.	Tile – Bias [V]	Pos.	Tile – Bias [V]	Pos.	Tile – BiasV [V]
					I_1		II_1		III_1	26 – 33.5	IV_1	152 – 33.1
					I_2		II_2		III_2	33 – 33.3	IV_2	14 – 33.0
II_12	II_11	II_10	II_9	II_8	I_3		II_3		III_3	41 – 33.3	IV_3	55 – 32.8
					I_4		II_4		III_4	43 – 33.6	IV_4	42 – 33.0
					I_5		II_5		III_5	50 – 33.4	IV_5	46 – 32.7
II_18	II_17	II_16	II_15	II_14	I_6		II_6		III_6	81 – 34.0	IV_6	24 – 32.5
					I_7		II_7		III_7	90 – 33.9	IV_7	326 – 33.5
					I_8		II_8		III_8	95 – 33.5	IV_8	88 – 31.9
II_24	II_23	II_22	II_21	II_20	I_9		II_9		III_9	98 – 33.9	IV_9	89 – 33.3
					I_10		II_10		III_10	272 – 33.5	IV_10	248 – 33.0
					I_11		II_11		III_11	133 – 33.8	IV_11	320 – 34.0
II_30	II_29	II_28	II_27	II_26	I_12		II_12		III_12	138 – 33.3	IV_12	314 – 32.2
					I_13		II_13		III_13	147 – 33.8	IV_13	312 – 33.3
					I_14		II_14		III_14	157 – 33.7	IV_14	188 – 33.2
					I_15		II_15		III_15	166 – 33.5	IV_15	193 – 32.8
II_36	II_35	II_34	II_33	II_32	I_16		II_16		III_16	167 – 33.5	IV_16	235 – 33.6
					I_17		II_17		III_17	168 – 33.9	IV_17	200 – 34.1
					I_18		II_18		III_18	173 – 33.6	IV_18	206 – 33.8
IV_1	IV_2	IV_3	IV_4	IV_5	I_19		II_19		III_19	178 – 33.7	IV_19	205 – 32.6
					I_20		II_20		III_20	184 – 33.8	IV_20	207 – 33.1
					I_21		II_21		III_21	249 – 33.8	IV_21	221 – 32.4
IV_7	IV_8	IV_9	IV_10	IV_11	I_22		II_22		III_22	186 – 33.5	IV_22	225 – 32.7
					I_23		II_23		III_23	252 – 33.7	IV_23	242 – 33.2
					I_24		II_24		III_24	264 – 33.6	IV_24	258 – 33.0
					I_25		II_25		III_25	241 – 33.6	IV_25	265 – 32.9
IV_13	IV_14	IV_15	IV_16	IV_17	I_26		II_26		III_26	213 – 33.6	IV_26	305 – 32.3
					I_27		II_27		III_27	227 – 33.7	IV_27	277 – 33.1
					I_28		II_28		III_28	185 – 34.0	IV_28	267 – 32.9
IV_19	IV_20	IV_21	IV_22	IV_23	I_29		II_29		III_29	240 – 33.4	IV_29	313 – 33.1
					I_30		II_30		III_30	208 – 34.0	IV_30	164 – 33.3
					I_31		II_31		III_31	196 – 33.2	IV_31	306 – 33.1
					I_32		II_32		III_32	201 – 33.2	IV_32	307 – 33.1
IV_25	IV_26	IV_27	IV_28	IV_29	I_33		II_33		III_33	194 – 33.3	IV_33	308 – 33.3
					I_34		II_34		III_34	87 – 33.3	IV_34	311 – 32.8
					I_35		II_35		III_35	125 – 33.3	IV_35	315 – 33.0
IV_31	IV_32	IV_33	IV_34	IV_35	I_36		II_36		III_36	181 – 33.3	IV_36	325 – 32.6

Each quadrant can choose between 3 SiPM bias voltages

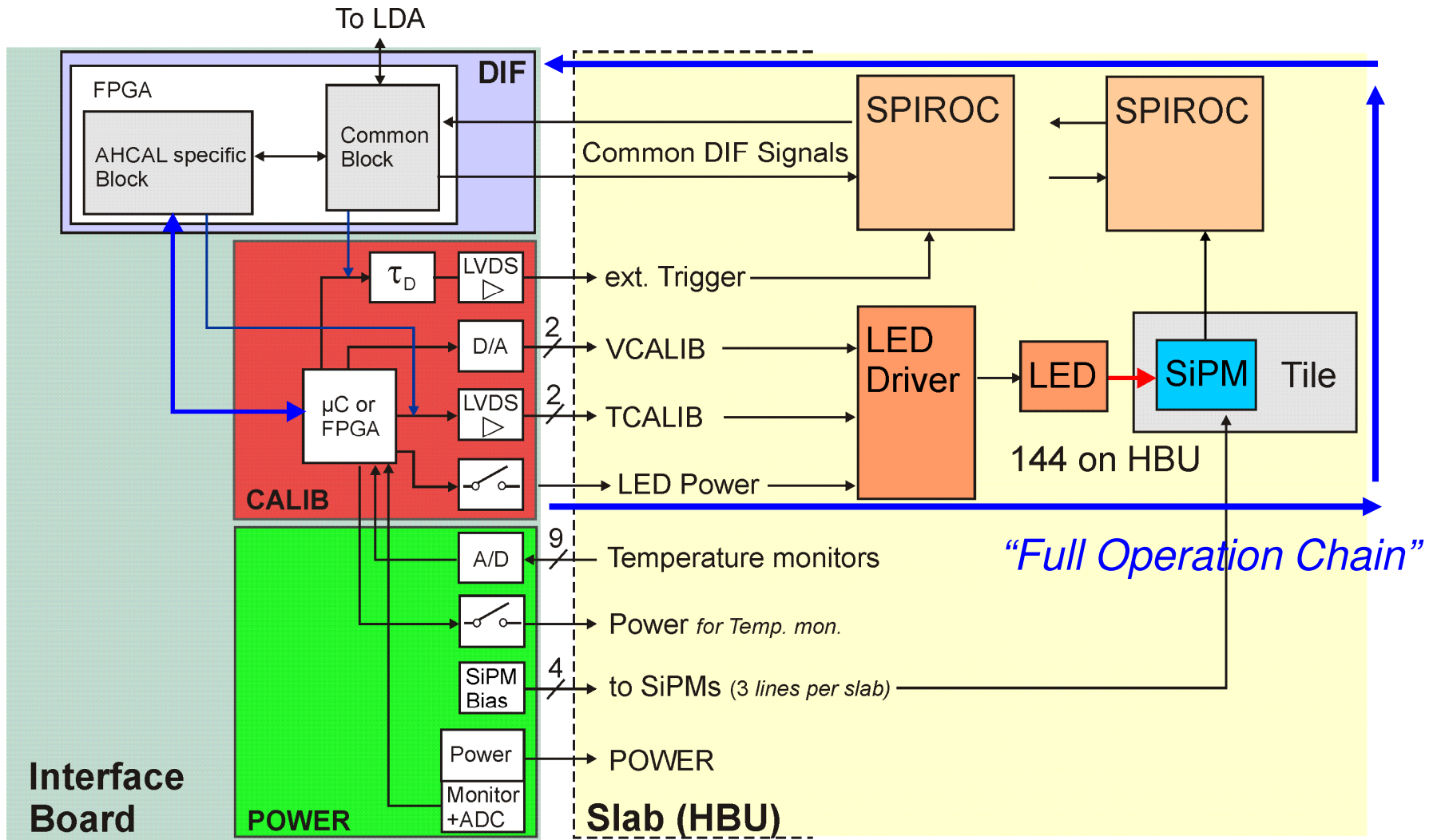
mechanics tiles (tile with drilling for cassette construction)

long tail response (SL, XL, XXL)

highest / smallest bias voltage in quadrant



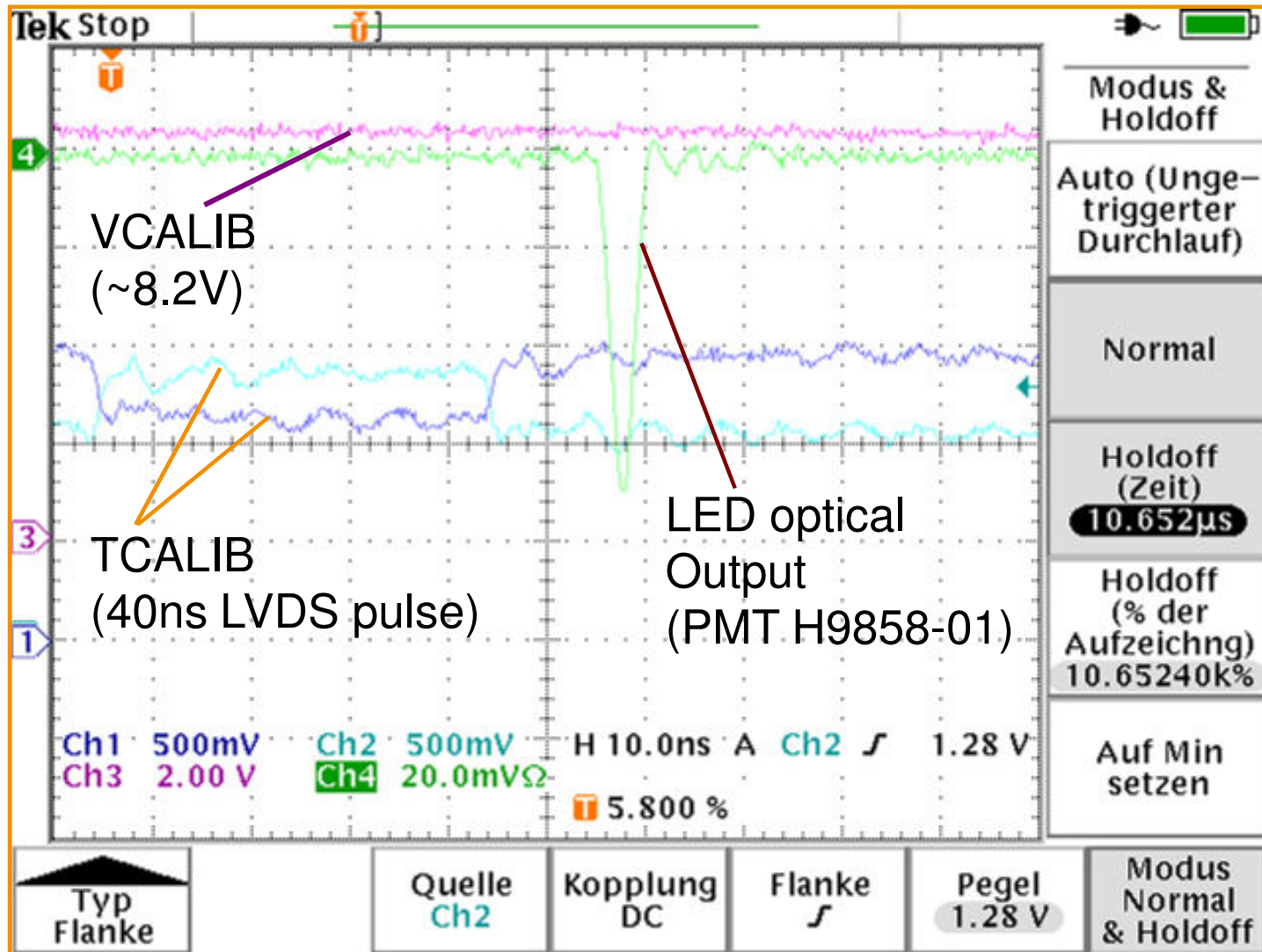
Commissioning – Signal Chain for LED operation



Concept : December 2007



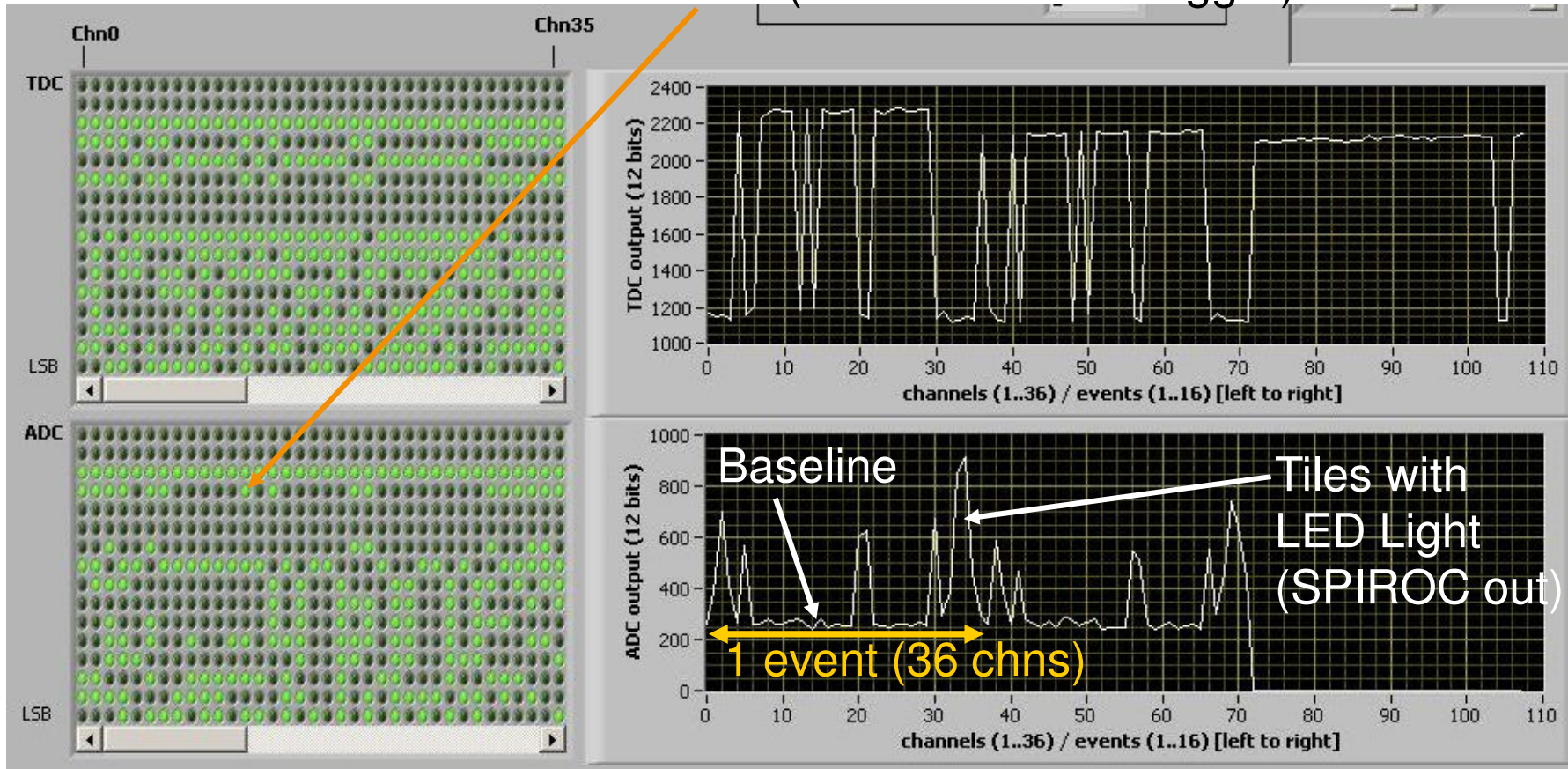
LED Pulse shape (measured on HBU)



Commissioning

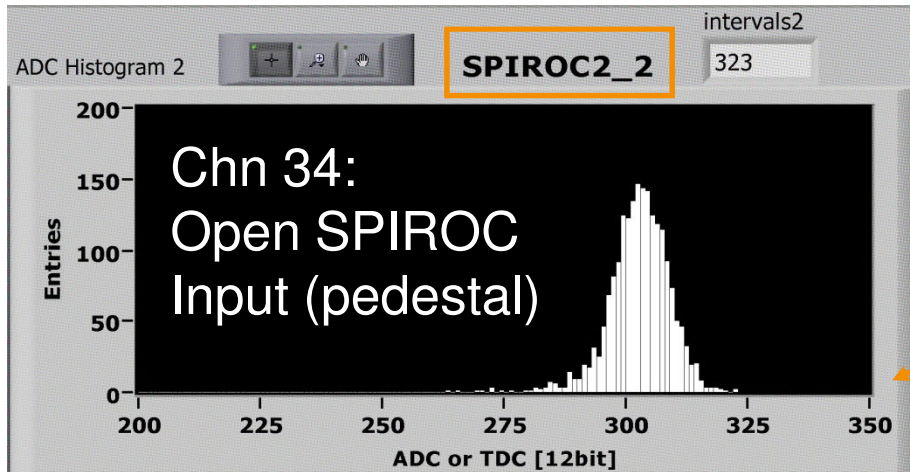
SPIROC2 output: LEDs firing, 3 events (triggers), 18 tiles assembled

Hit Bit (internal channel trigger)

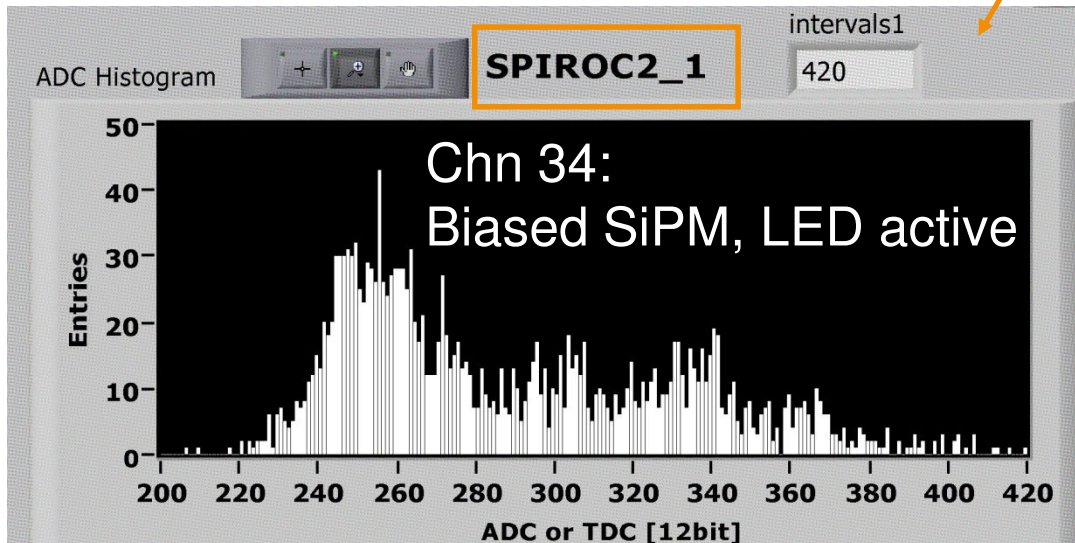


Commissioning (status last Friday)

SPIROC2 output: LEDs firing, 2000 events (trig.), 18 tiles assembled



Labview Software extended to multi-cycle data taking
=> **histograms**



we try to get single peak spectra now to get an idea about global **channel gain** and **noise margin**



Commissioning

Slow Control : Read detector's temperatures, voltages, currents

ADC operation

ADC_Cal
Calibrate

ADC_AVG
Set

No. Avgs
1..255

Read

No. Avgs (hex)

R_ADC1	R_ADC2	R_ADC3	R_ADC4
<input type="button" value="Read"/> <input type="button" value="Set"/>	<input type="button" value="Read"/> <input type="button" value="Set"/>	<input type="button" value="Read"/> <input type="button" value="Set"/>	<input type="button" value="Read"/> <input type="button" value="Set"/>
Temp1 20,86	VCALIB1 0	VDAC 4,943	HV1 4,767
Temp2 20,86	VCALIB2 0,002	IDAC 12	HI1 0
Temp3 20,41	VDDD 3,302	VREF 3,383	HV2 4,751
Temp4 20,38	IDDD 4	IREF 0	HI2 0
Temp5 20,68	VDDA 3,302	VADCREf 0,065	HV3 4,459
Temp6 20,65	IDDA 125	reserved 68	HI3 5
reserved 27,04	reserved 27,04	reserved 69	reserved 252
VADCREf 2,497	VADCREf 2,497	VADCREf 2,497	VADCREf 2,497

voltages in V
currents in mA
temperatures in degrees C

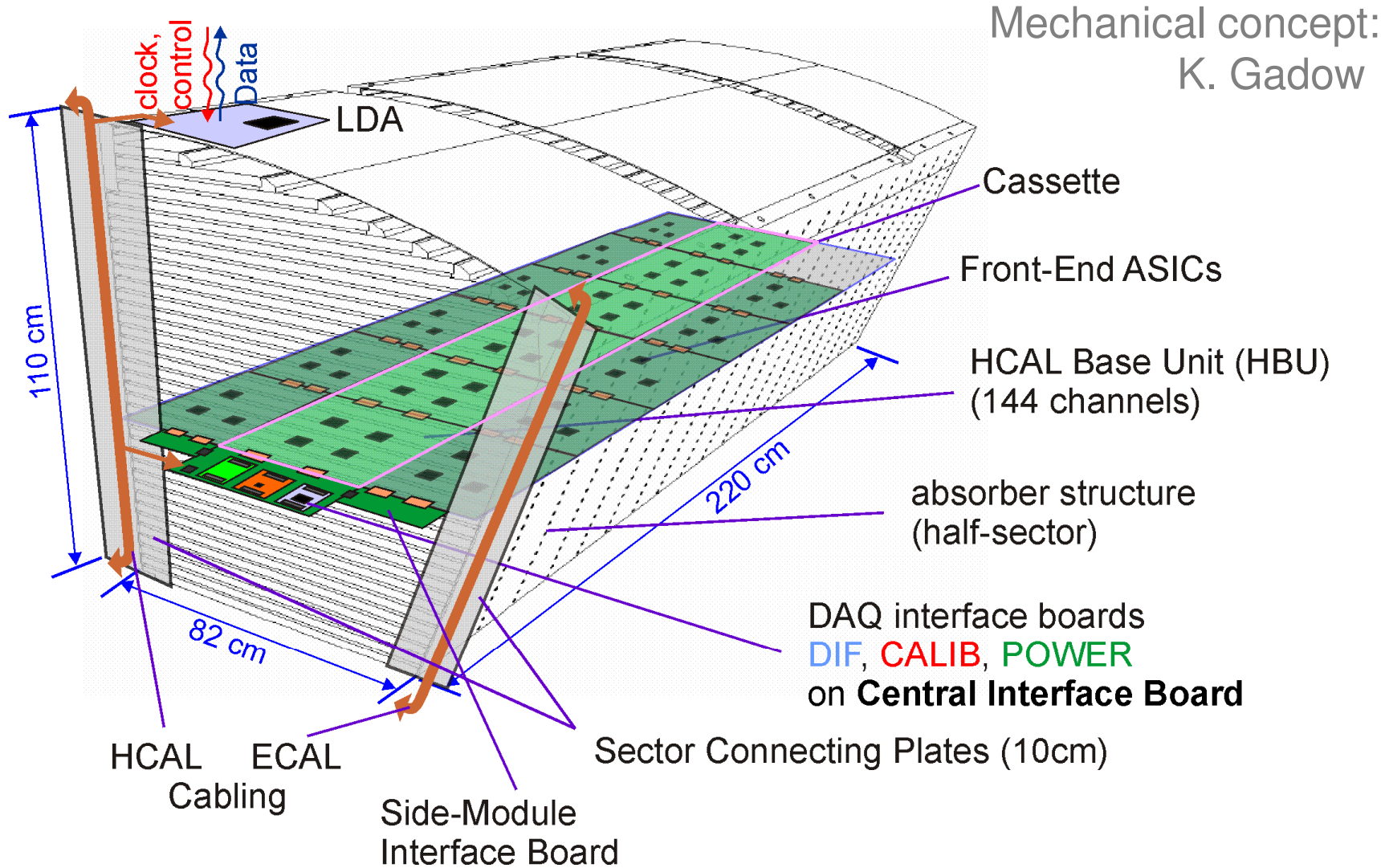
HBU temperature profile

VDDA, VDDD and currents

**Slow-Control:
Still under test**



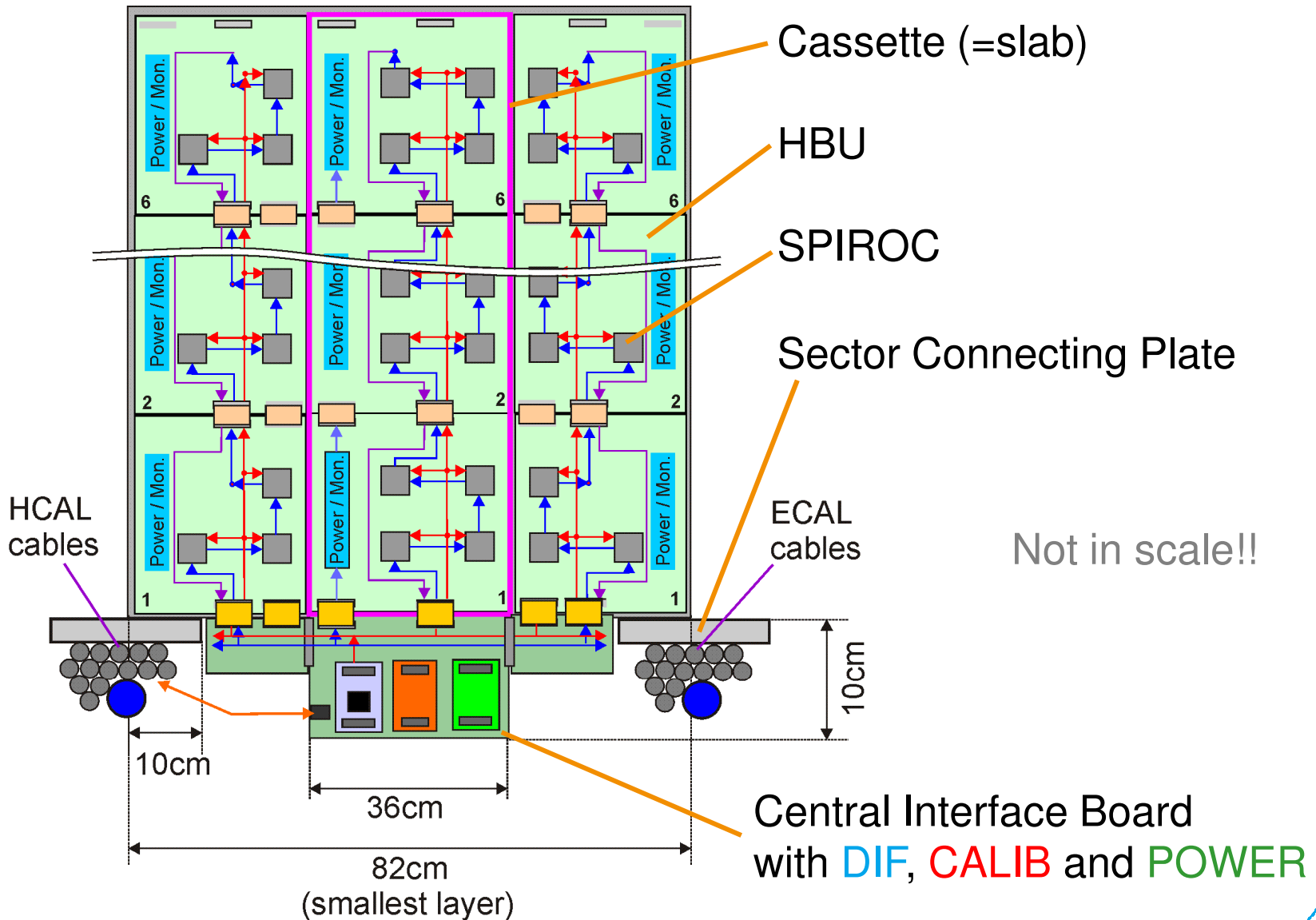
The Next Generation ('final' ILC setup concept)



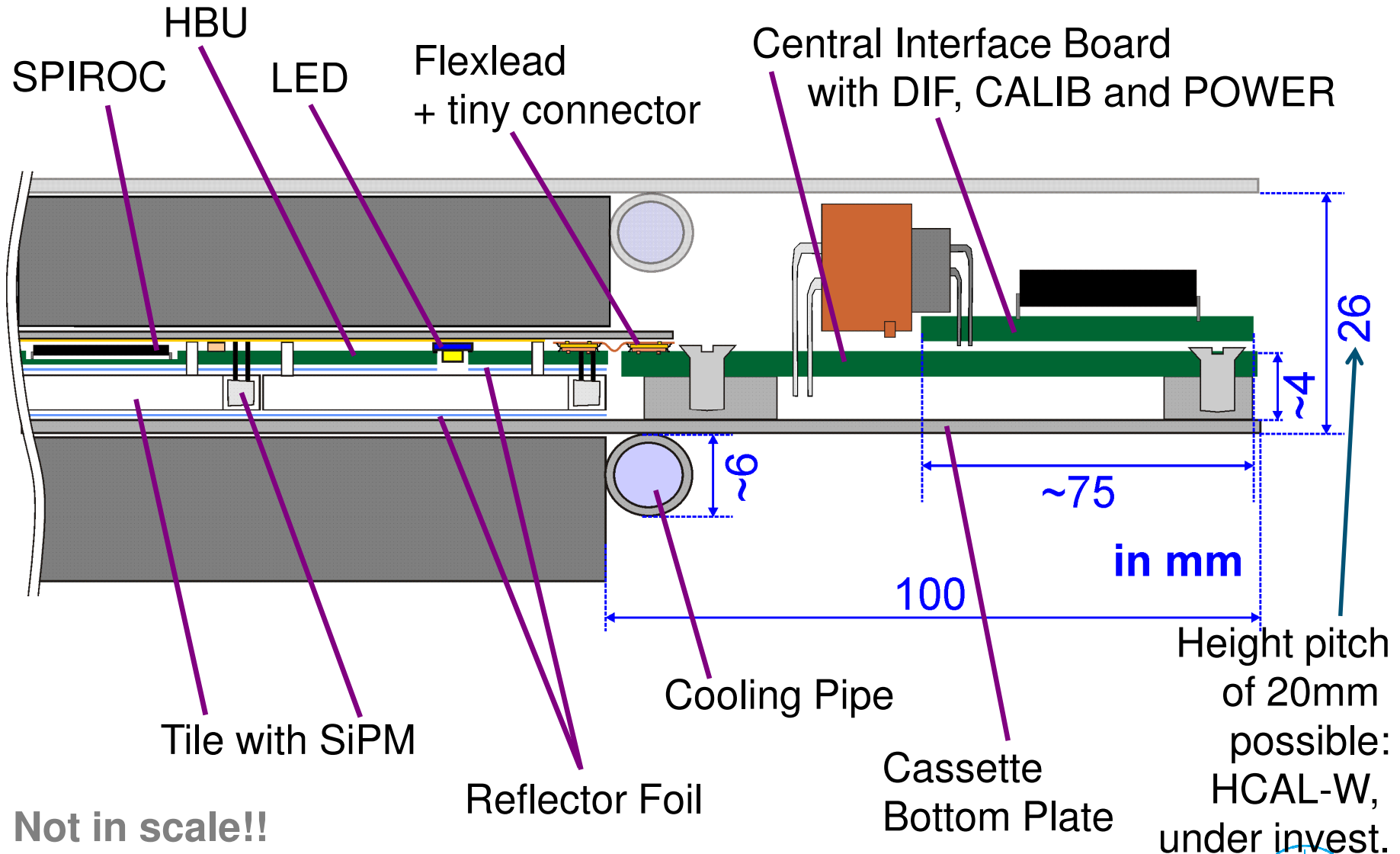
Not in scale!



The Next Generation



The Next Generation



Not in scale!!



Conclusions and Outlook

- > AHCAL prototype delivers first test-data from LED system.
- > British DAQ (hardware, DIF firmware) still has to be implemented.
- > Full equipment of HBUs with tiles very soon now.
- > DESY electron-testbeam preparation:
 - => S. Christen: Labview extension for testbeam
 - => small hardware changes (e.g. ext. trigger)
 - => lab characterization of HBU (incl. LED system)
- > Redesign concepts of AHCAL modules are prepared now.

- > A lot of system's and SPIROC analogue and digital tests ahead.

