Standalone Silicon Test Infrastructure and Transnational Aspects

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Outline

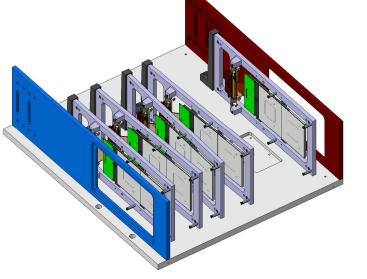
- The Silicon Infrastructure components:
 - => The Silicon Modules and Silicon prototypes
 - => The Faraday & cooling cage
 - => The 3D Table
 - => The alignment system
 - => The FE readout chips
 - => The DAQ system
- The applications
- The transnational aspects

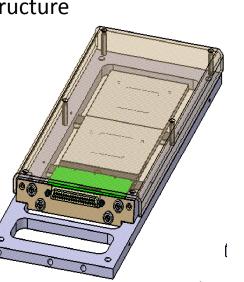
Construction of the Silicon modules/prototypes Design of the modules

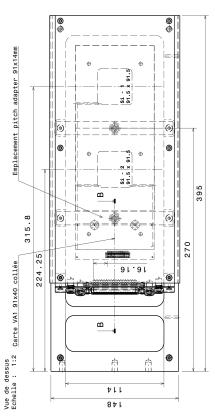
- Modules are made of two sensors bonded to each other (bonding performed at CERN bonding Lab)
- •Flexibility wrt the FE chip (hybrid board can be replaced)
- All kinds of sensor types can be included in this structure
- Special case are the alignment friendly modules (laser IR integrated

in the system

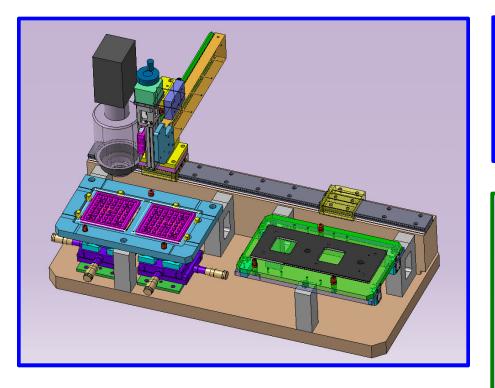
- Tests with radioactive source is integrated as wel
- Easy to manipulate -> robust support structure







Construction of the modules

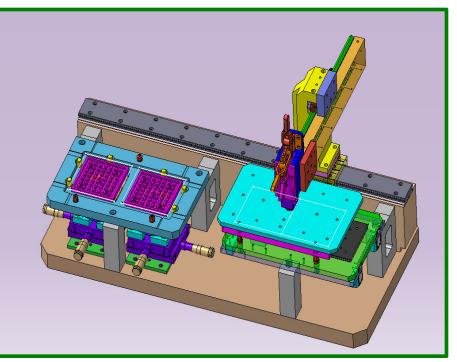


Gluing tool

Preserving the alignment Integration of sensors on Carbone support structure

Alignment tool

Alignment of high precision between the various components of the module : Si sensors, pitch adaptor, FE hybrid board



Installation of a clean room dedicated to the cosntruction of modules

- Alignment of Si microstrips between the two sensors
- Preparation of the support structure
- Gluing of the sensors
- Alignment & gluing of the pitch adaptor and FE hybrid board



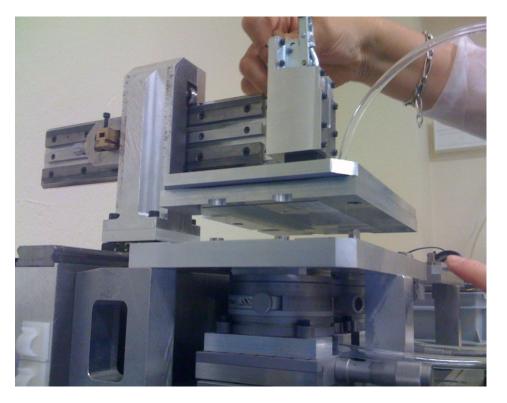
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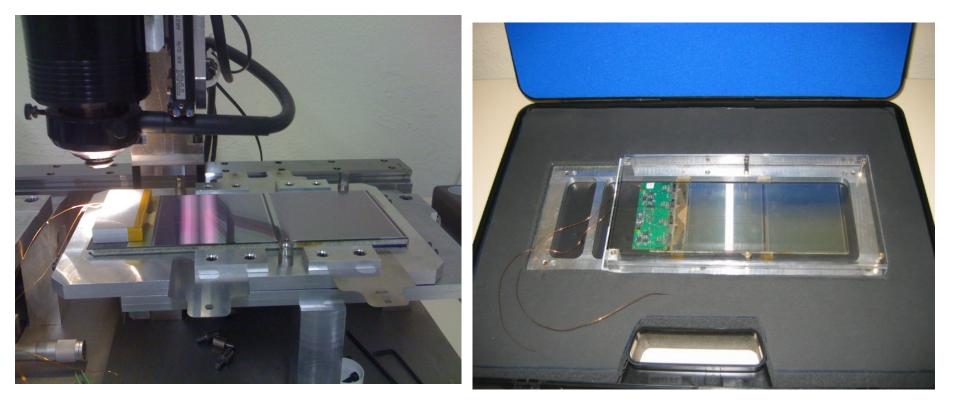
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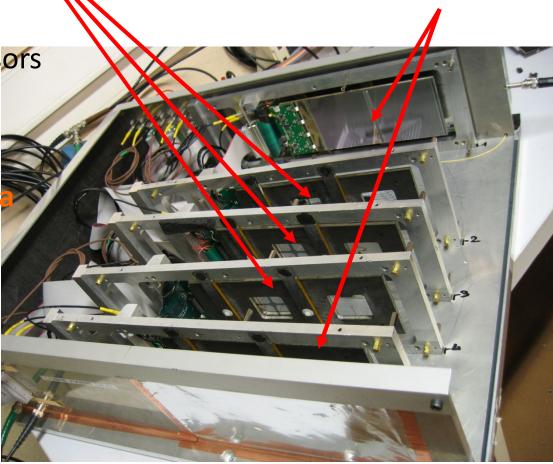


The new Faraday and cooling cage



Inside the Faraday cage

- 3 modules with friendly aligned HPK sensors
- Surrounded with 2 non AL treated HPK sensors
- Electronics from VA1[®]
 - 512 ch per sensor,
 - 25.4 mm active are

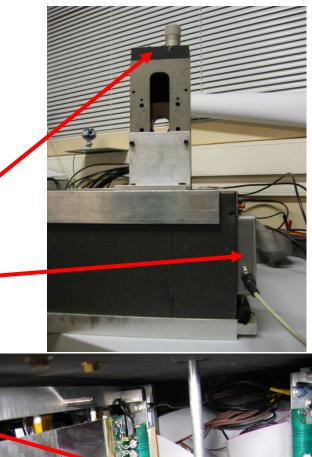


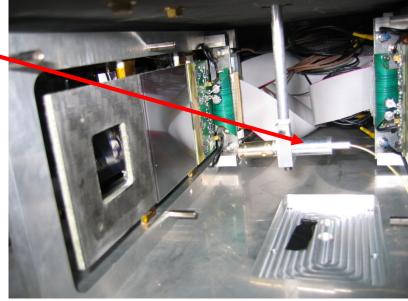
Integrated laser beam

adjustment of the position from outside

Laser diode and its command

Fiber and collimator





The 3D Table for test beam at CERN



The FE readout chips

The present test infrastructure is adapted to:

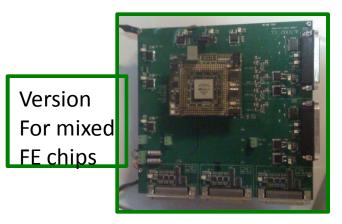
- \Rightarrow VA1 chips as reference readout chips
- \Rightarrow The new SiTR_130 chips (see TH Pham presentation)
- A complete DAQ framework has been developed able to handle both FE readouts The VA1 and SiTR_130 chips are dra asstically different.
- The VA1' is a commercial device from IDEA that only performed the very front end processing (Low noise preamplifier plus long shaping time in the currently used version)
- The SiTR_130 chip instead perform the whole processing of the signal including pulse-height reconstruction and digitization. In the new version under development it will include a full digital processing in addition.

Two FE hybrid boards have been designed and built for each of these ASICs as well as two different FPGA systems.

The global Si DAQ both on the hardware and software sides is able to handle both systems (flexibility)

The related DAQ system: Hardware part

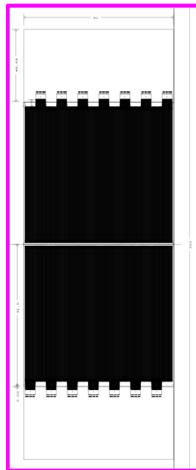
- The number of channels to read out is growing
 - Alignment tests (2009)=> 2560 channels
 - Combined calo tests (mid-2010) => 15000 à 20000 ch
 - 2011-2012 -> much more !!!
- DAQ hardware "Kit", evolutive system
 - VA1 (VFE reference), SiTR_130 and new prototypes, mixed mode FE (Ref+SiTR_130)
 - XILINX modules: Altera/USB (currently available → Altera/(Ethernet, USBx)? Under development

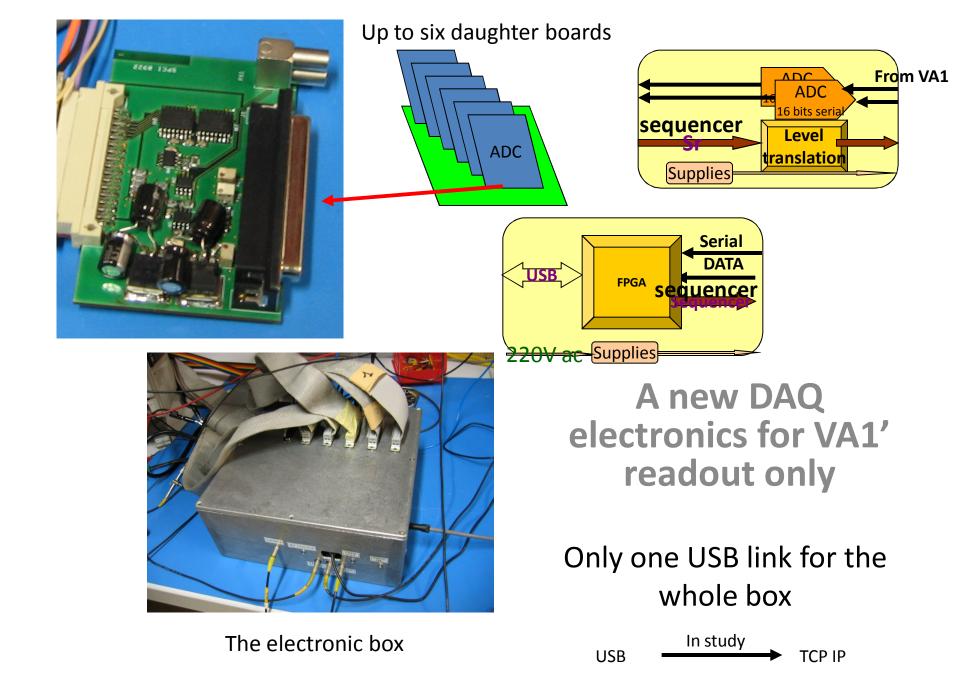


FPGA system for VA1 only



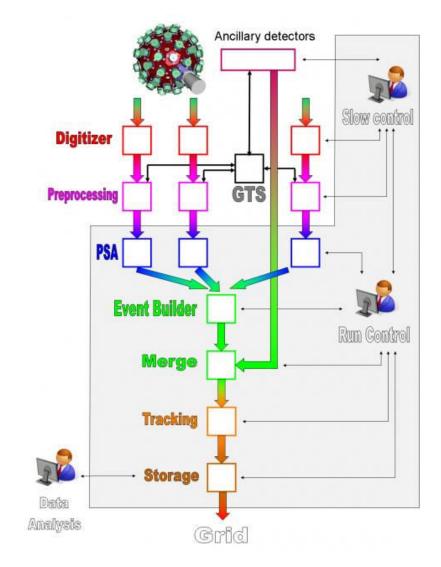
Redesign of the module for the new SiTR 130-128





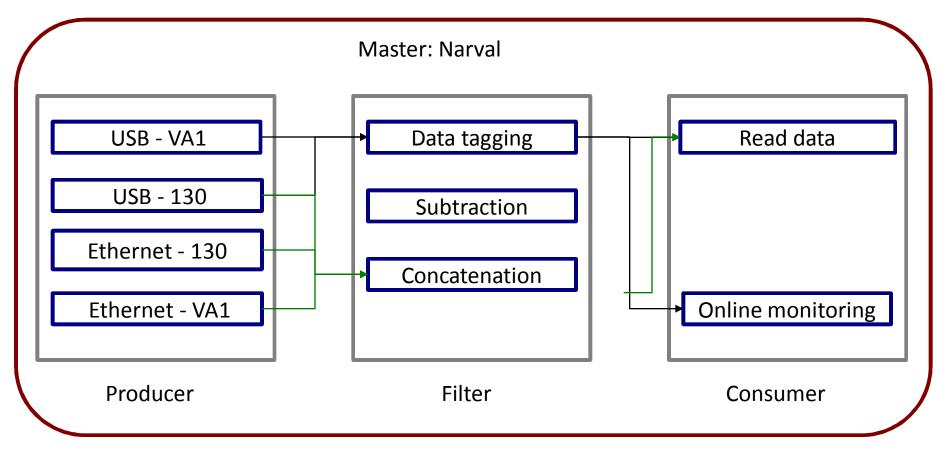
A new DAQ Software: VHDL, C++, ROOT based

- « Narval » C-oriented is the main frame
- Can be interfaced with any other DAQ
- The FPGA system is handled by a full
 VHDL software
 package.



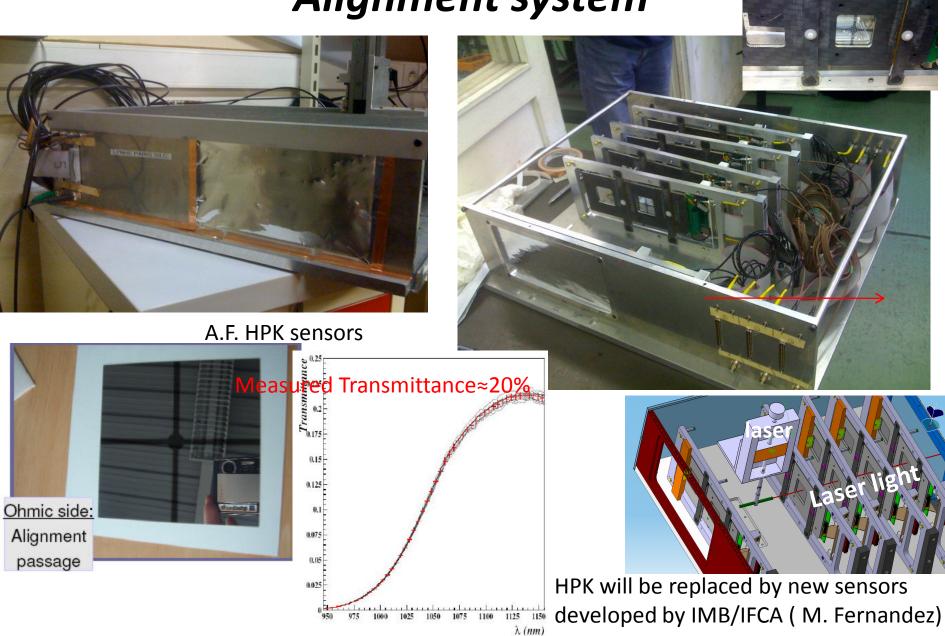
DAQ software: main frame

• Flow diagram of the DAQ with Narval main frame:



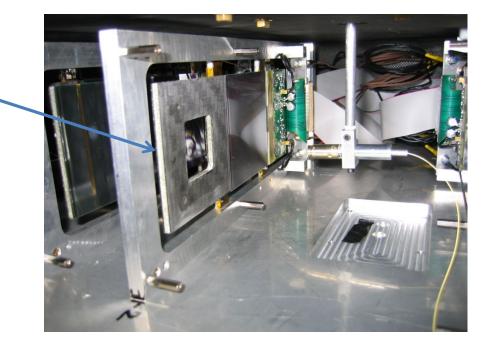
Can be easily connected to any global DAQ software

Alignment system



Applications of this test infrastructure

- Tests of the friendly aligned HPK sensors
 - With a laser beam embedded
- Tests of other sensors types (new strip technology, new pixel devices)
- Tests of new FE electronics
- Combined tests with other sub-detector prototypes
 => new such infrastructure are developed and adapted to those tests

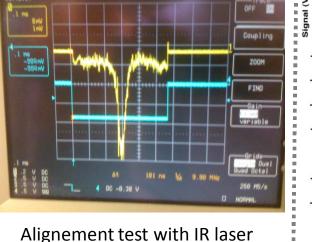


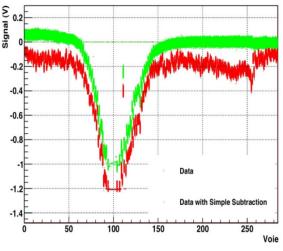
Applications of the Si test infrastructure

HPK long strips SPS West area 10-22/10/2007 Tests of SiTr130-4 reading new Combined test with EUDET telescope **HPK** sensors Signal : Chip 1- Strip 3 Entries 11933 Entries 17033 Mean -1.01482 Nean 0.03561 RVA 3 (6613 RN8 and the short have been Number of counts - Inc - 1062 . -0.6 -0.4 -0.2 0 0.2 0.4 0.6 Signal Estimator 0.8



Tests of alignment system based on AF HPK sensors





S/N = 23 with 18.3cm

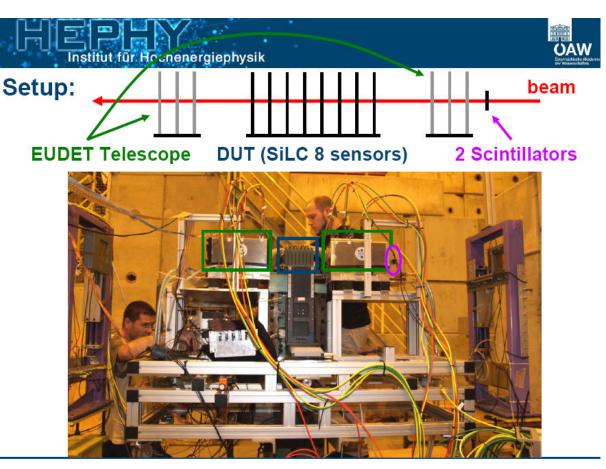
1.718

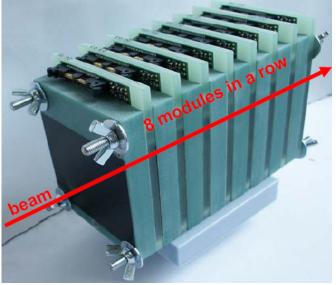
End 2009: beam tests at CERN & laser at IFCA Santander

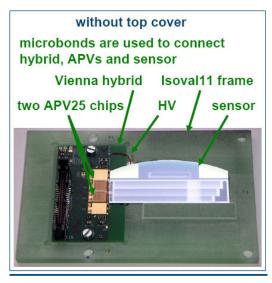
Transnational Aspects

- Tests of the current alignment system with with the IR laser (Santander laser test bench) and at SPS test beam still in 2009, conducted by the *Torino team*
- 2- Tests of new sensor technologies conducted by *HEPHY-Vienna* at CERN SPS (15-30 August 2009) (see Th.Bergauer's presentation). Will be pursued next year.
- 3 Combined tests with calorimetry: dual readout test beam at CERN (2010), conducted by italian teams (*Pisa*)
- 4- Tests of new sensor technologies: tests of news sensors including new pixel technologies from *IRST, VTT* (in preparation for 2010): modules will be made at LPNHE&CERN and will be included in the present standalone test infrastructure.

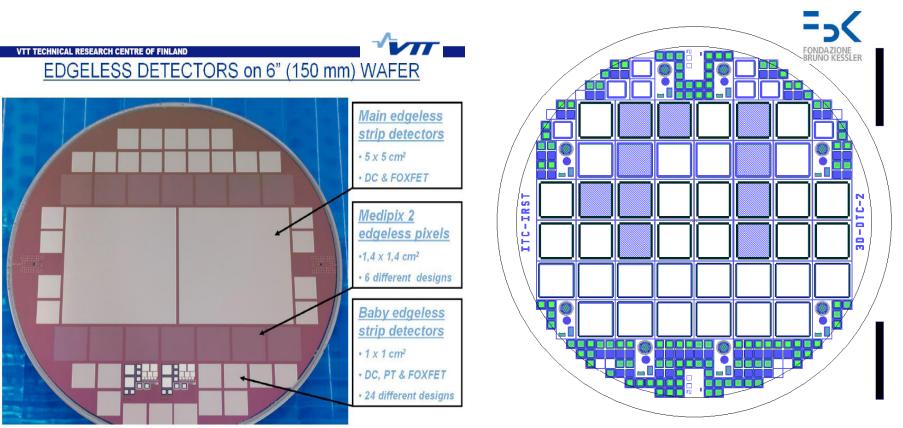
HEPHY tests infrastructure studies: direct application for Superbelle strip detector







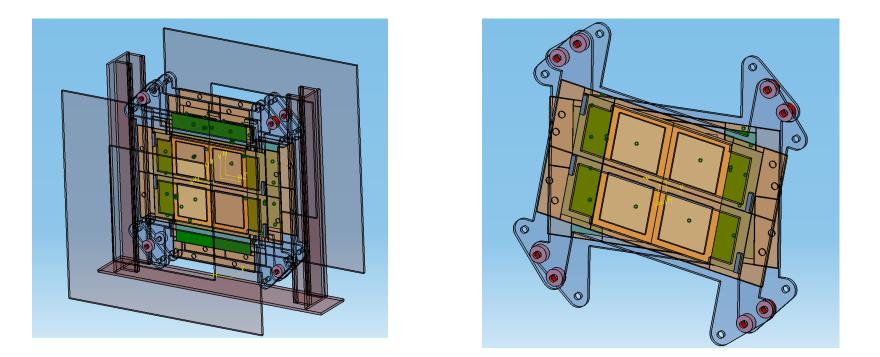
Using standalone structure to test new sensor technologies



Modules are going to being designed at LPNHE to host various types of new sensor Strip prototypes: new edgeless strip sensors (left) with 5x5cm2 sensors; new short Strip sensors (right) 1.5x1.5 cm2, in 3D technology amd planar edgeless strip sensors 2.5x5cm2 prototypes

Construction of new larger modules for combined test beam with calorimetry

Under preparation for next year first for CALICE (can be adapted to other calorimetry tests Surface to be covered: 18x18cm2 in 2010 tests=> first 2 false double sided modules are built



Design allows to study various coupling angles between the single sided modules (XUV or small angle tilted modules for false double sided case)

Concluding remarks

- An expertise has been developed within the SiLC collaboration that has been exploited in the EUDET project to develop the full Silicon test infrastructures.
- It includes: construction of prototypes, design of new FE electronics (based on ref. Chips and new chips), development of the associated DAQ (hardware & software), cooling-Faraday cage and 3D Table, plus a full alignment system based on IR laser system.
- Transnational based applications of these various infrastructures are occuring in 2009 (2) and at least 2 other before the completion of the programme in 2010.
- The development of these infrastructure will be instrumental for the launching of the (hopefully) next EU I3-FP7 project; it will be used to built the Silicon tracking system to be coupled to calorimetry and eventually also the TPC gaseous prototype.