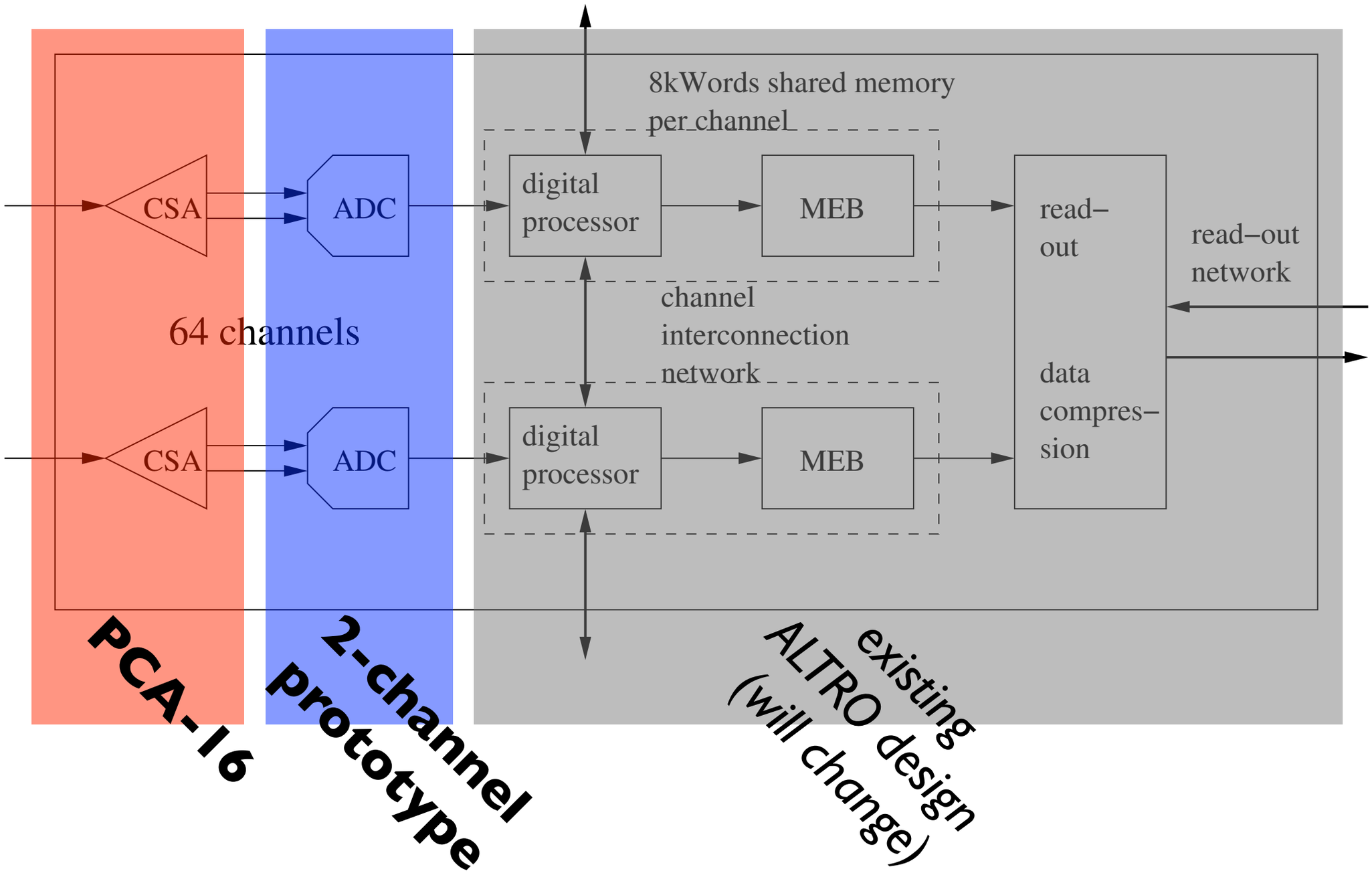
S-ALTRO

integration and system level studies

Outline

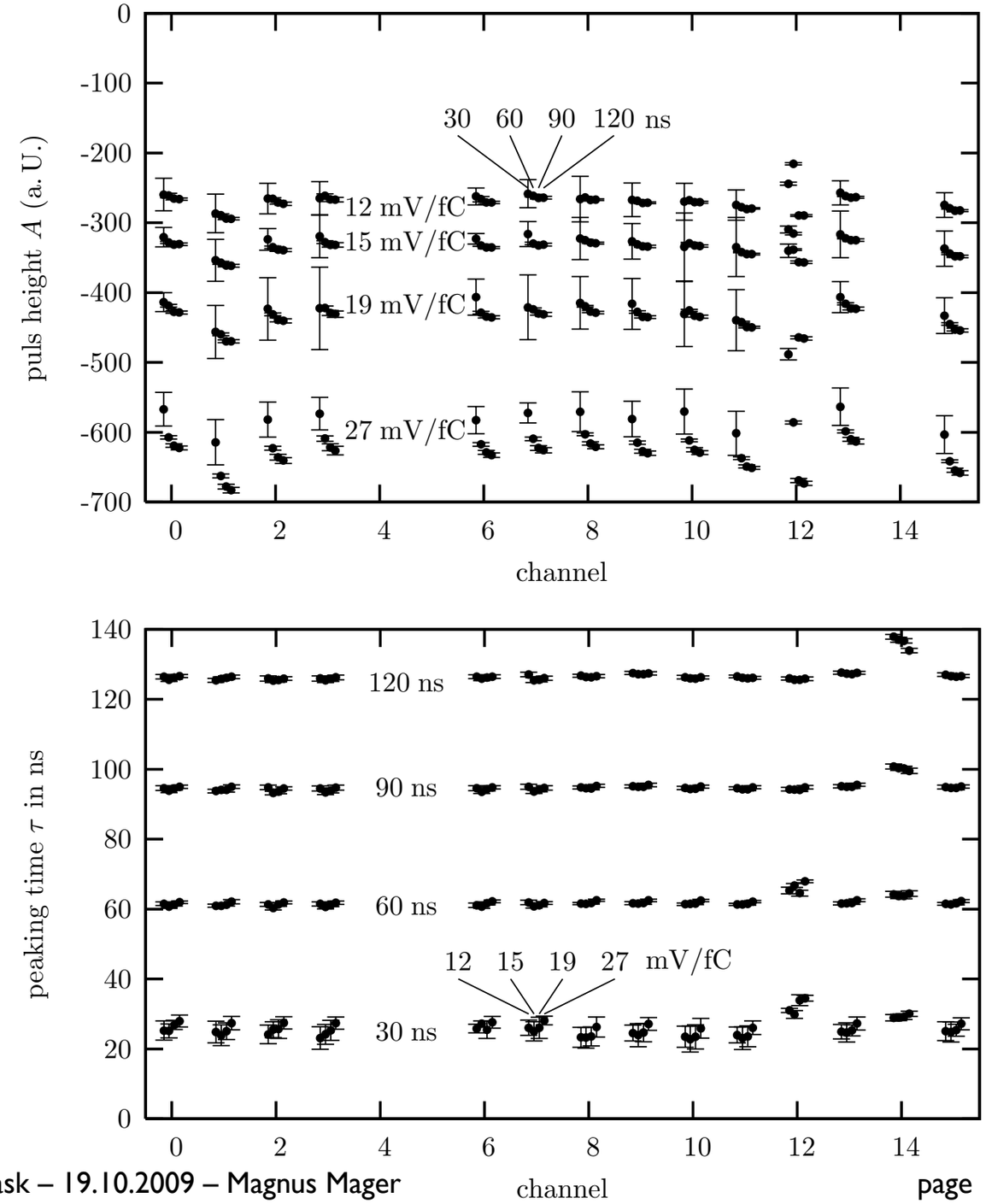
- status of S-ALTRO development – short summary
  (see Paul's talk in "Special session on microelectronics developments within EUDET (NA2)" for details)
- Read-out backplane studies
- Plans/Outlook

S-ALTRO design – current status

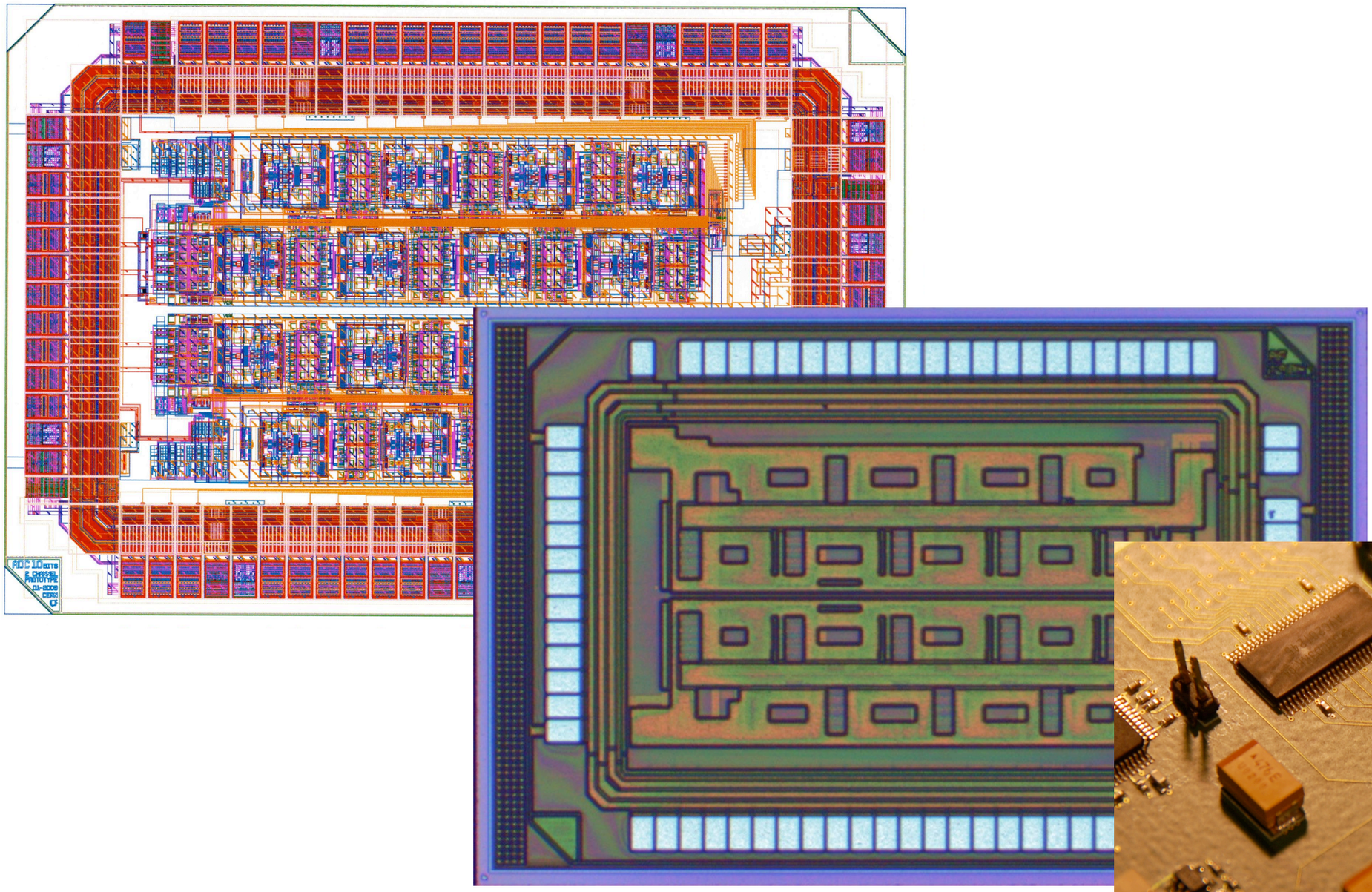


PCA-16

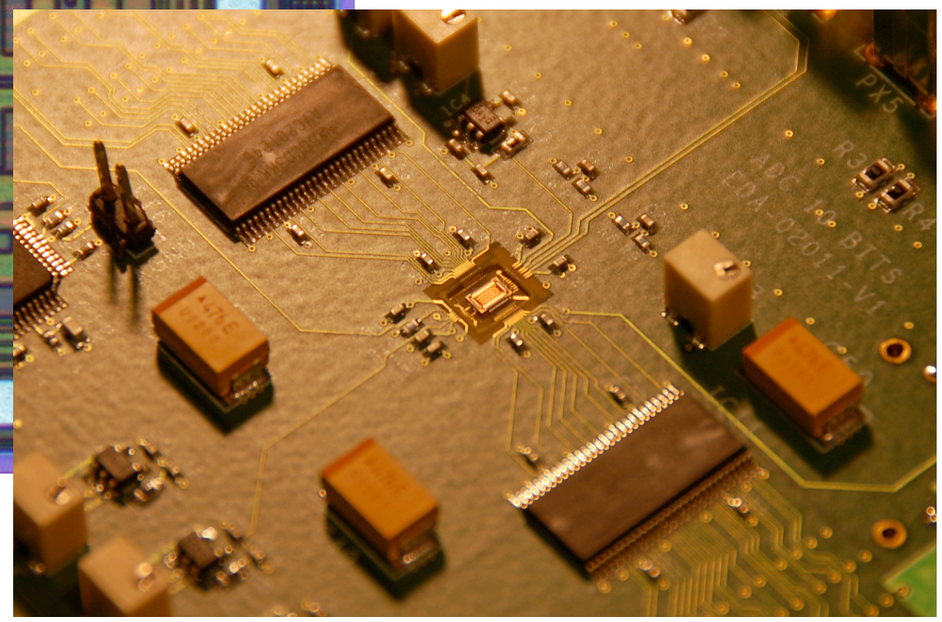
- CMOS 130 nm
- 0.2 mm^2/channel
- < 8 mW/channel
  - <1mW in standby
- works according specifications
- is already in use (e.g. at DESY)



ADC prototype

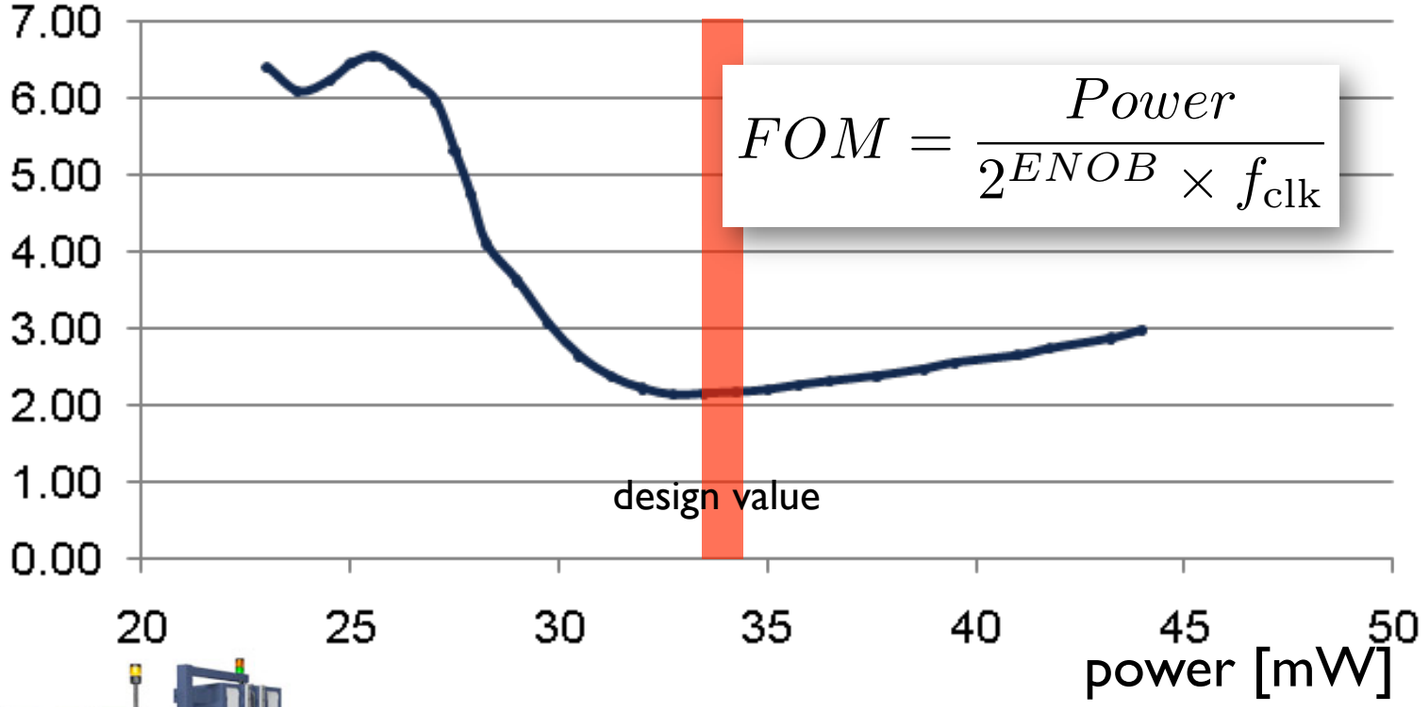


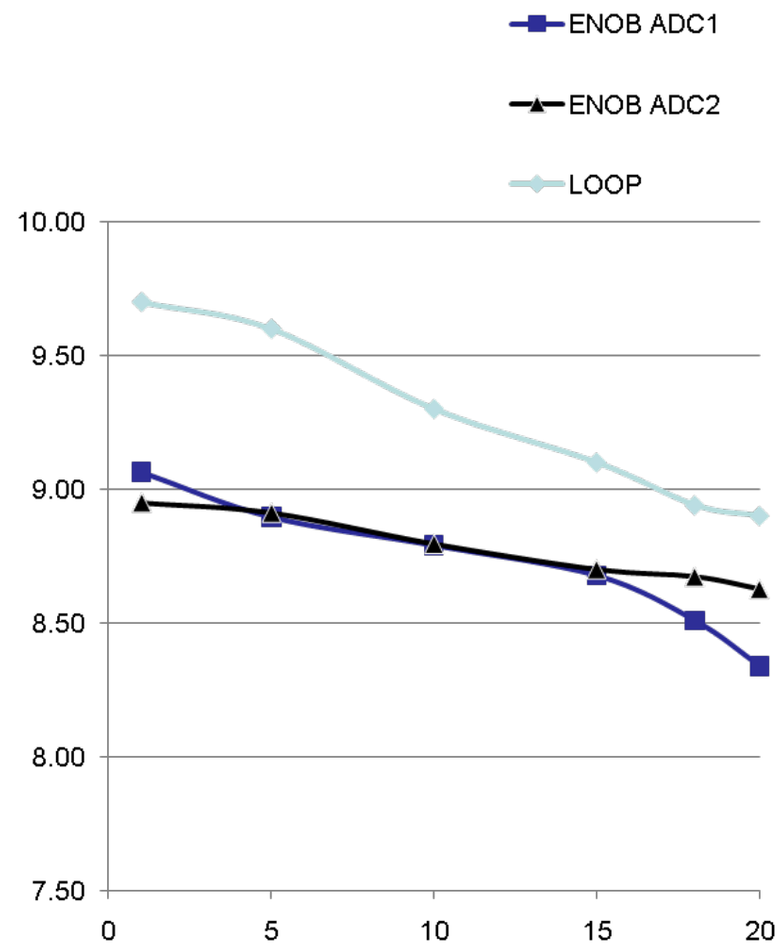
courtesy of Hugo França Santos



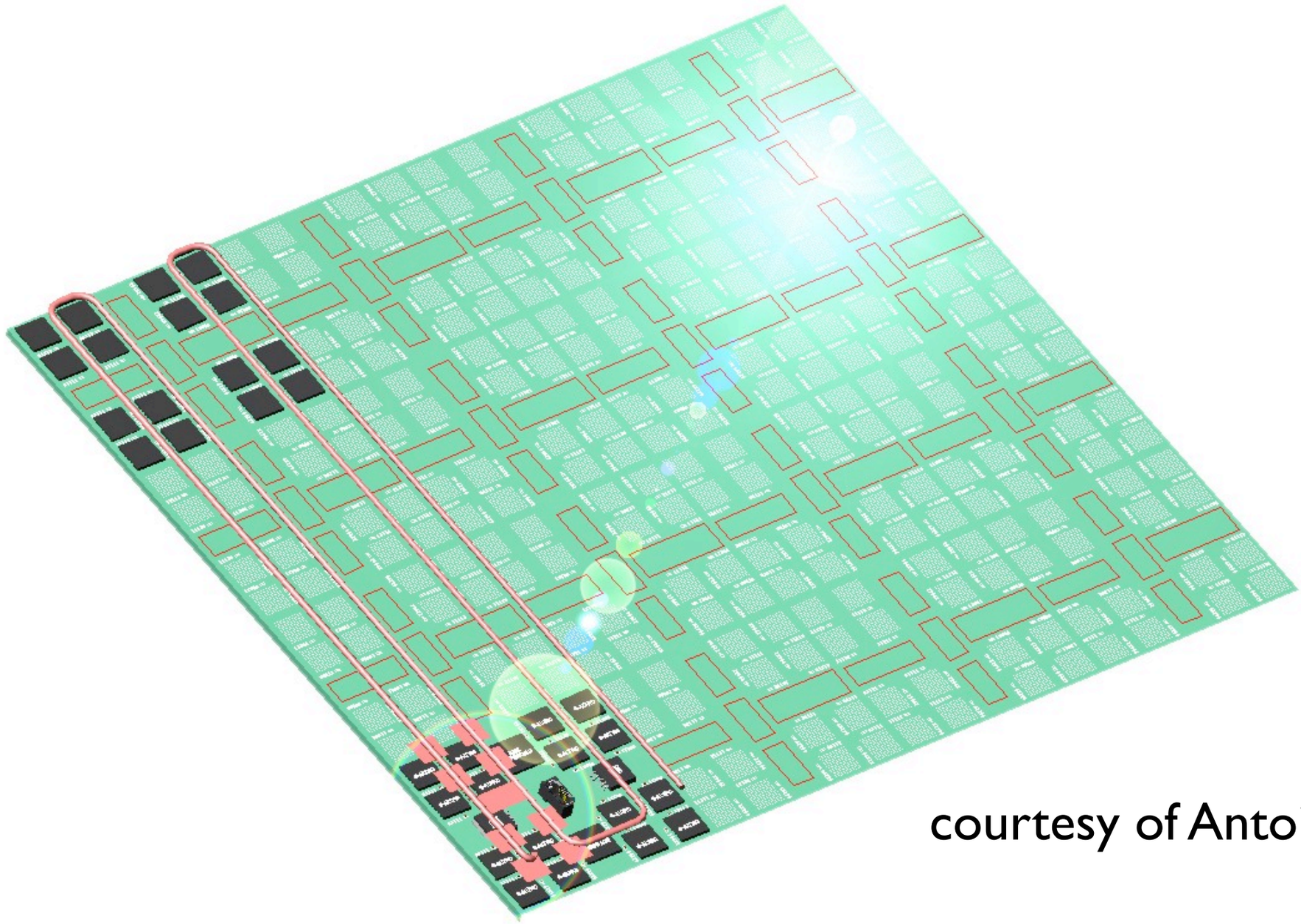
Single ADC area: 1.57 X 0.45 = 0.7 mm² **Prototype area: 2.35 X 1.6 = 3.76 mm²**

ADC prototype – test



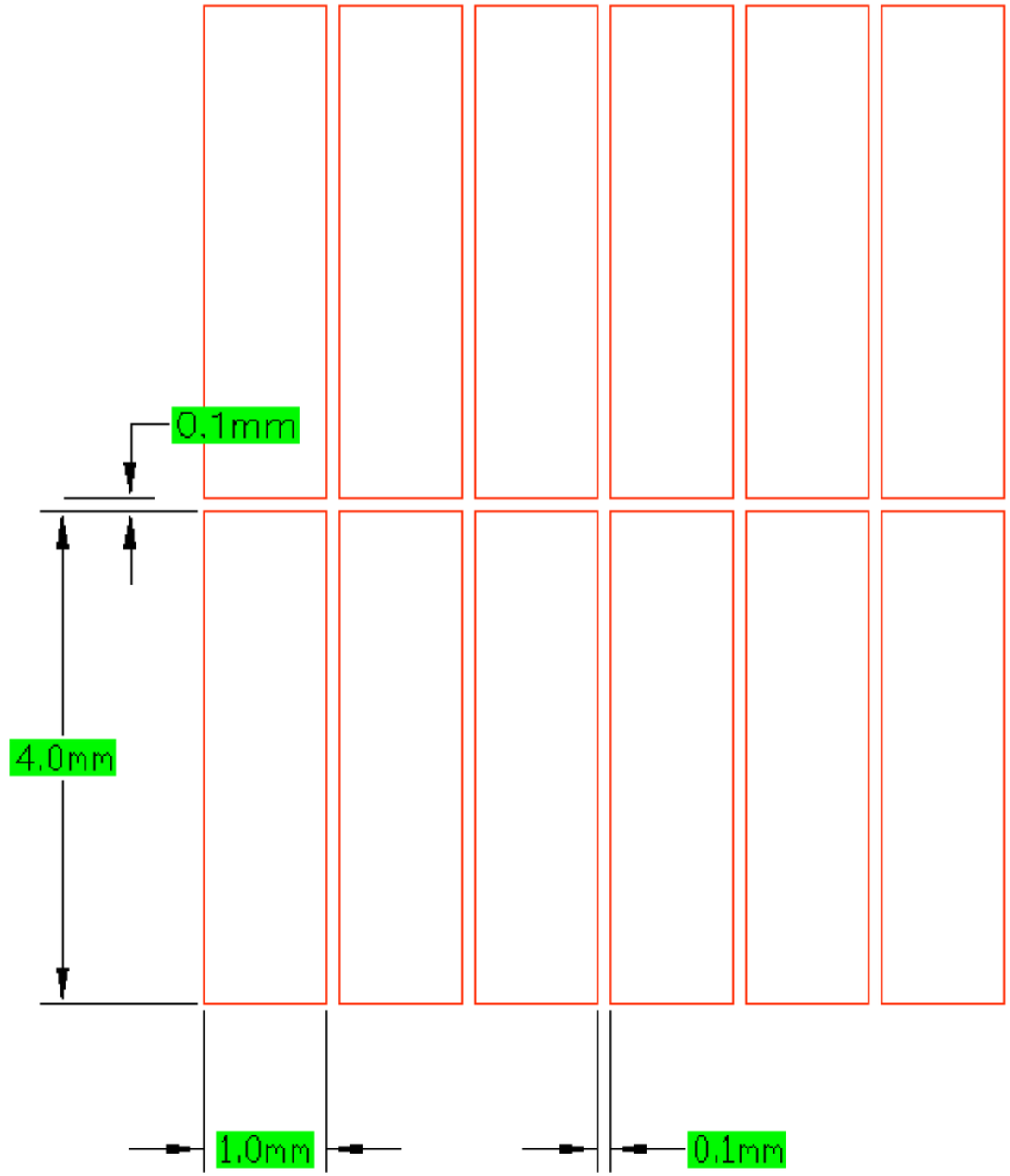


Read-out backplane

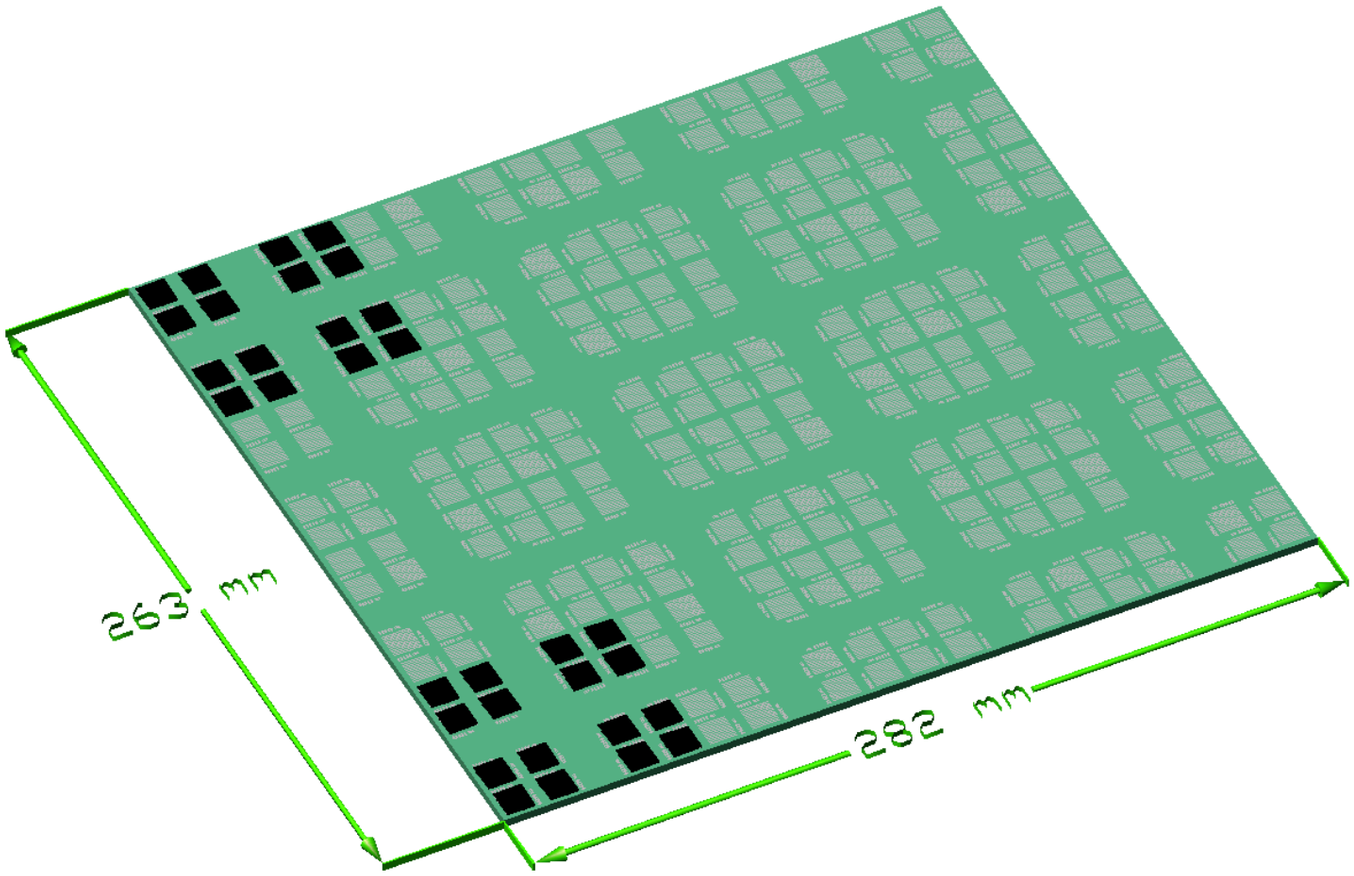


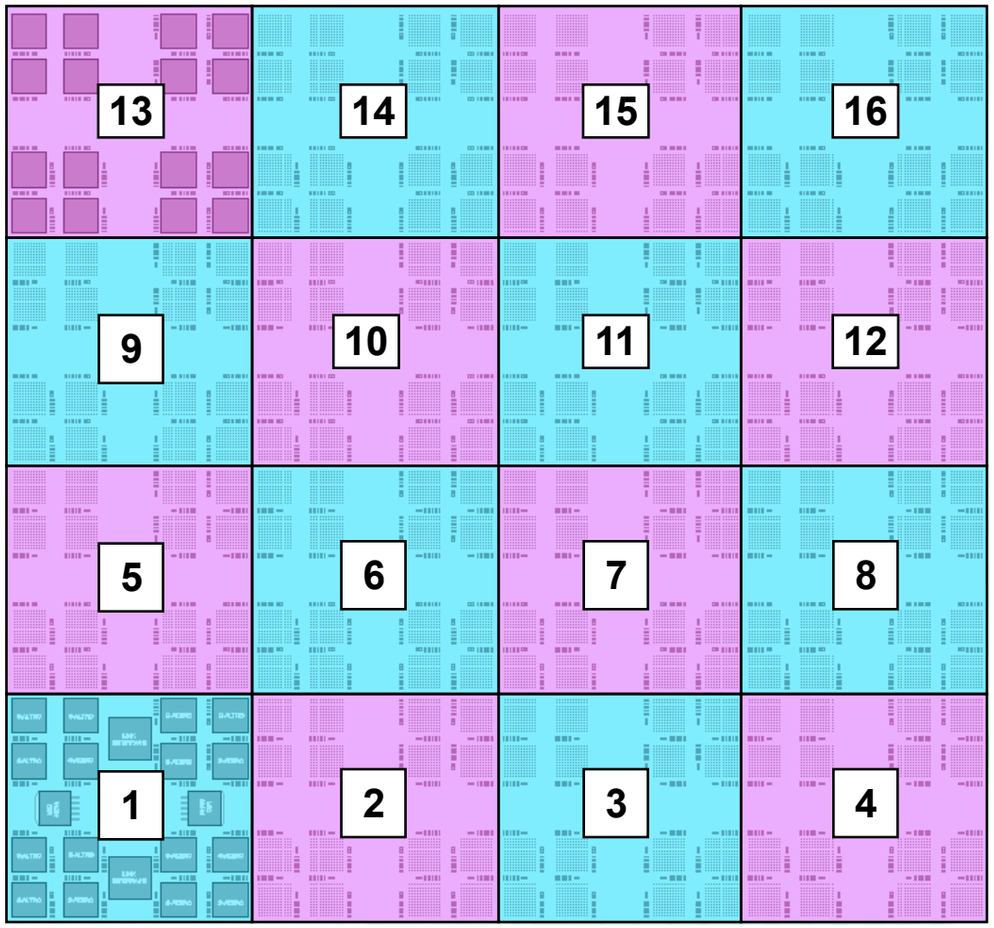
courtesy of Antoine Junique

Pads

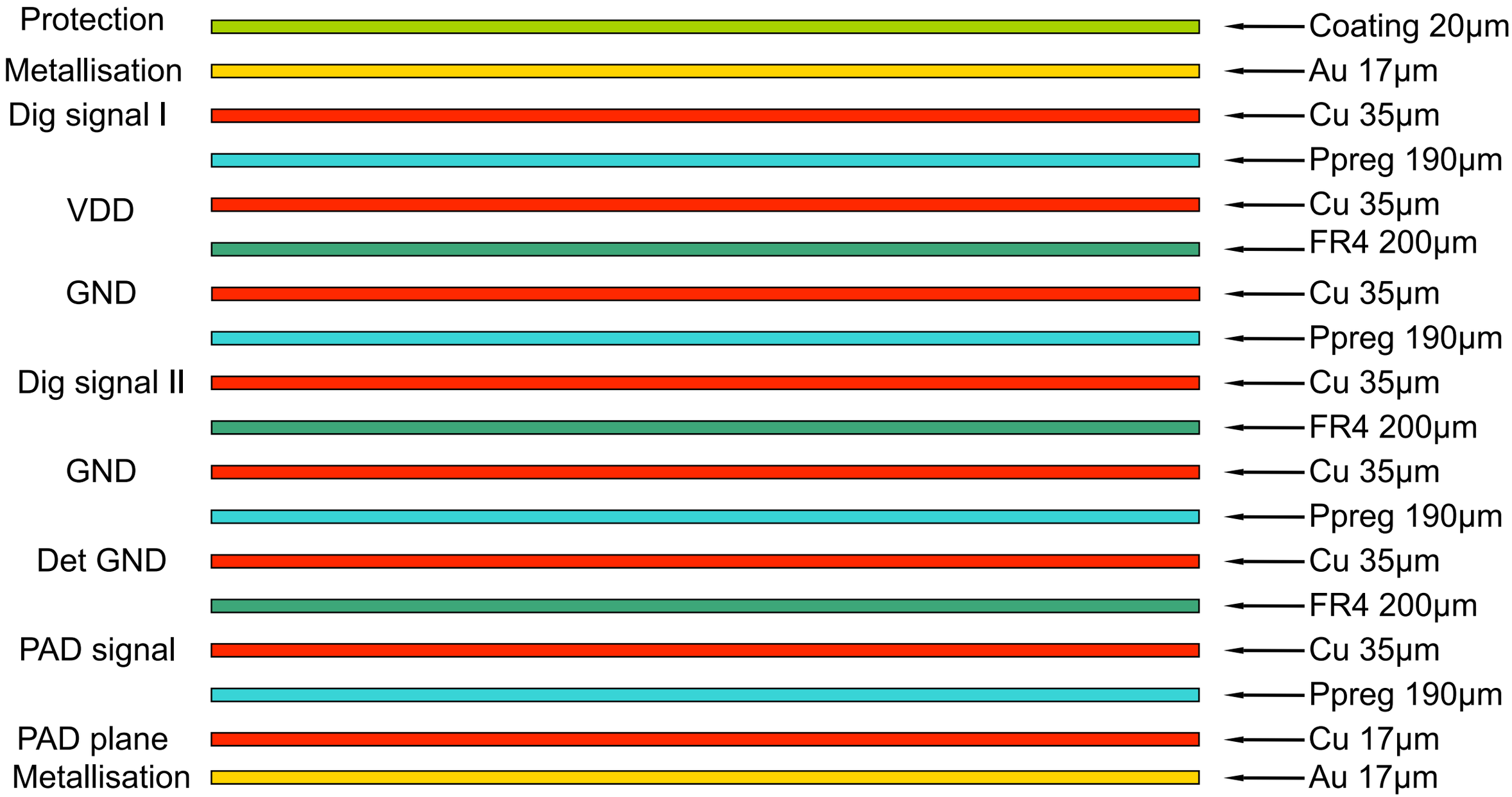


Dimensions & Layout

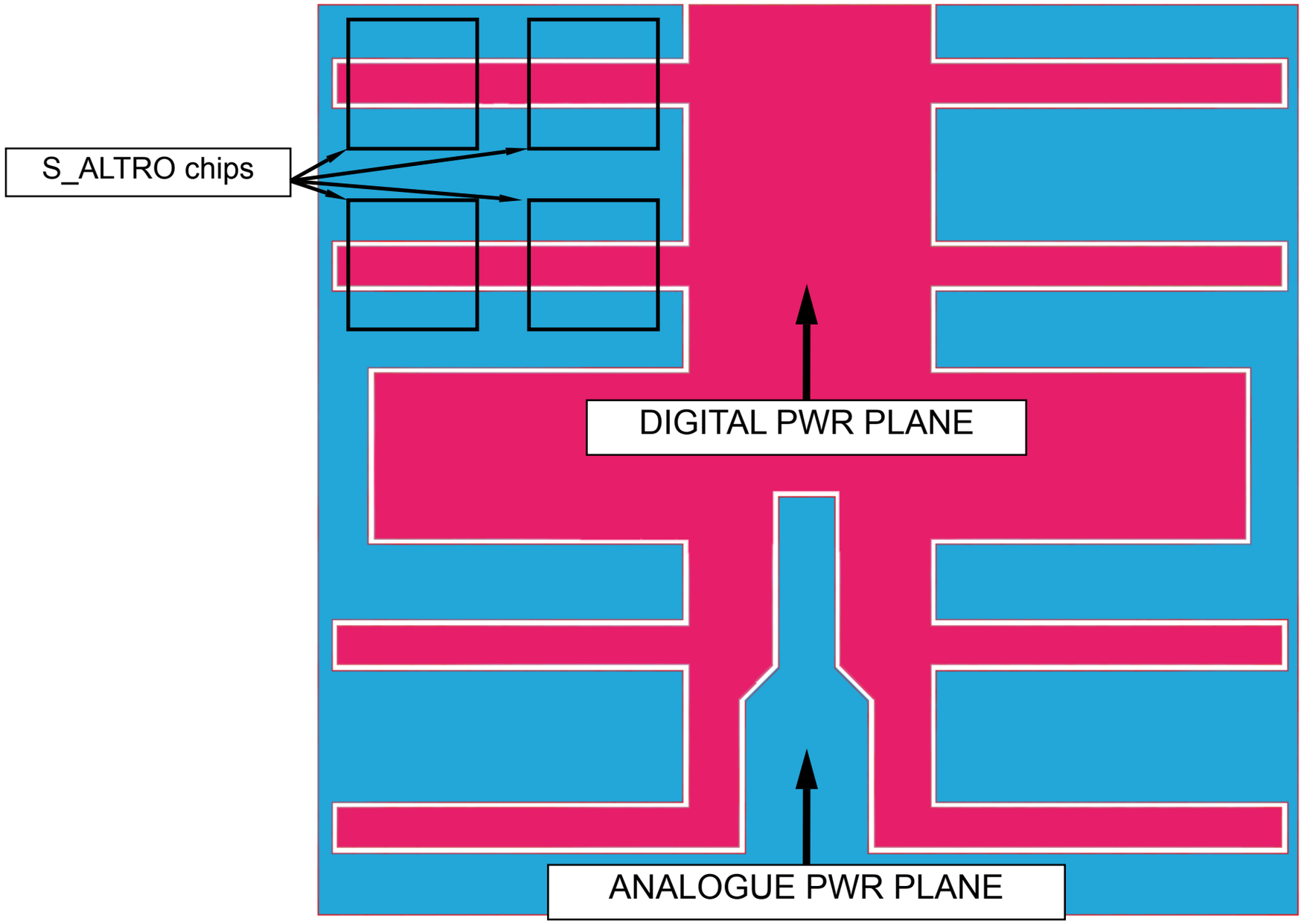




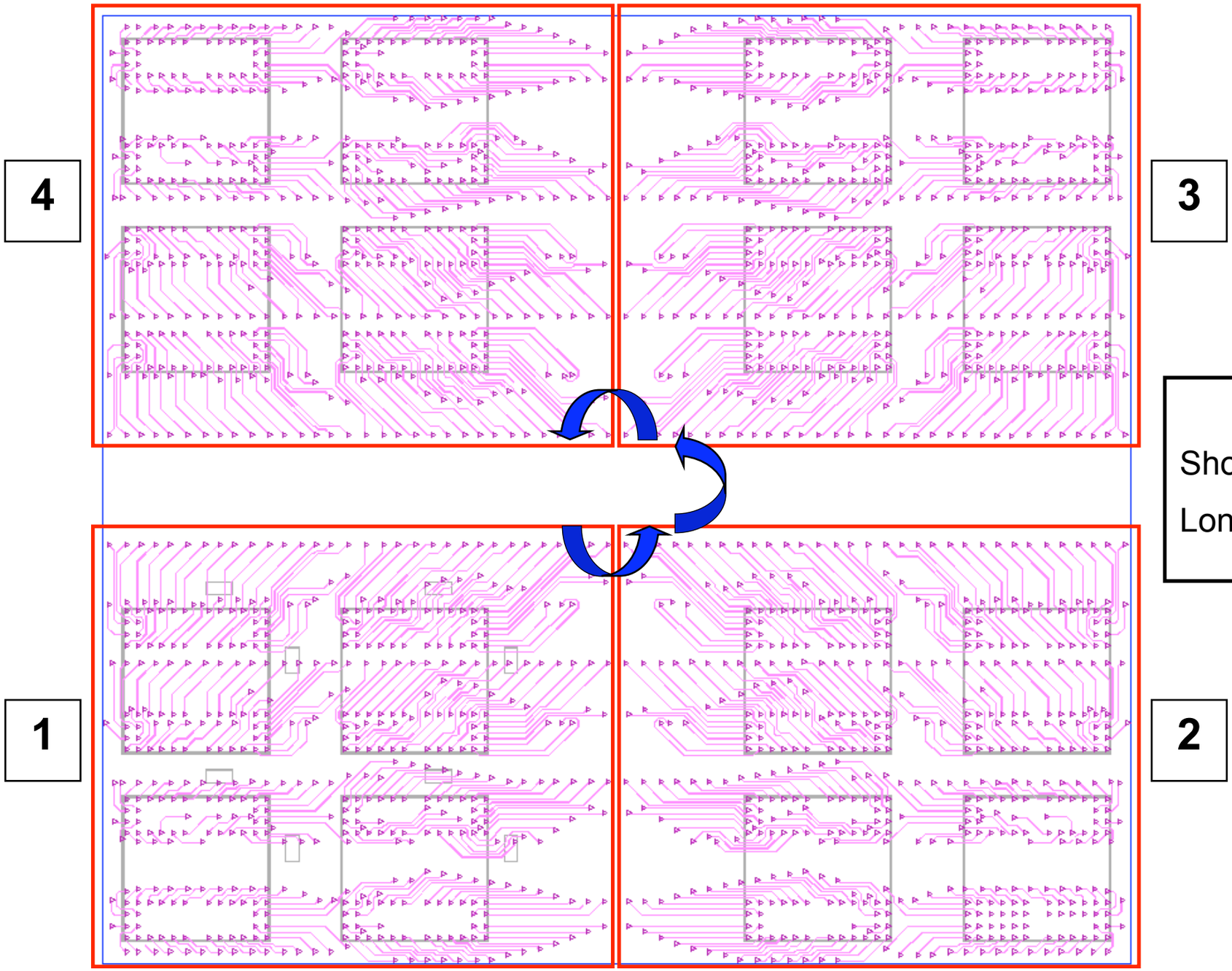
Layer stack-up



Power distribution



Signal routing

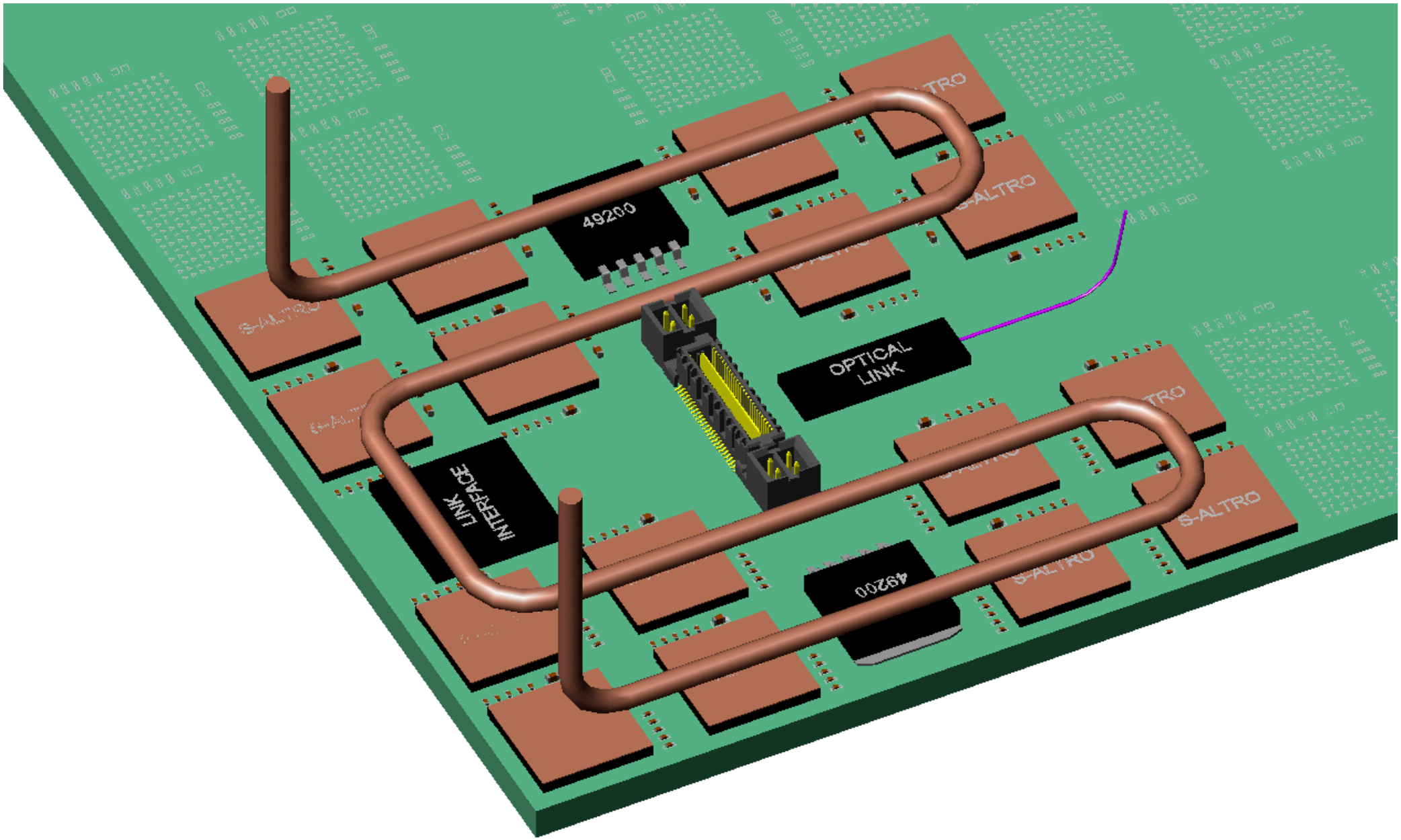


Lines length

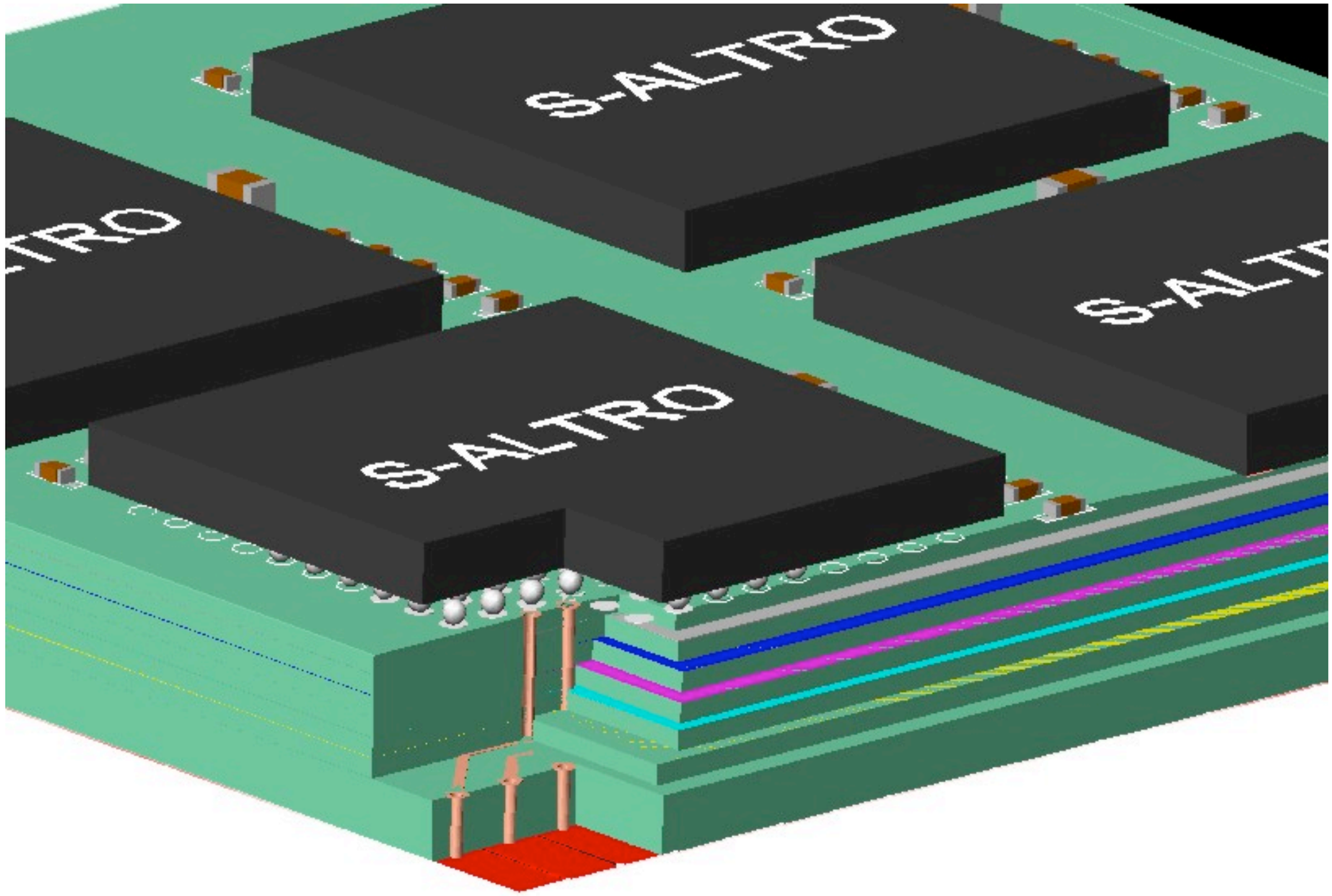
Shortest : 0.8 mm

Longest : 10 mm

Close-up view



Close-up view II



Plans

- Adopt design to real geometry, in particular:
  - non-quadratic shape of chamber
  - mounting margins
- Understand heat production and cooling
  - 40mW/ch
- Power pulsing
  - FPGA prototype by Japanese group