Status of the LP-TPC at DESY

Klaus Dehmelt

DESY

EUDET Annual Meeting 2009

Geneva, Switzerland

Oct. 19, 2009

LP TPC

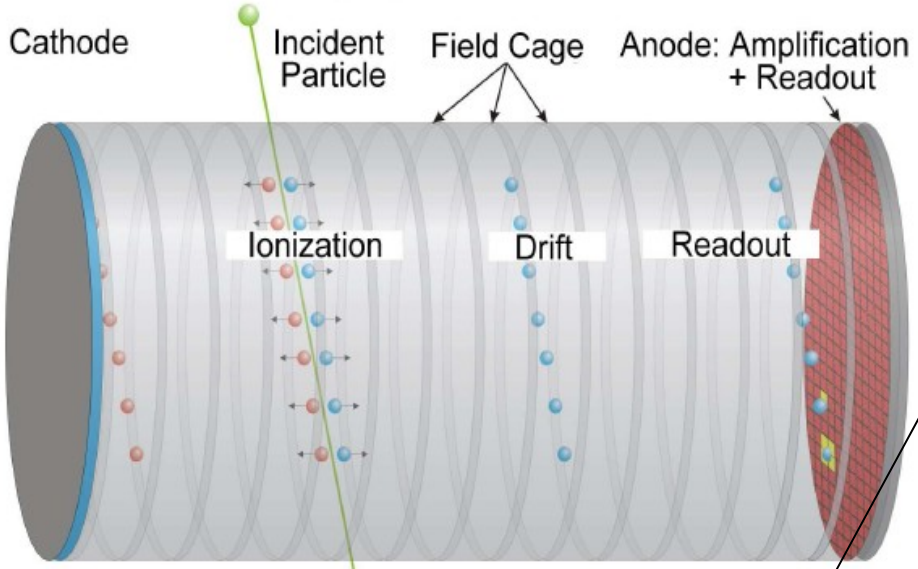
Main objective: Large Prototype (LP) of a TPC.

Consisting of

- Field cage
- Readout electronics
- DAQ and Monitoring
- Gas-/HV-system
- Common Software
- SiLC envelope
- End plate
- MPGD detector modules
- Cosmic/beam trigger

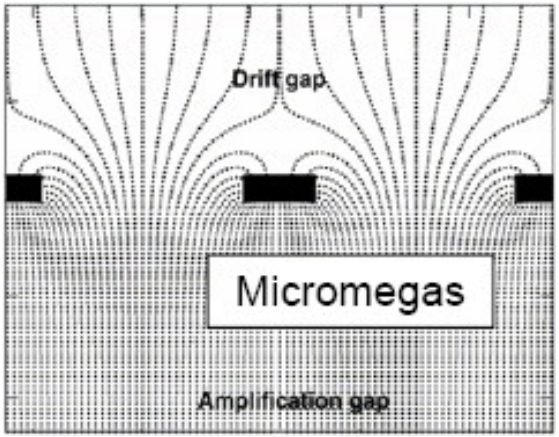
Magnet (PCMAG) + infrastructure
DESY II: T24 Test beam

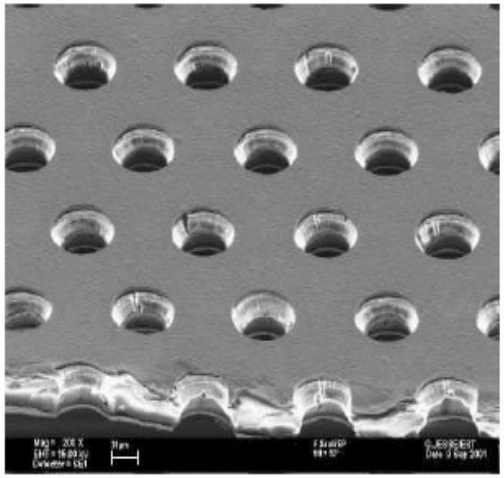
TPC with MPGD

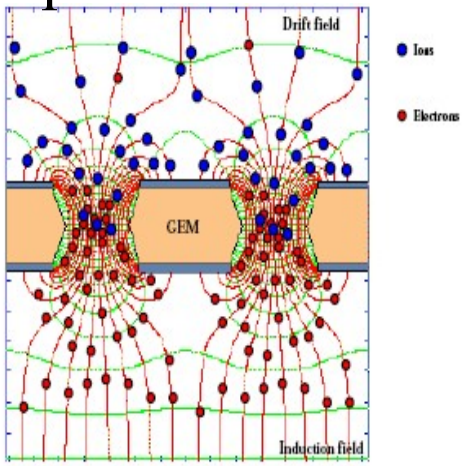


MicroPatternGasDetector
MPGD
not limited by **E** x **B** effects

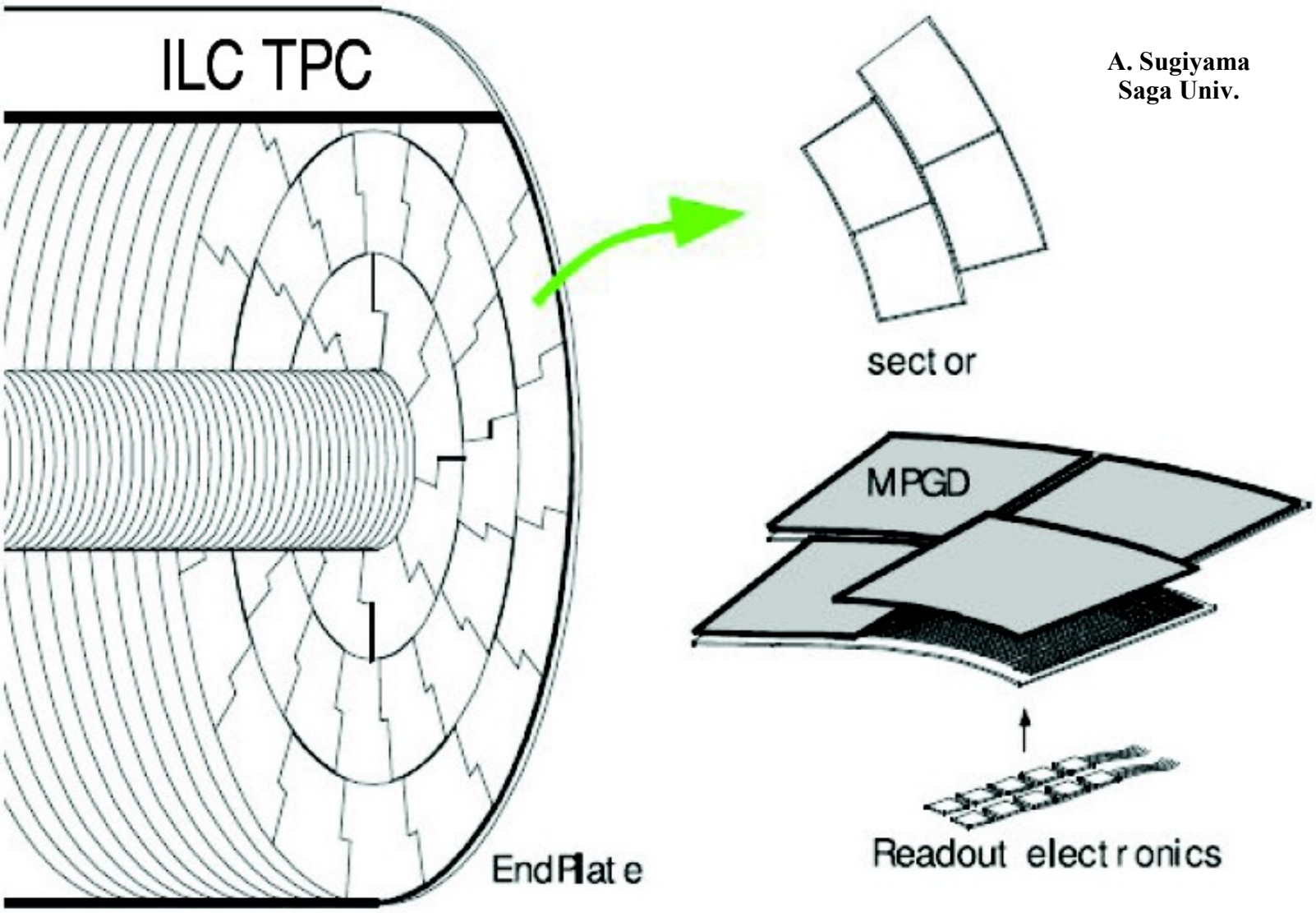
Gas Electron Multiplier GEM





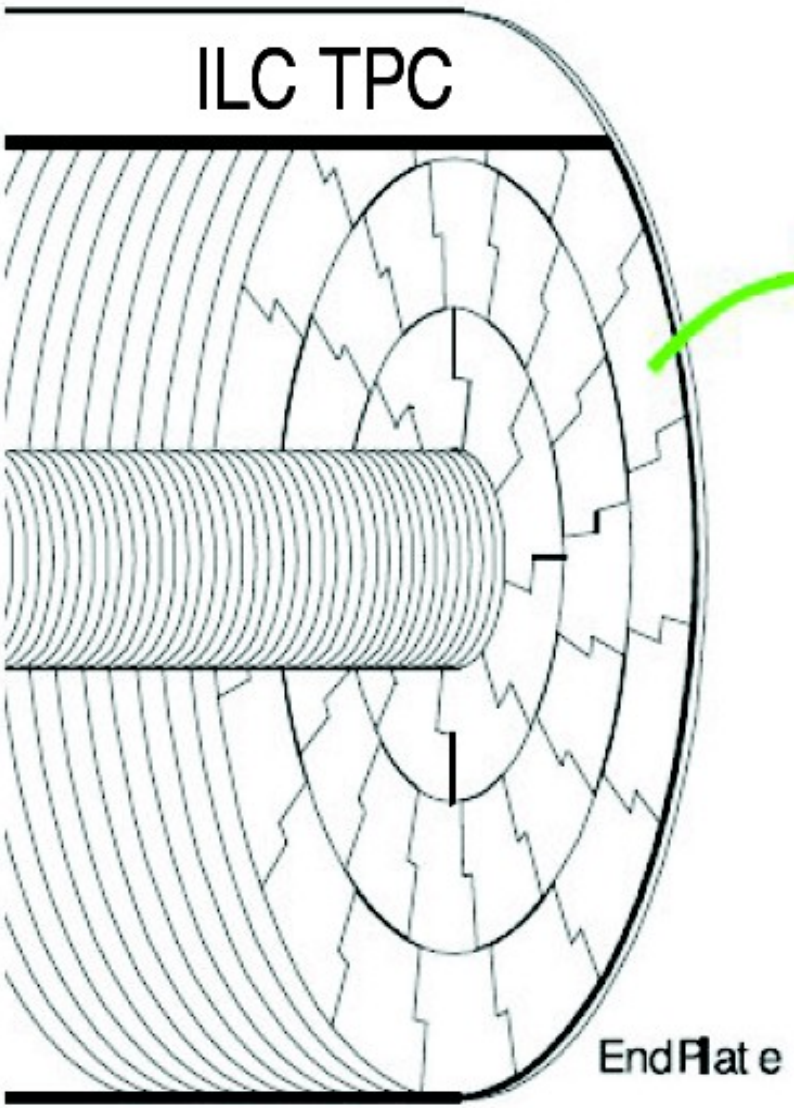


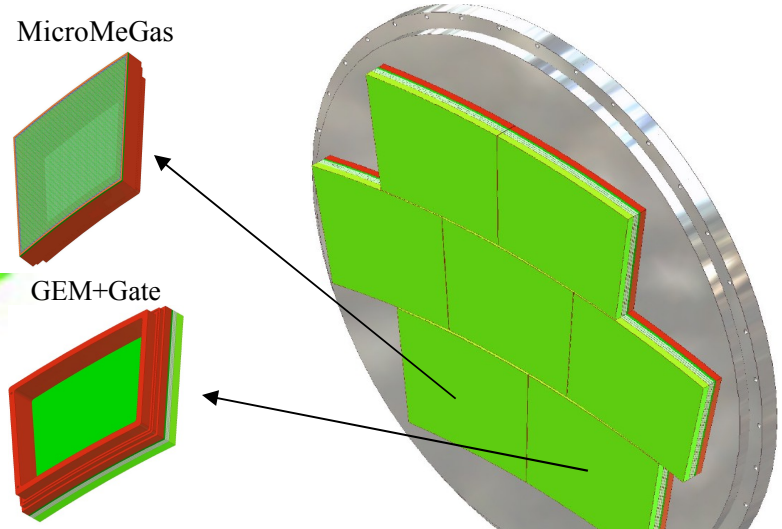
TPC with MPGD



A. Sugiyama
Saga Univ.

TPC with MPGD





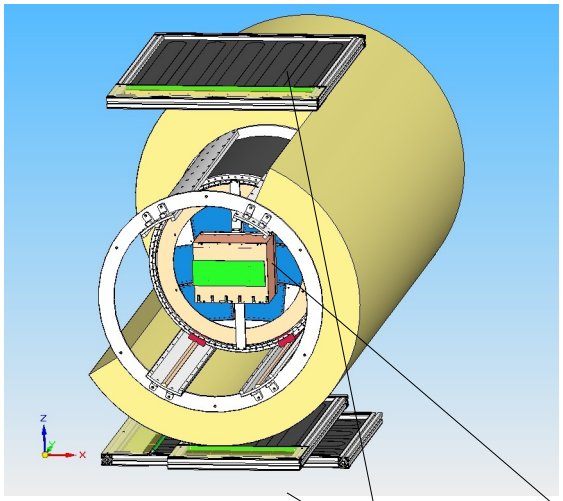
D. Peterson, Cornell

Endplate:

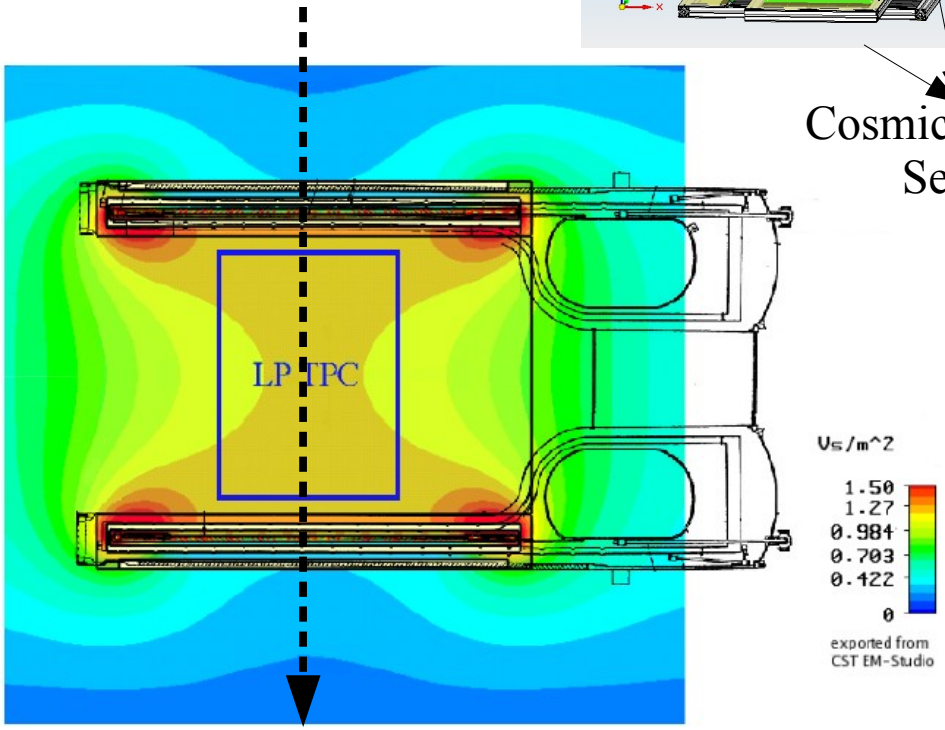
- Aluminum
- Accommodates seven detector/ dummy modules
- $d = d_{outer,FC} = 770$ mm
- Modules have same shape → interchangeable

DESY Setup

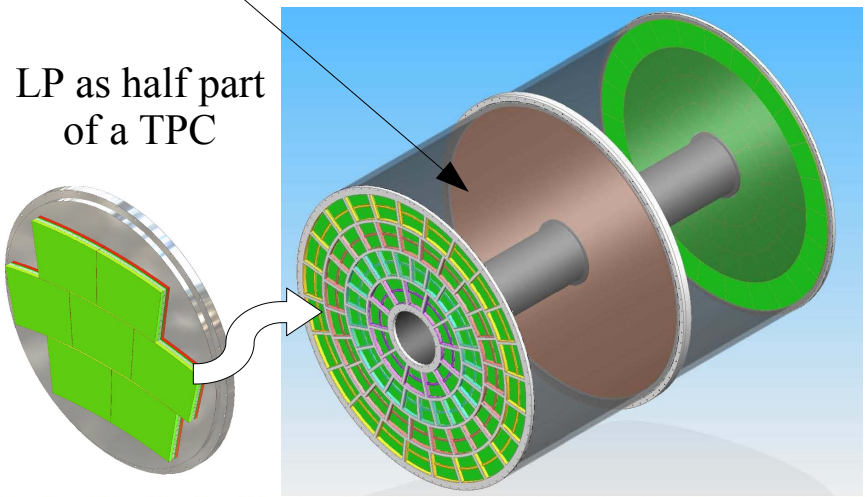
- *PCMAG:* superconducting magnet, up to 1.25 T
- e^- test beam @DESY (1GeV/c<p<6GeV/c)



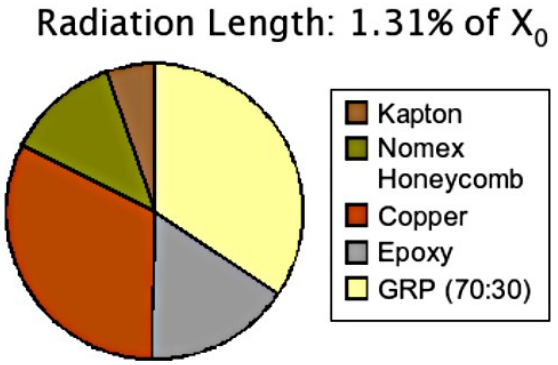
Cosmic Trigger Setup

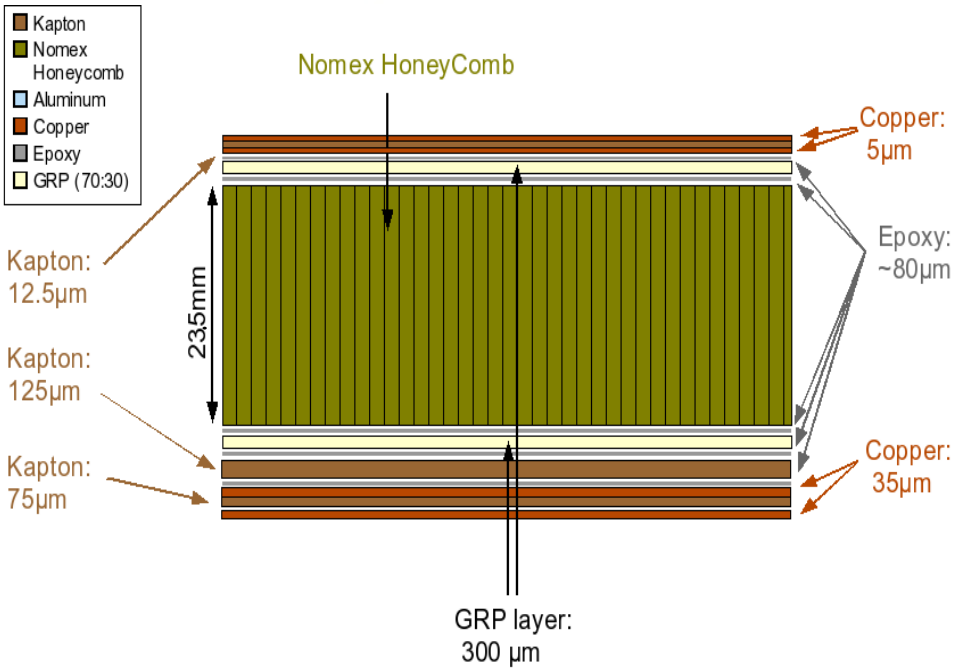


LP as half part of a TPC



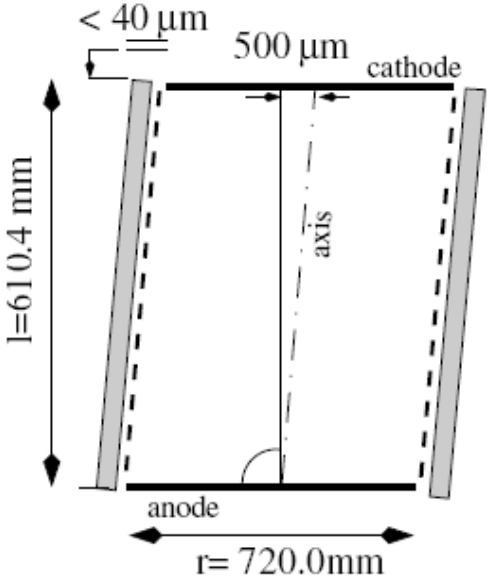
LP-TPC Field Cage (FC)

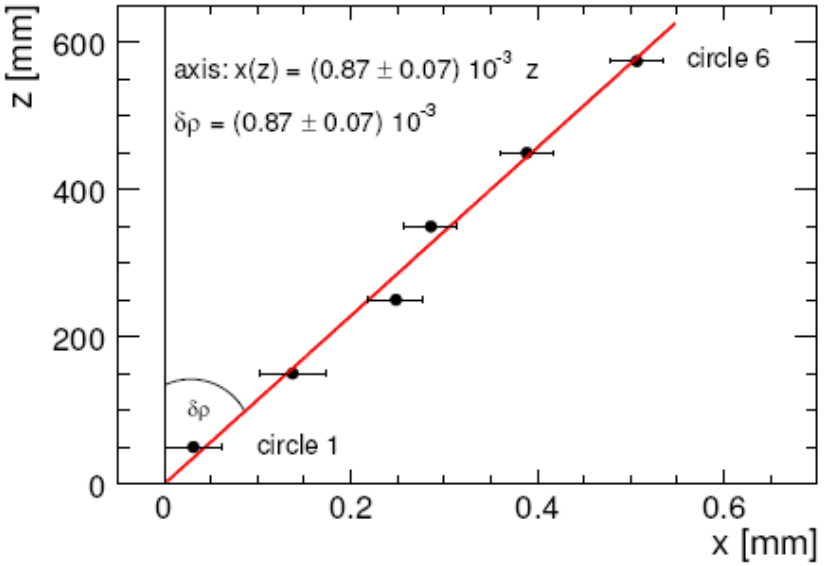


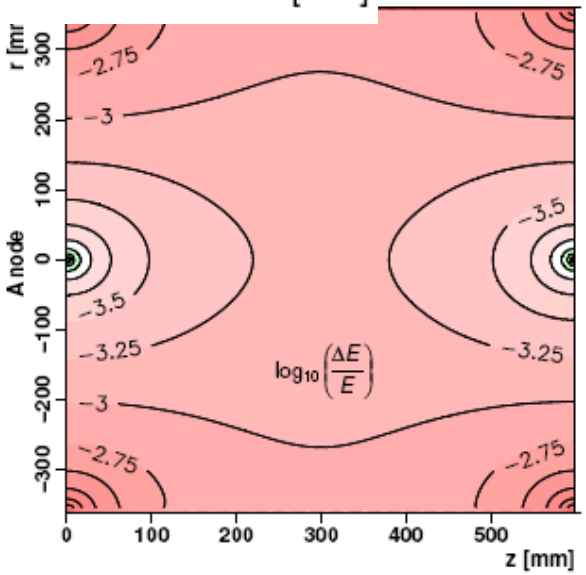


Diameter: Inner 720 mm,
Outer 770 mm
Wall thickness 25 mm
Length 610 mm
HV to be applied: up to 20 kV

FC





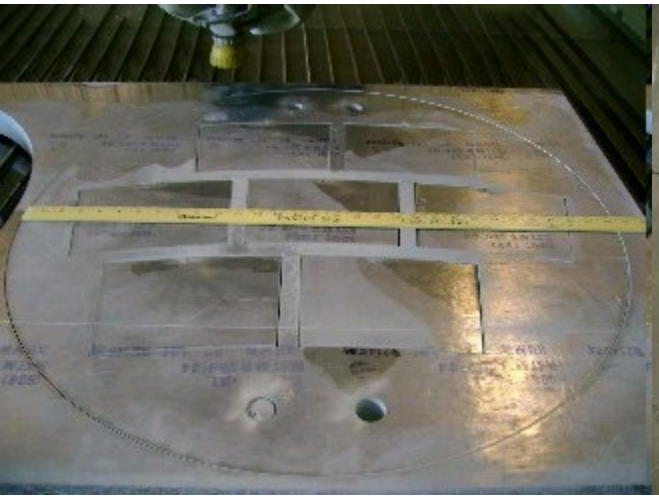
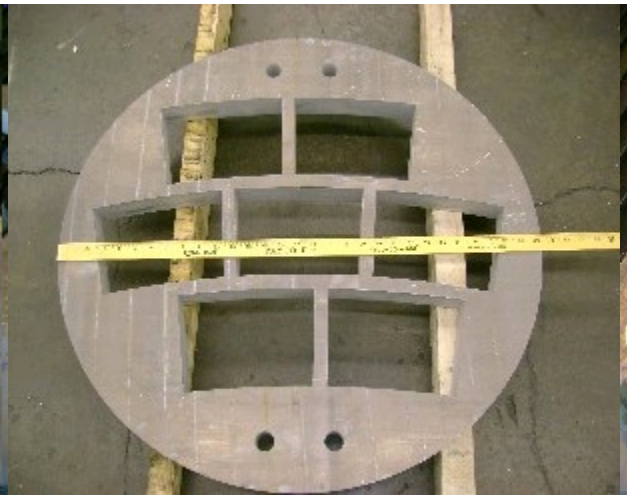


Achieved mechanical accuracy:

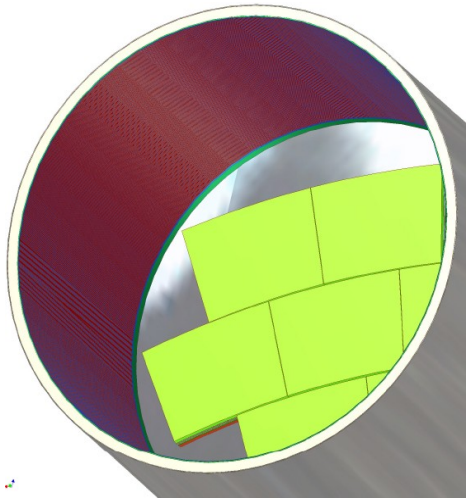
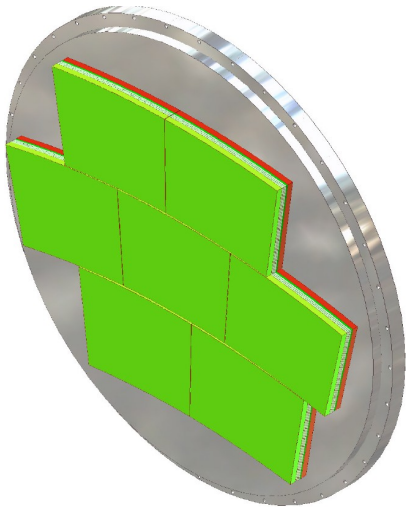
- Aligment of the end faces: $\delta l < 40\ \mu m$
- Alignment of field cage axis: $\delta A \sim 500\ \mu m$
- Field quality $10^{-4} \lesssim \Delta E/E \lesssim 10^{-3}$

P. Schade, DESY

LP-TPC Endplate

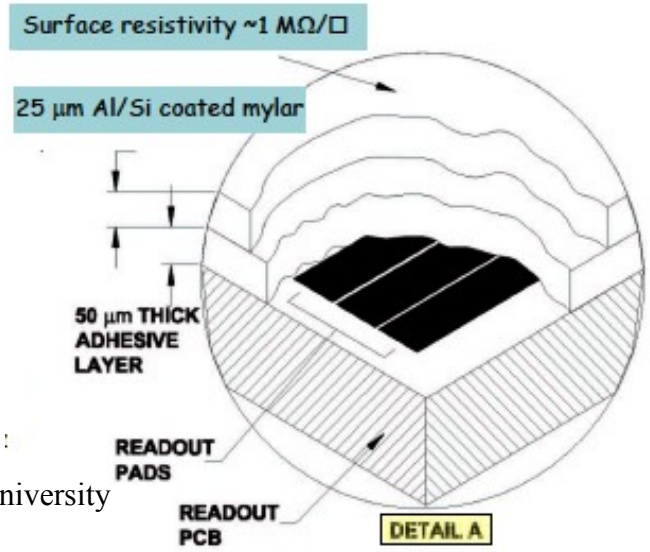


D. Peterson, Cornell

MicroMeGaS Structure

'Bulk Micromegas' panels, without resistive foil and with resistive carbon-loaded kapton, have been produced at CERN (Rui de Oliveira)

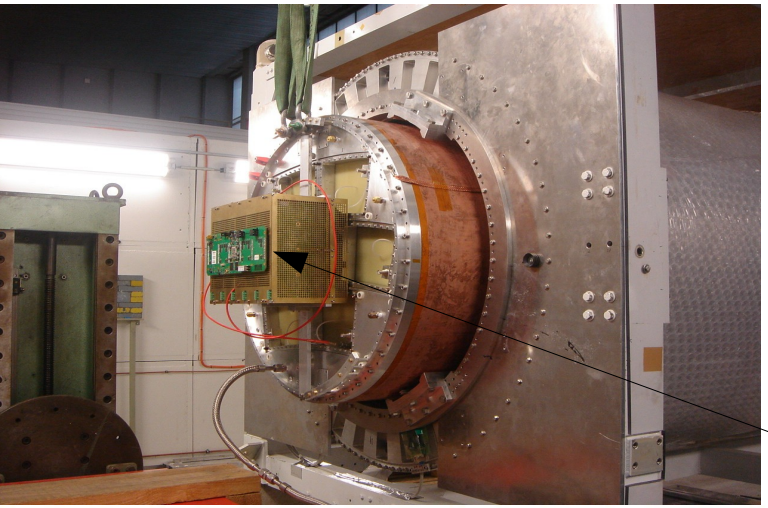


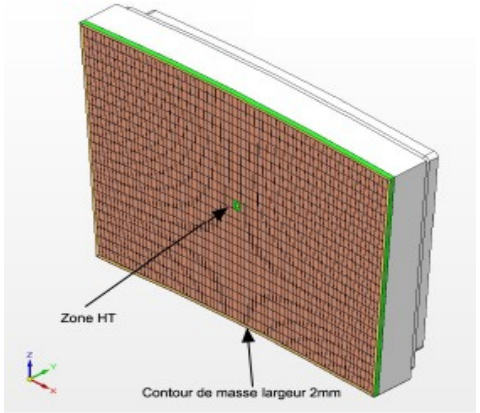
MicroMeGaS for LP:

24 rows x 72 pads

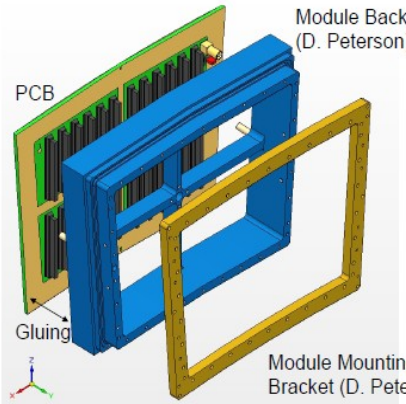
Av. Pad size: 3.2 x 7mm²

P. Colas, CEA Saclay
M.S.Dixit, Carleton University





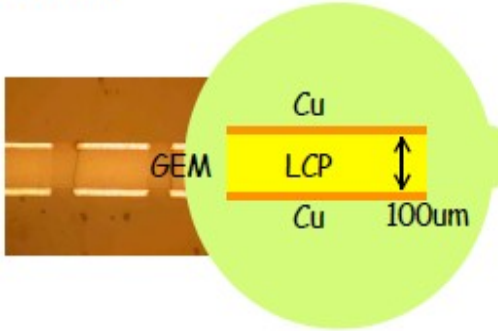
Detector side



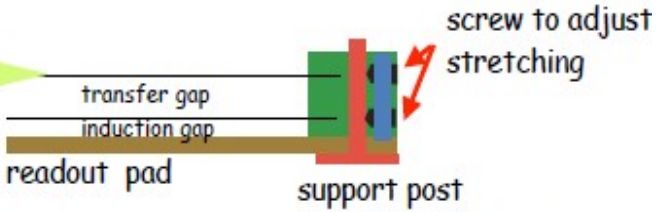
Readout electronics: AFTER (T2K TPC)

Double GEM Structure

GEMs

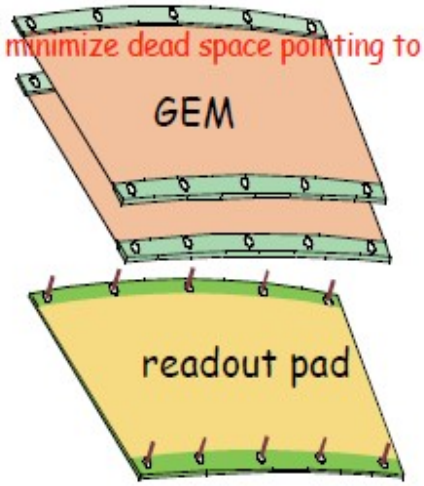


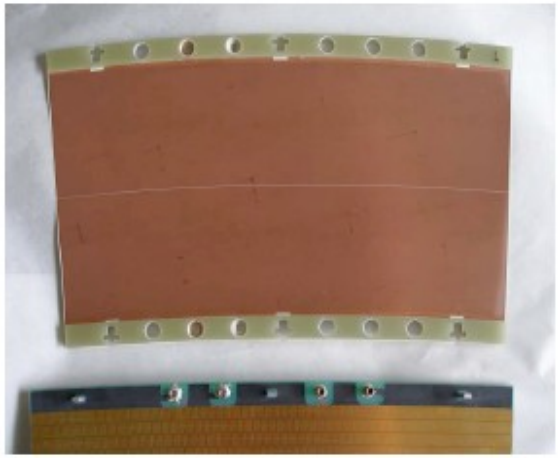
mounting(stretch) mechanism



Transfer gap ~ 4mm (+2mm) : enlarge signal distribution width > 0.3* pad pitch

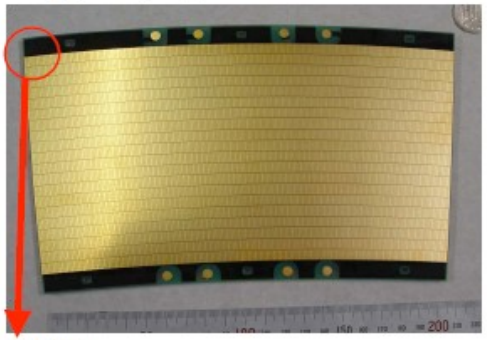
frame : top & bottom frame.
no side frame

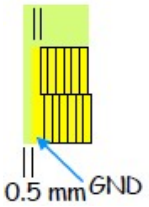




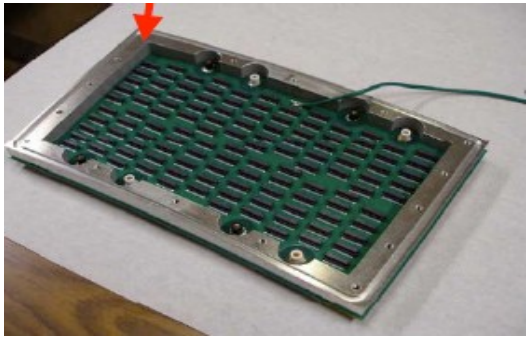
28 pad raws (176/192 pads/raw)
~1.2(w) x 5.4(h) mm^2
staggered every each layer

Total 5,152 ch/module





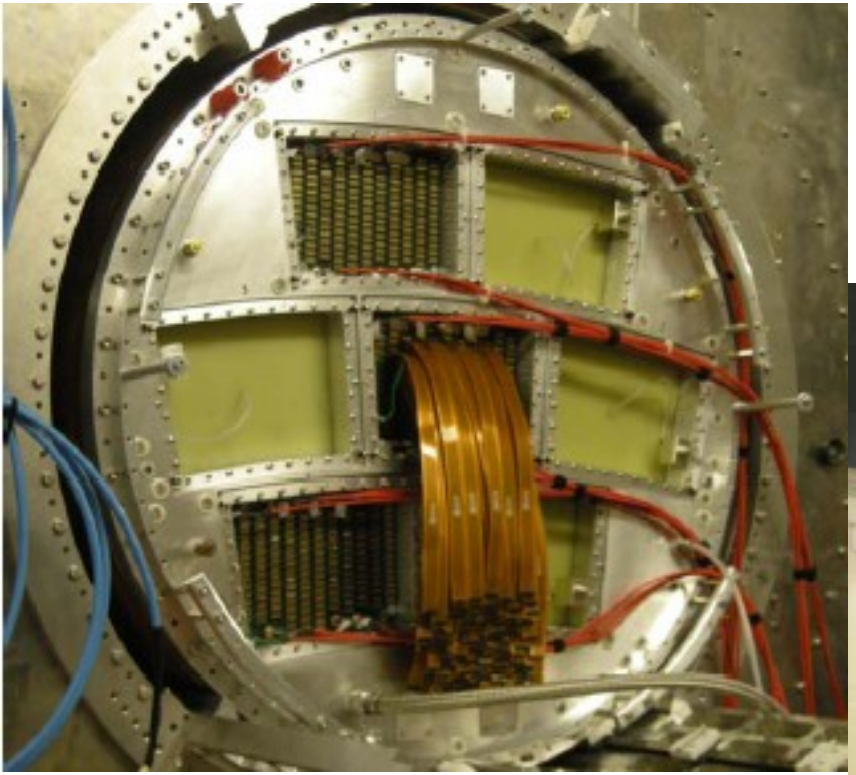
6 layers PCB
one GND layer



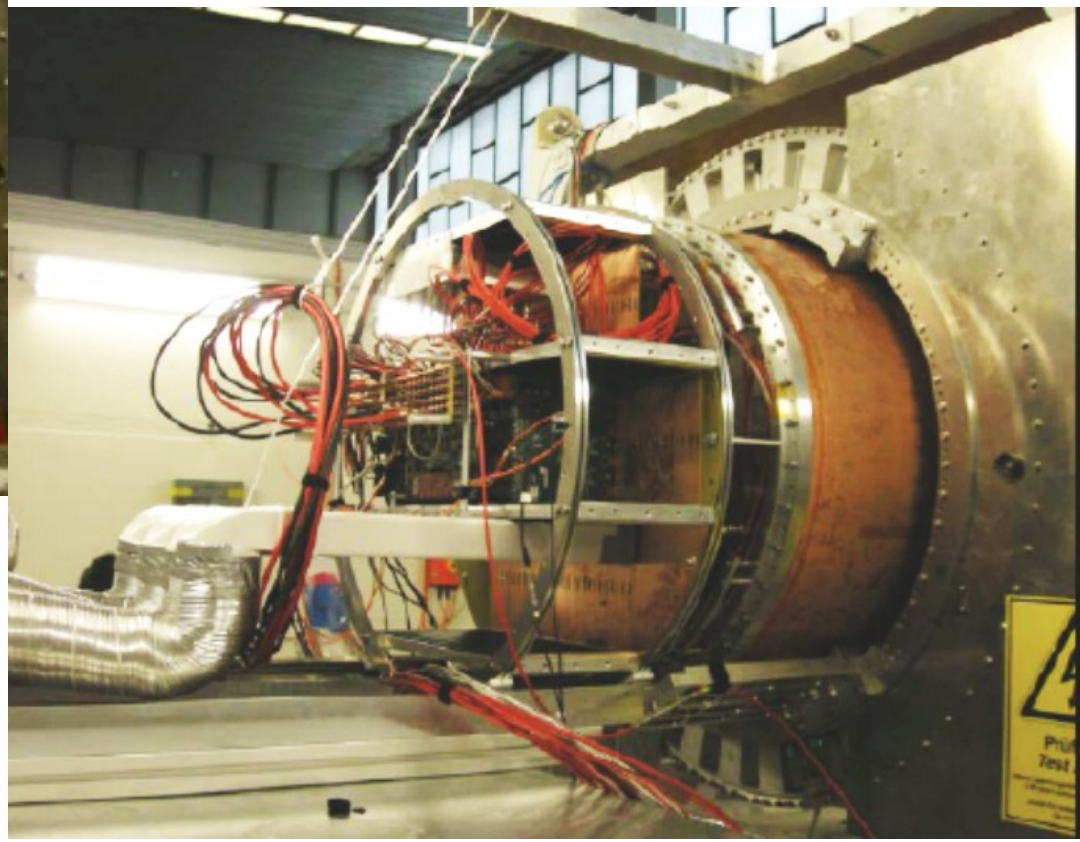
Setup planned w/ gating GEM

A. Sugiyama, Saga Univ.

Double GEM Structure



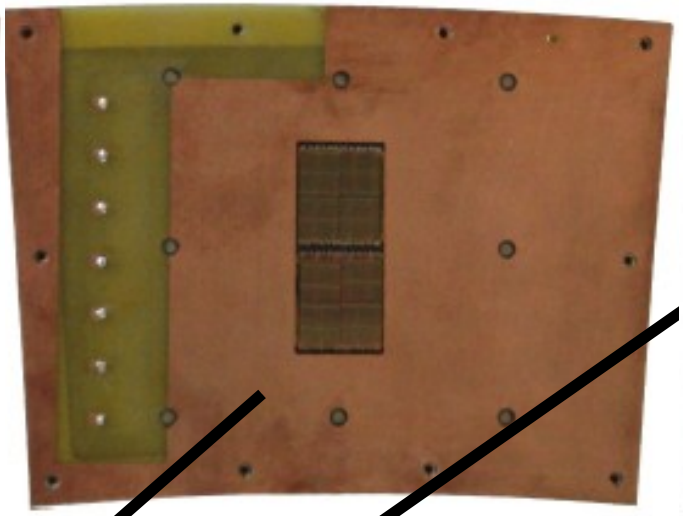
About 3200 channels readout electronics

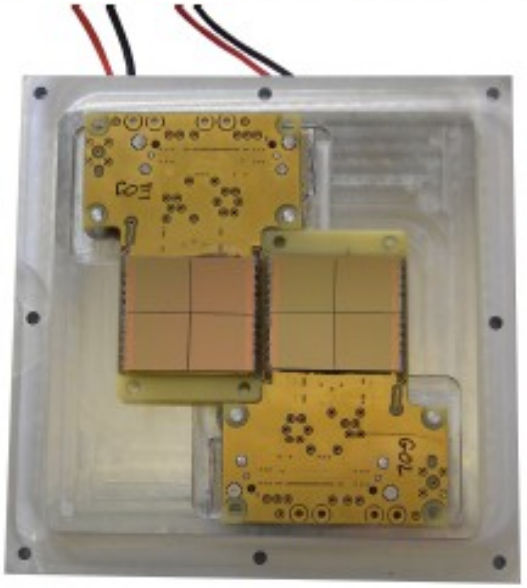


Readout electronics:
Based on ALTRO (ALICE TPC)

L. Joensson, LUND University

3-GEM Structure & TimePix





anode plane

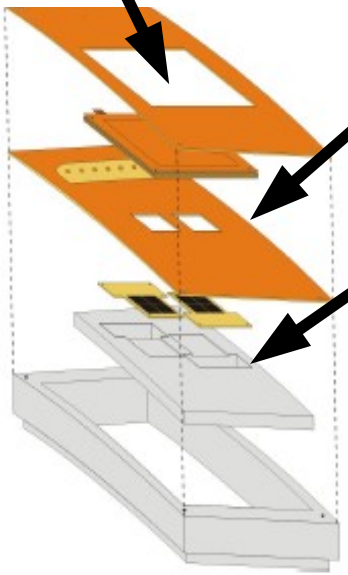
GEMs

readout plane

quad-boards

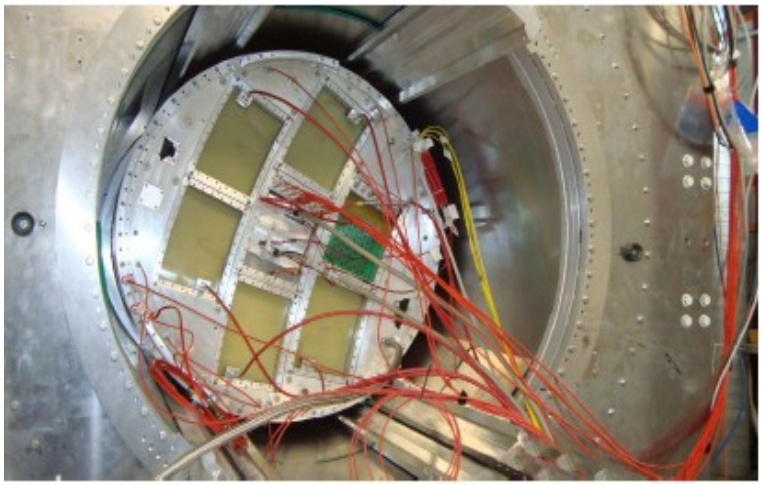
reinforcement of anode plane

redframe



Readout:
2 quadboards
(4 TimePix
Chips each)

J. Kaminski, Univ. of Bonn

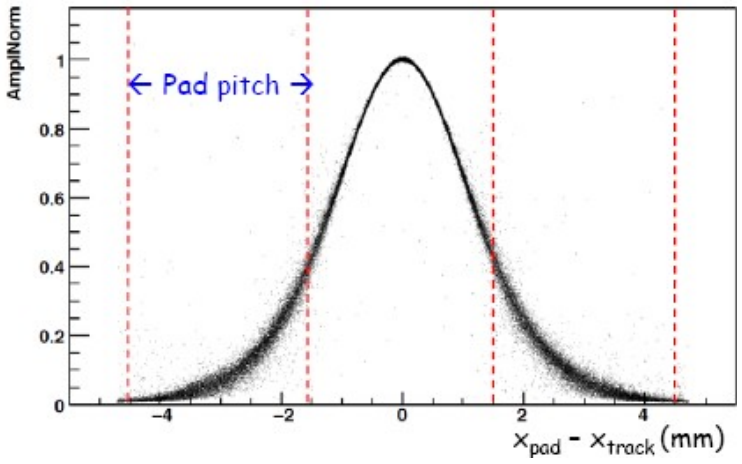


MicroMeGaS Structure

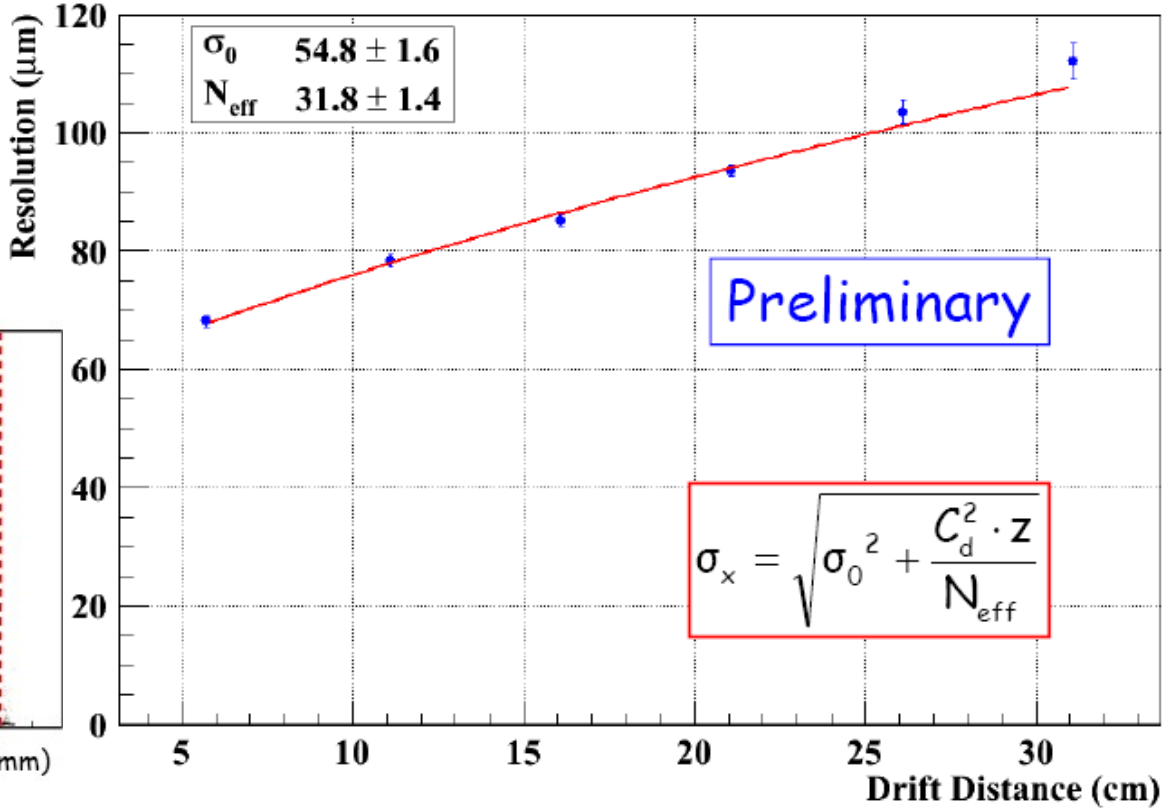
Electrons (5 GeV), Magnetic field (B=1T)

- Fraction of the row charge on a pad vs $x_{pad} - x_{track}$ (normalized to central pad charge)

→Clearly shows charge spreading over 2-3 pads (data with 500 ns shaping)



- Resolution at z=0: σ_0 = 54.8±1.6 µm with 2.7-3.2 mm pads (w_{pad}/55)
- Effective number of electrons: N_{eff} = 31.8±1.4 consistent with expectations

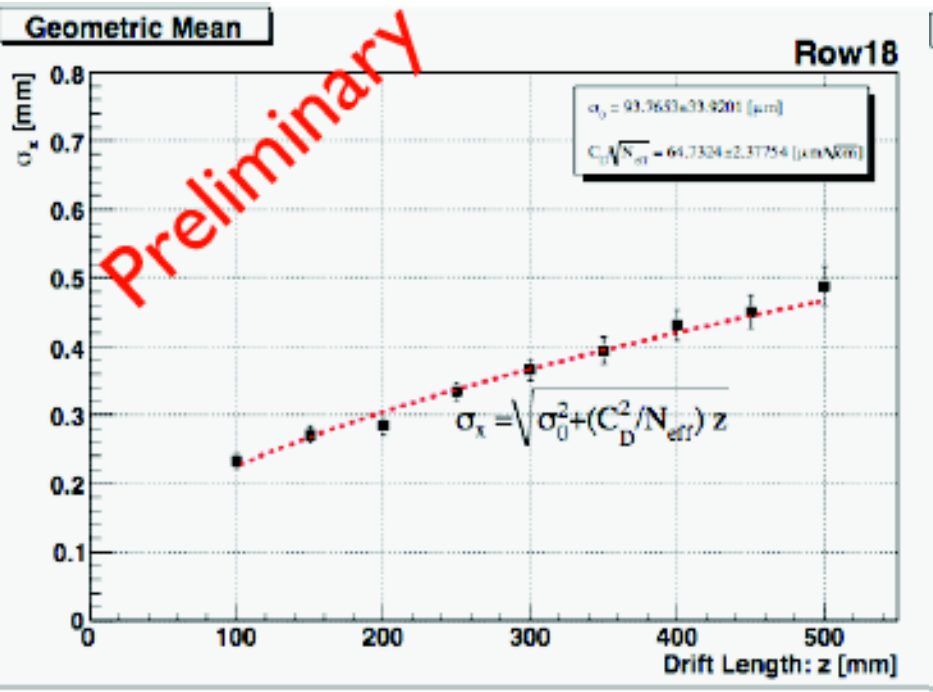


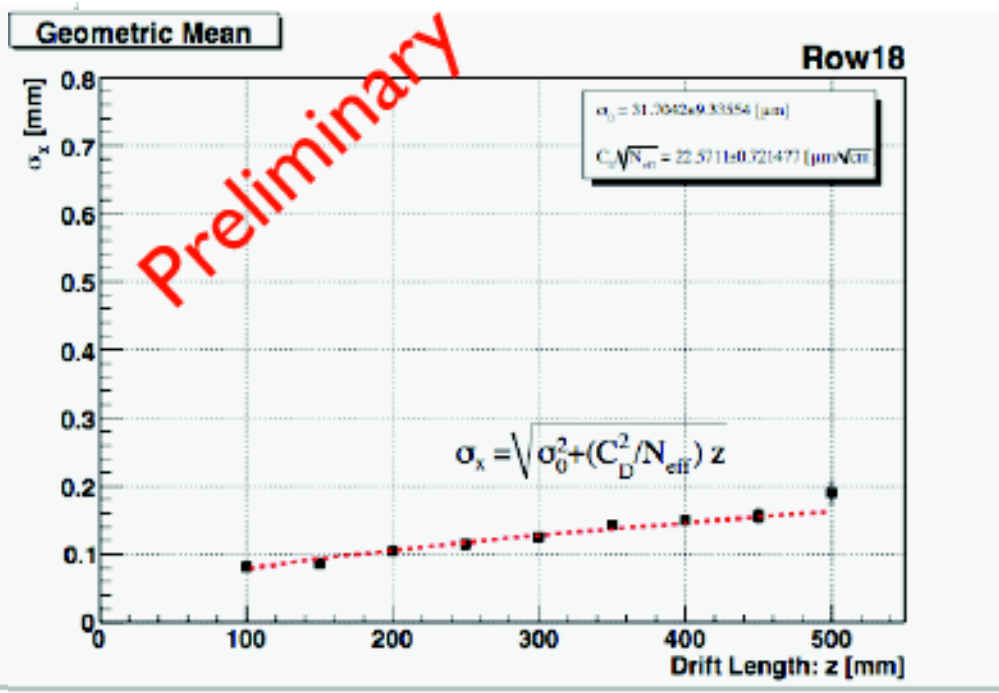
P. Colas, CEA Saclay

Double GEM Structure

Resolution as a function of drift distance

R. Yonanime, KEK





B=0T

$$\begin{cases} C_D = 303 \pm 1 [\mu/\sqrt{cm}] \\ \dfrac{C_D}{\sqrt{N_{eff}}} = 65 \pm 2 [\mu m/\sqrt{cm}] \end{cases}$$

$\longrightarrow N_{eff} \sim 22 \pm 1$

Garfield

$C_D = 311.8 [\mu m/\sqrt{cm}]$

Result of MP-TPC
Neff = 21±2

B=1T

$$\begin{cases} C_D = 101.6 \pm 0.4 [\mu/\sqrt{cm}] \\ \dfrac{C_D}{\sqrt{N_{eff}}} = 22.6 \pm 0.7 [\mu m/\sqrt{cm}] \end{cases}$$

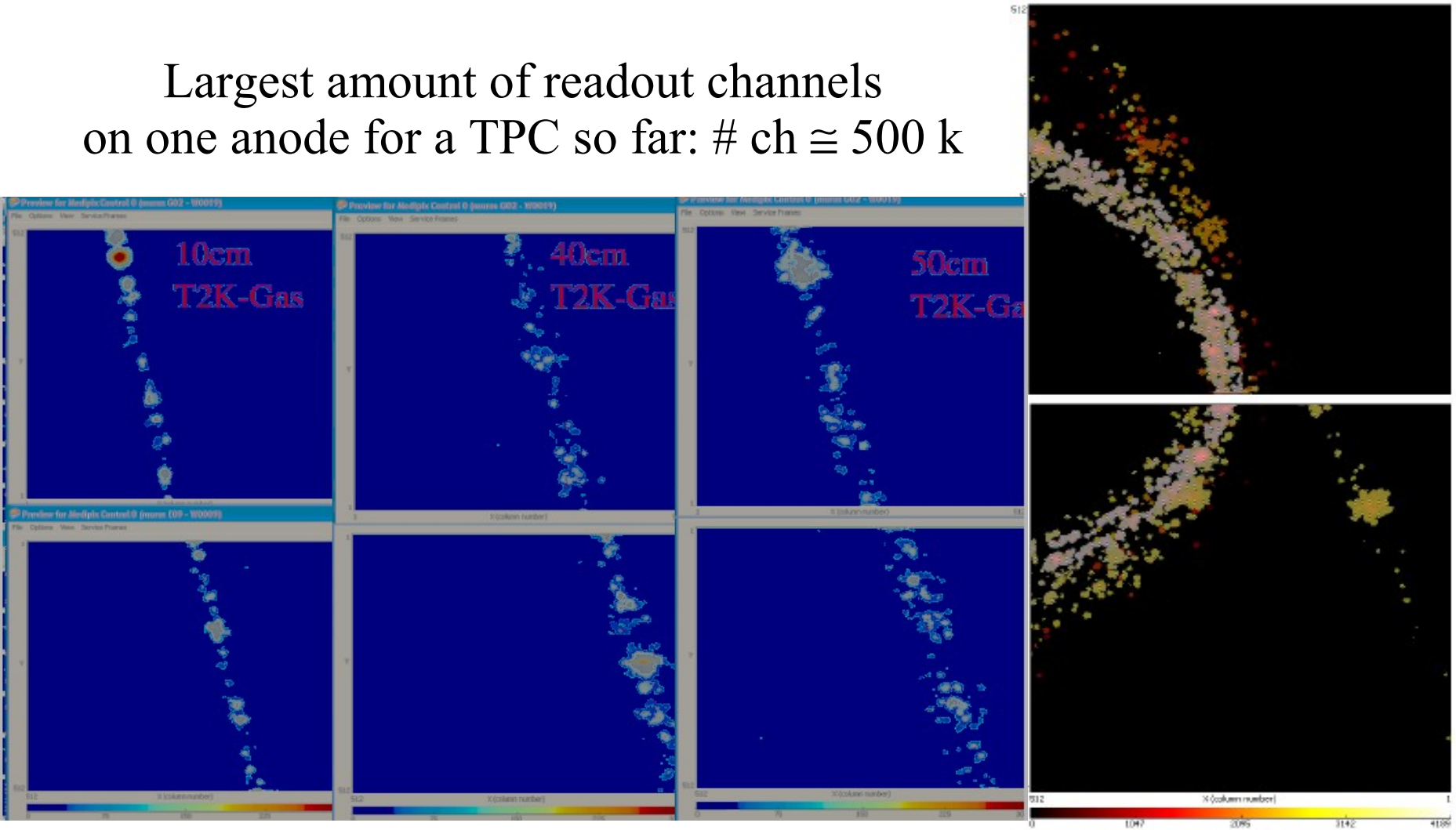
$\longrightarrow N_{eff} \sim 20 \pm 1$

Garfield

$C_D = 95.4 [\mu m/\sqrt{cm}]$

3-GEM Structure & TimePix

Largest amount of readout channels
on one anode for a TPC so far: # ch ≅ 500 k



J. Kaminiski, Univ. of Bonn

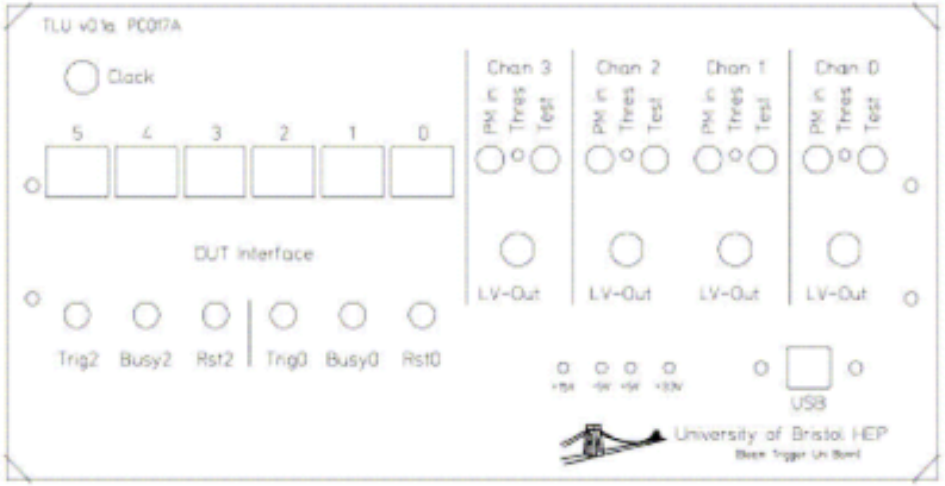
DAQ Trigger System

Trigger Logic Unit (TLU) provided by University of Brussels:

- 4 comparators
- Beam trigger with scintillators

TLU outputs:

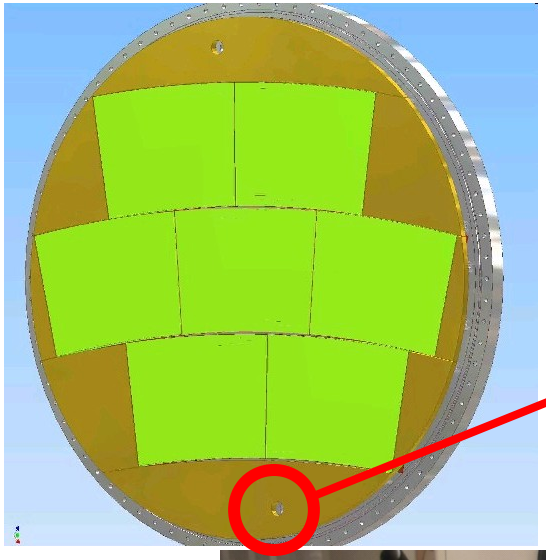
- Trigger signal (LVDS)
- Event number (LVDS) pulled out by a data clock (LVDS)

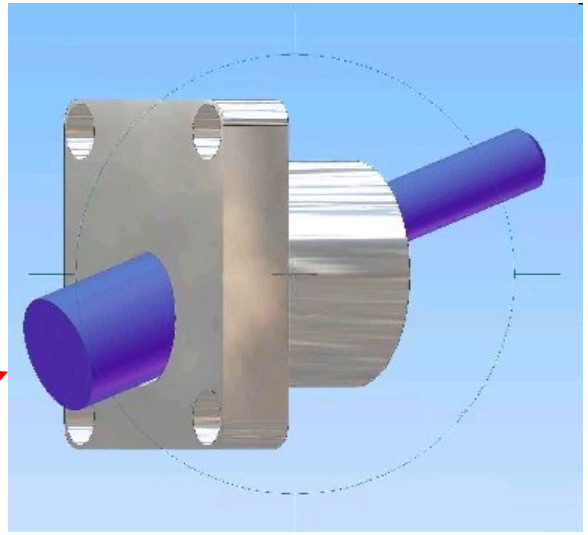


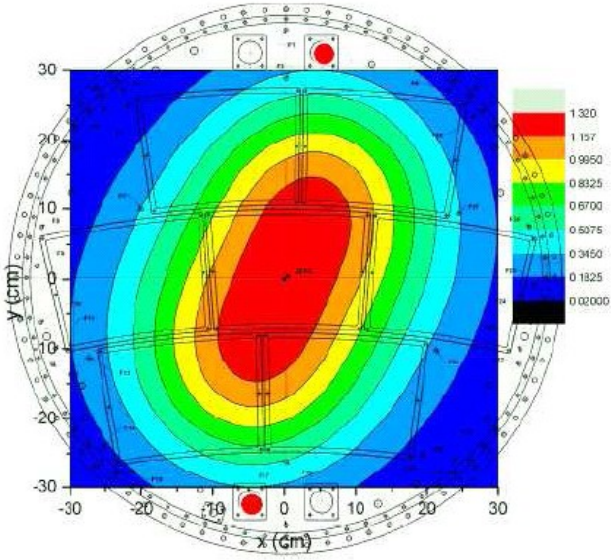
Distributor box:

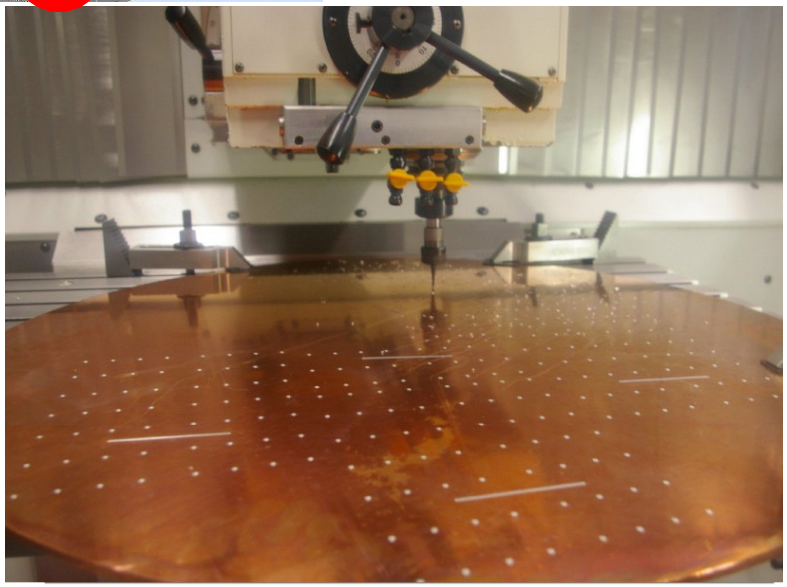
- Get event# from TLU and tag event with time
- Send event # + time to DAQ computer, assert BUSY for a fixed time: waiting for DAQ PC end of r/o
- Provide common clock

Laser Calibration Setup



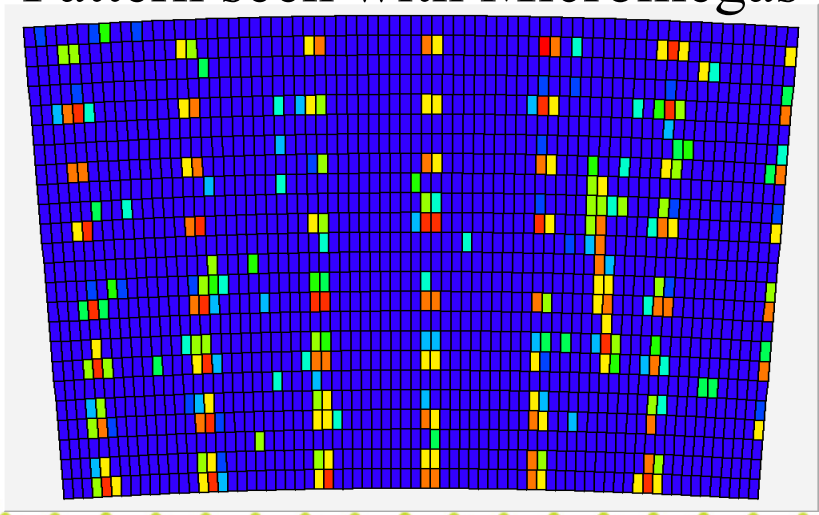






P. Conley
Victoria Univ.

Pattern seen with Micromegas



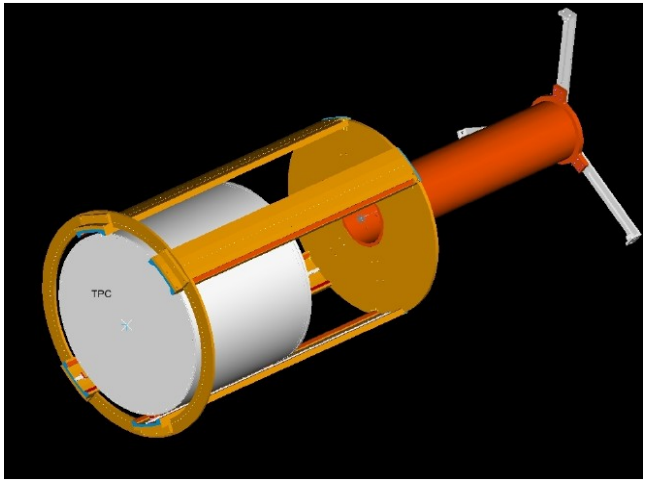
Common Software

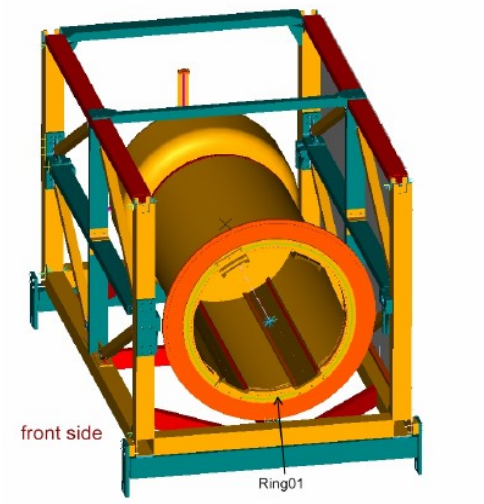
Goal:
- Common data taking
- Common data stream
- Common data format
- Unified reconstruction and analysis

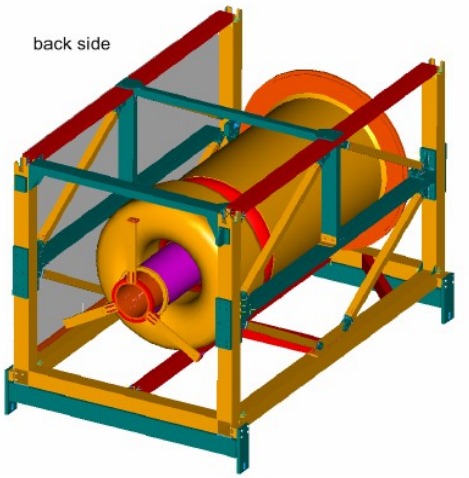
Modular **A**nalysis & **R**econstruction for the **L I N**ear Collider

Modular MarlinTPC:
Marlin based simulation, digitization, reconstruction and analysis code for the TPC

LP Mechanics

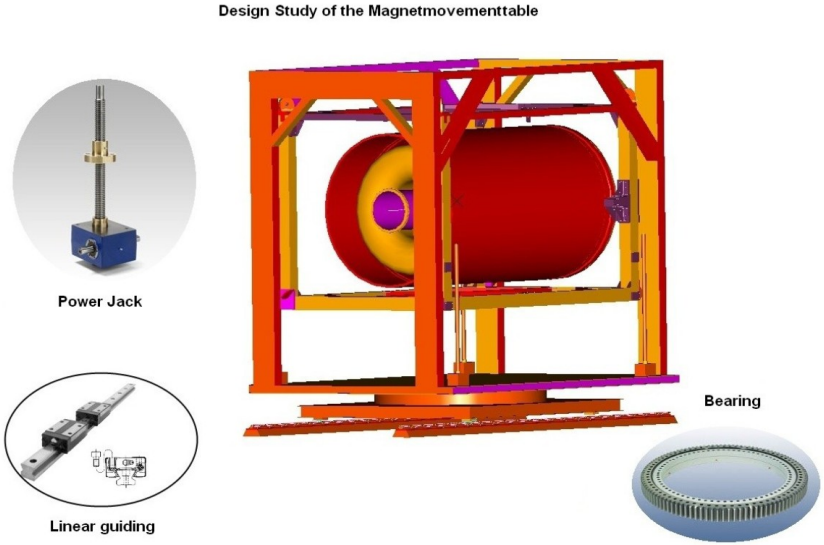






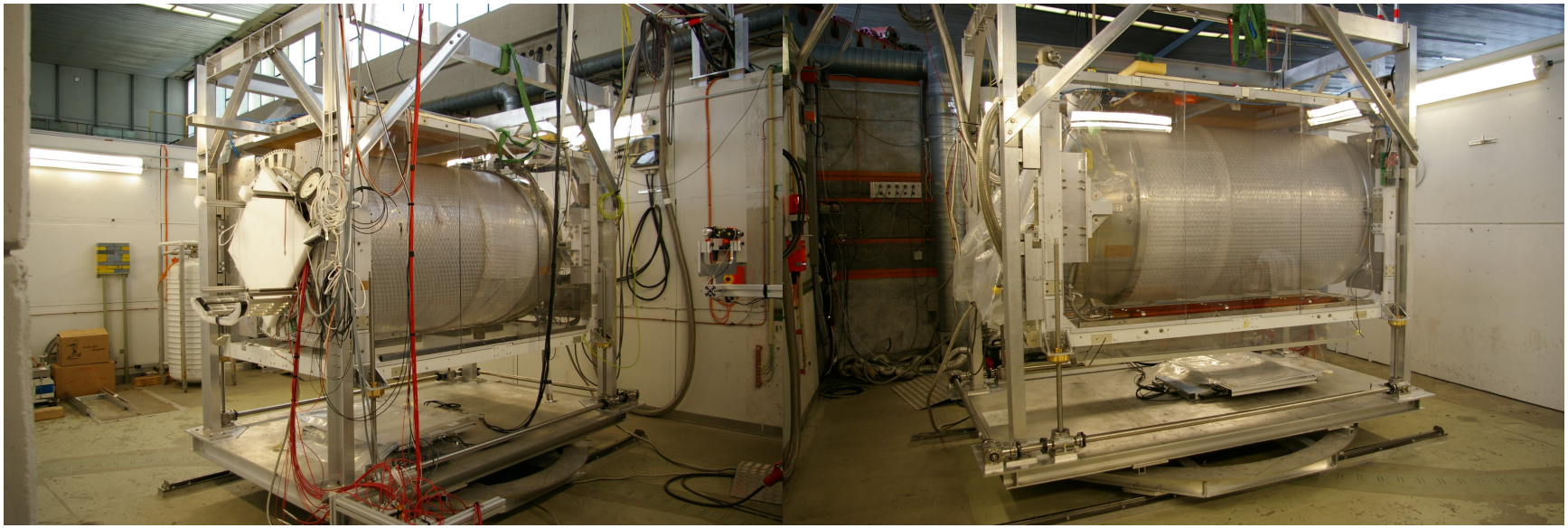
Support structures:

- TPC
- PCMAG

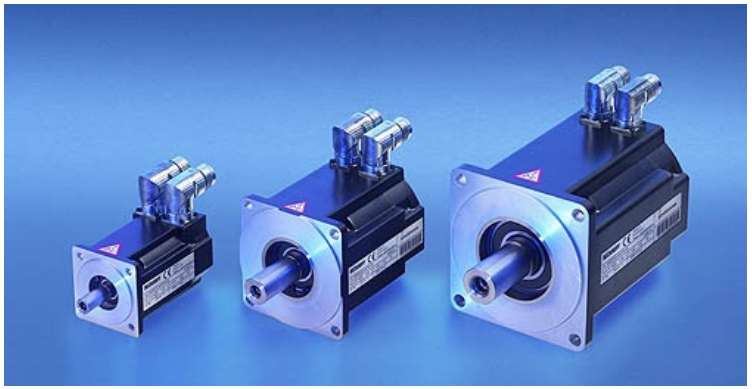


F. Hegner, V. Prahl, R. Volkenborn, DESY

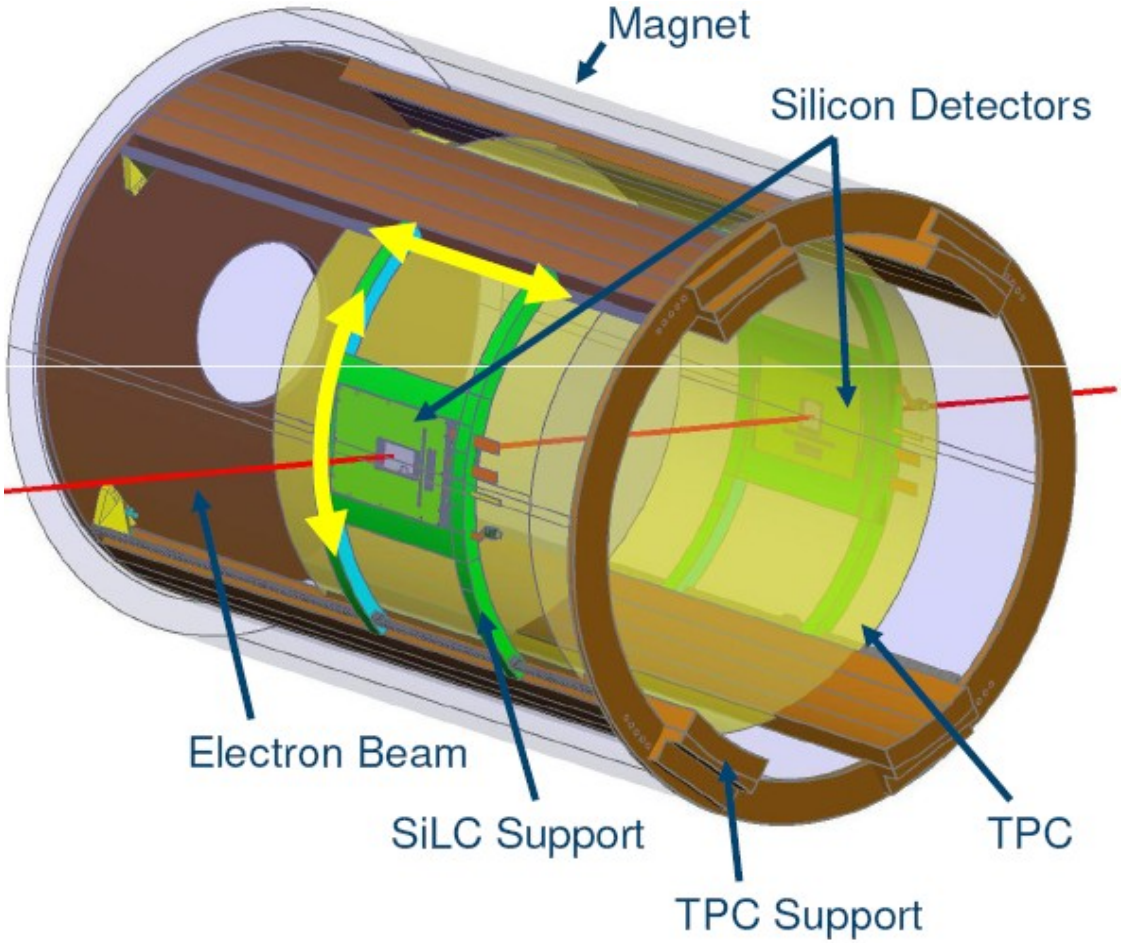
LP Mechanics

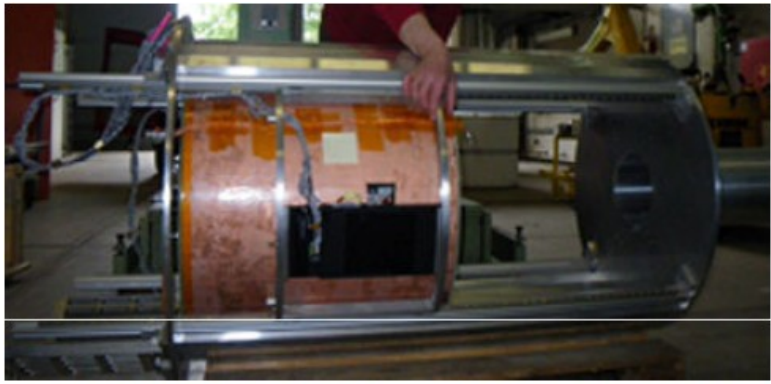


Actuation and Control



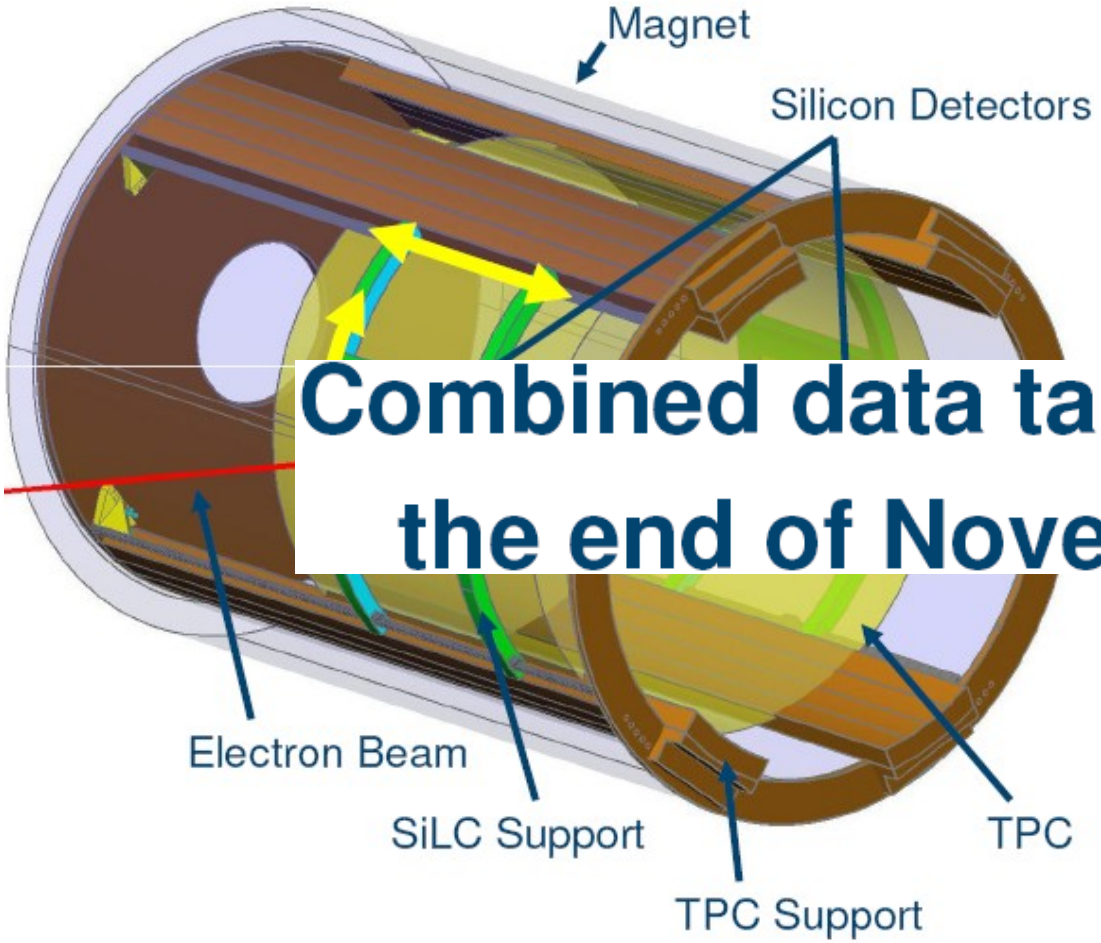
Si Envelope





S. Haensel HEPHY Vienna

Si Envelope



Combined data taking before the end of November 09!

S. Haensel HEPHY Vienna

Status

- Field cage, cathode end plate / alignment wheel, cathodes delivered, one cathode patterned
- 3200 channels of ALTRO electronics in use

  1800 channels of AFTER electronics in use

  640 channels TDC electronics available → noise problems
- TLU trigger system available → synchronization problems

Status

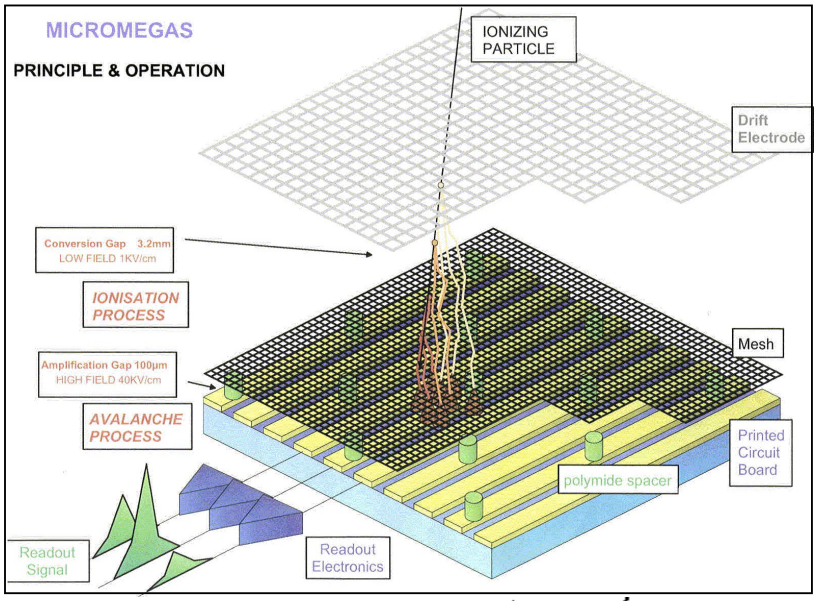
- Gas-/HV-system in use
- Common software under construction
- Infrastructure for SiLC envelope installed
- LP assembled, commissioned and being tested
- LP with three different MPGD operated
- 12 weeks of test beam with LP operation so far → more to come

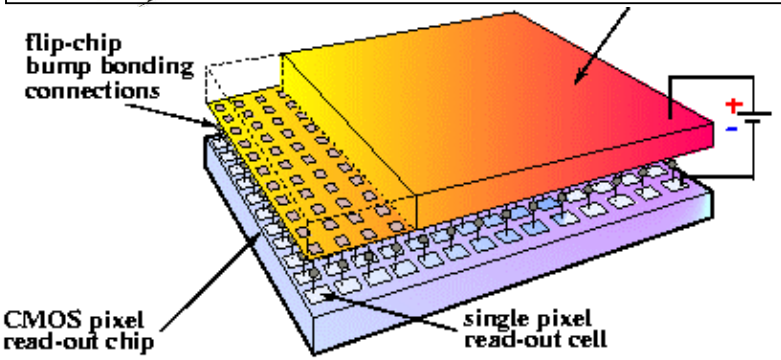
Summary & Outlook

- A Large Prototype of a TPC has been built and is being assembled/tested/commissioned by the LCTPC collaboration
- Two MPGD technologies (with three electronics techniques) are being tested
- Infrastructure for Large Prototype has been constructed
- e^- test beam (DESY) in conjunction with PCMAG (*1T* magnet)
- Preliminary results are looking very promising
- Further test beam campaigns in the current year:
  - Si envelope combined w/ one MicroMegas module
- Further test beam campaigns in the next year:
  - Backplane integrated 10,000 channel readout system, based on ALTRO electronics
  - Seven Micromegas modules with AFTER electronics attached to the modules

Backup Slides

TimePix





- High field created by Gas Gain Grids
- Most popular: GEM and Micromegas

Use 'naked' CMOS pixel readout chip as anode

J. Timmermans
NIKHEF

Readout Electronics

Three-fold readout electronics:

- ALICE based:
  new PCA16 amplifier chip + ALTRO chip (EUDET & LCTPC)
- T2K based:
  AFTER electronics for T2K TPC (CEA Saclay)
- TDC based:
  ASDQ chip + TDC (EUDET & Uni Rostock)

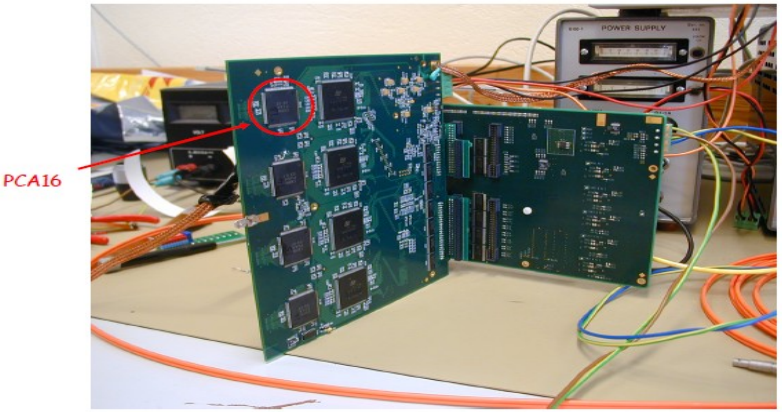
AFTER electronics for MicroMeGAS (resistive anode readout)
ALTRO and TDC based electronics will be hooked to the GEM detector modules (connector compatibility)

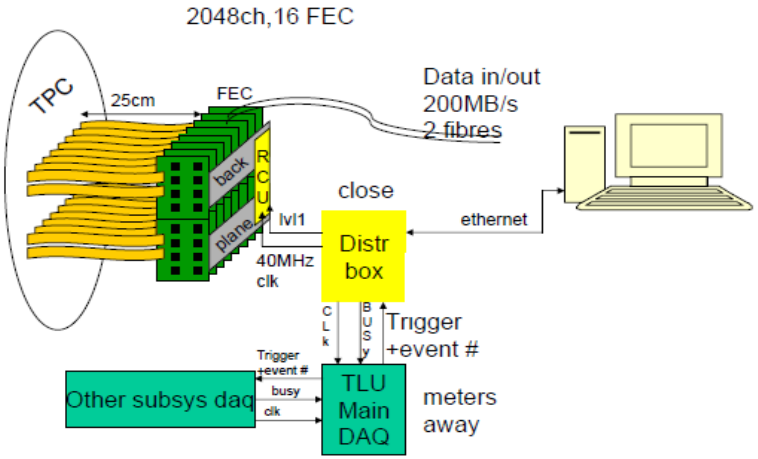
Readout Electronics: ALTRO

PCA16:

1.5 V supply; power consumption <8 mW/channel
16 channel charge amplifier + anti-aliasing filter
Fully differential output amplifier
Programmable features
signal polarity
Power down mode (wake-up time = 1 ms)
Peaking time (30 – 120 ns)
Gain in 4 steps (12 – 27 mV/fC)
Preamp out mode (bypass shaper or not)
Tunable time constant of the preamplifier
Basically pin-compatible with PASA

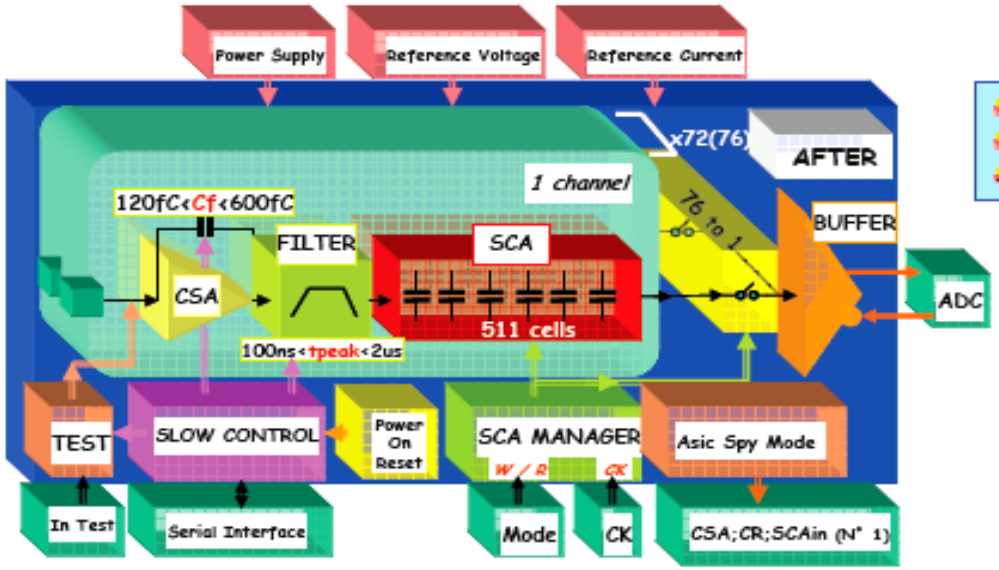
The test set up with a fully equipped front end board





Readout Electronics: AFTER

AFTER Main Features



- No zero suppress.
- No auto triggering.
- No selective readout.

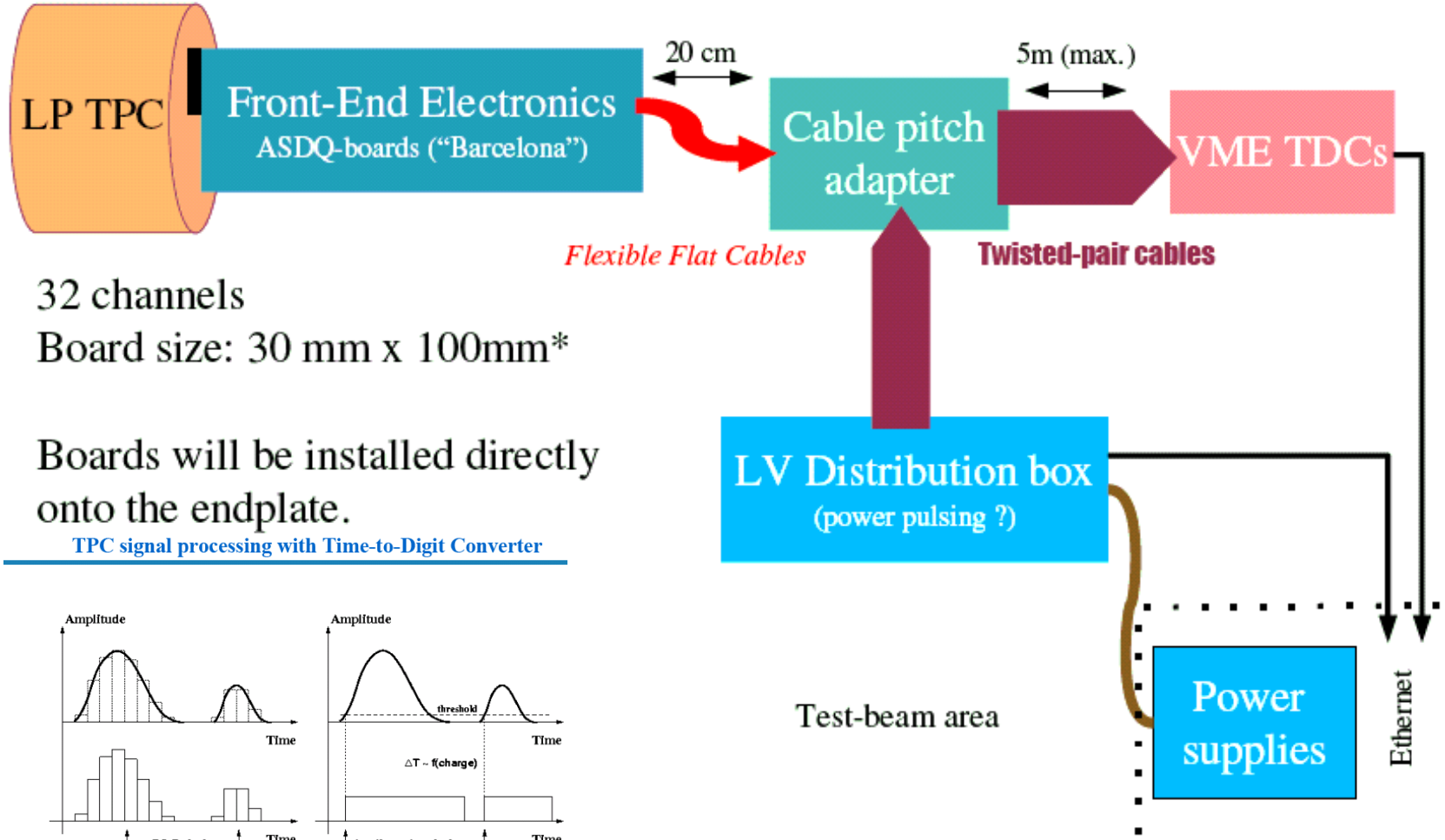
Main features:

- **Input Current Polarity:** positive or negative
- **72** Analog Channels
- **4** Gains: 120fC, 240fC, 360fC & 600fC
- **16** Peaking Time values: (100ns to 2µs)
- **511 analog memory cells / Channel:**
  Fwrite: 1MHz-50MHz; Fread: 20MHz

- **Slow Control**
- **Power on reset**
- **Test mode:**
  calibration or test **[channel/channel]**
  functional **[72 channels in one step]**
- **Spy mode on channel 1:**
  CSA, CR or filter out

LCTPC meeting Oct. 10, 2007 *E. DELAGNES* 4

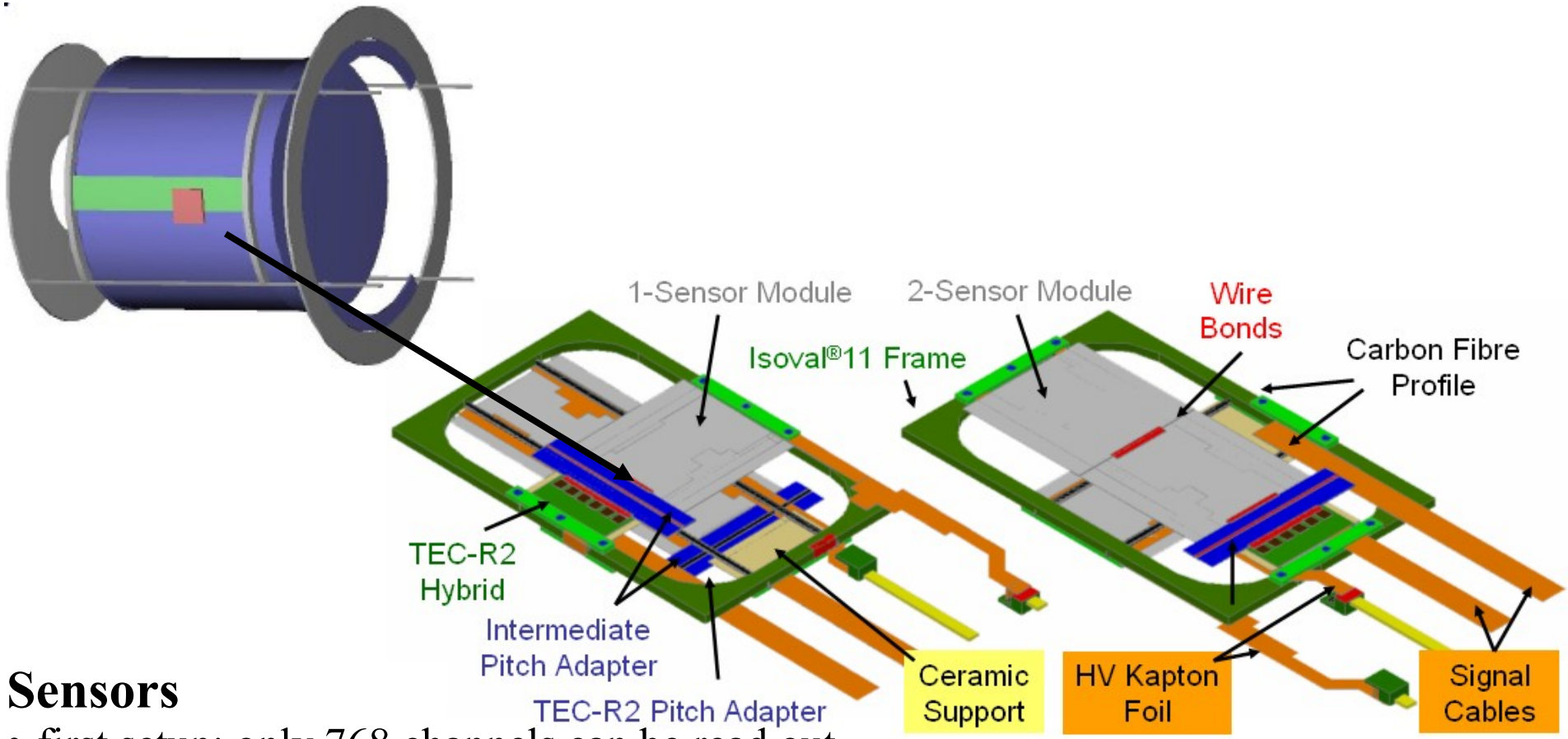
Readout Electronics: TDC



- The time of arrival is derived using the leading edge discriminator.
- The charge of the input signal is encoded into the width of output digital pulse.

A. Kaukher, Univ. Rostock

Si Envelope



Sensors

- first setup: only 768 channels can be read out
  - ➢ the readout sensitive area is reduced to 38.4 x 38.4 mm² (only the intersecting readout area of the two modules on top of each other is interesting)