# R&D advances on Micromegas for a semi-DHCAL

#### M. CHEFDEVILLE LAPP, ANNECY, FRANCE SID MEETING, 28<sup>TH</sup> MARCH 2010, BEIJING

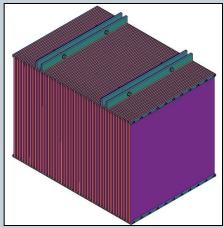


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- Micromegas semi-DHCAL
- Basic performance (analog electronics)
- m<sup>2</sup> prototype (semi-digital electronics)
- Simulation

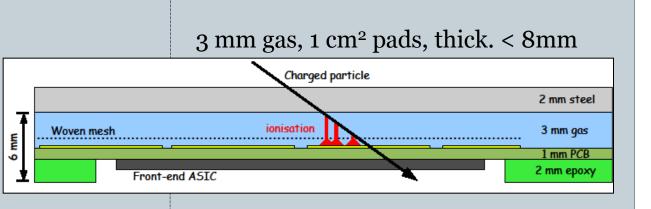
## Micromegas semi-DHCAL

- Proportional mode
- Low working voltage
- Standard gas mixtures
- Robust (Bulk)
- High rate capability
  - 1 m<sup>3</sup> structure



• Sparking

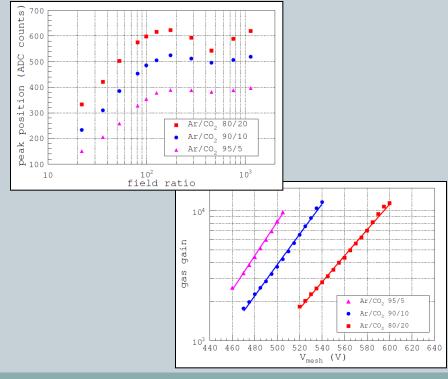
- Depends on gain & rate
- Protection exist (RD51)
- Large area
  Relatively new
  RD51, MAMMA



## **Basic performance (X-rays)**

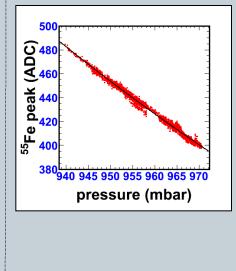
#### • Gas mixtures

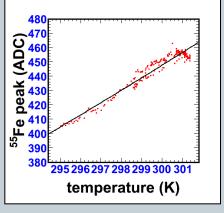
- Collection efficiency
- o Gas gain



#### Ambient parameters

- Pressure
- o Temperature





## **Basic performance (TB)**

80 100120140

threshold (fC)

40 60

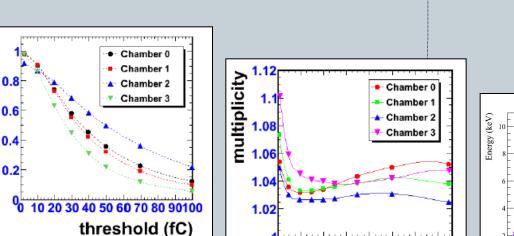
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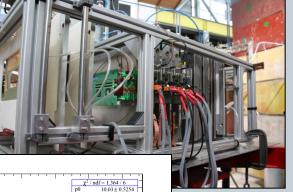
#### • Study with MIPs

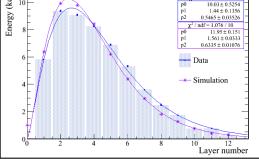
- Efficiency, multiplicity
- Uniformity better than 1 % (100 cm<sup>2</sup>)
- Threshold effect understood

#### • Shower profiles

- o 2 GeV/c electrons
- Hadrons analysis on-going







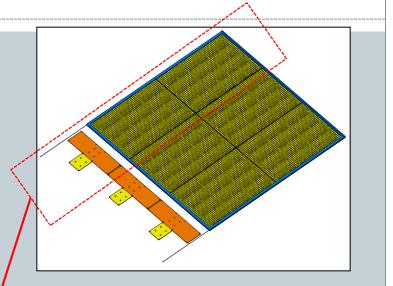
efficiency

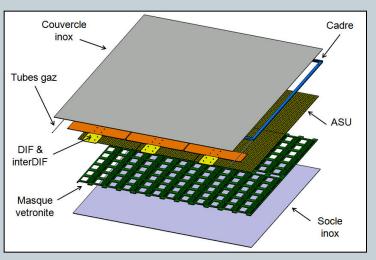
## 1 m<sup>2</sup> prototype

#### • Active Sensor Unit (ASU)

- Front-end electronics embedded on 1 side of PCB
- Pads and mesh on the over side
- Prototype
  - 6 ASU of 48x32 cm<sup>2</sup>
- Before that:
  - Tests with smaller prototypes and different chips

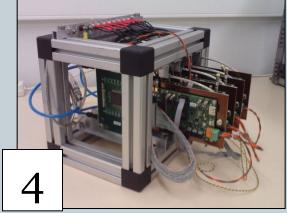


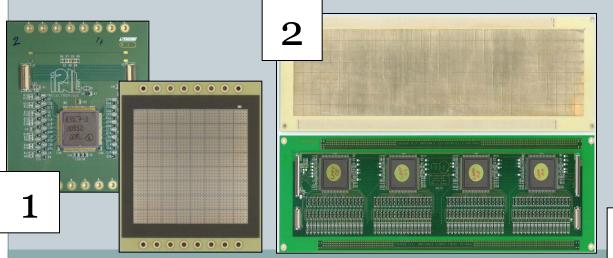


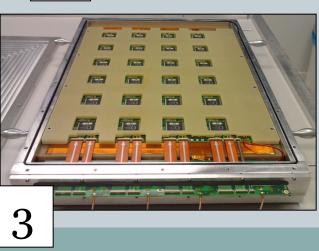


## **Active Sensor Units**

- 1. DIRAC chip, 8x8 cm<sup>2</sup>, 2008
- 2. HARDROC1 chip, 32x8 cm<sup>2</sup>, 2008
- HARDROC2 chip, 48x32 cm<sup>2</sup>, 2009
   DIRAC2 chip, 8x8 cm<sup>2</sup>, 2009







## ASU test in CERN particle beams

#### • DIRAC chip

- Promising results on efficiency
- Not spark-proof yet, protection tests @ LAPP just started

#### • HARDROC 1 & 2

- Too short shaping time w.r.t. Micromegas signals
- Very low efficiency
- Work on a new chip in collaboration with LAL/Omega

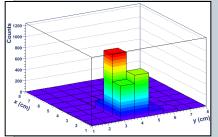
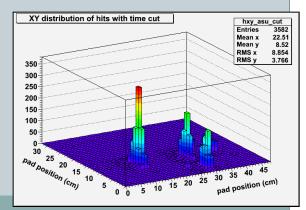


 Image of responses with time out
 Image of responses with

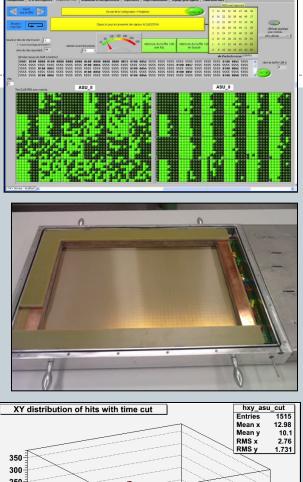


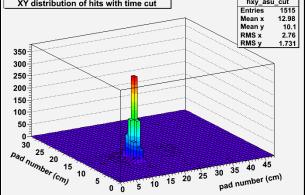
For more details, see Micromegas talk in calo/muon session

# Status and future plans

#### • ASU test on-going

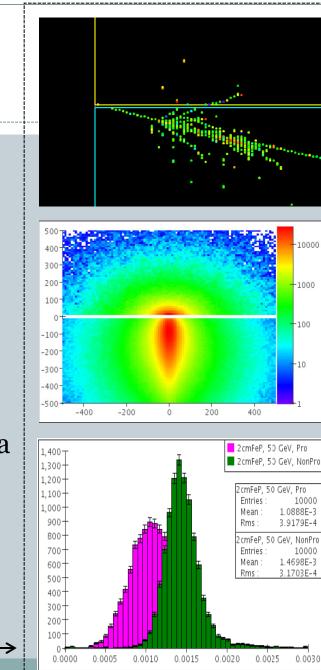
- Measurement of ASIC performance
- Response to <sup>55</sup>Fe X-rays and cosmics
- 4 ASU with HR2, 1 ASU HR2b + 1 dummy Assembly foreseen in April Cosmics tests @ LAPP until June
- 2-3 weeks of beam in SPS/H4 end of June
  - Efficiency, multiplicity, uniformity
  - Spark study (beam intensity)





## Simulation

- Comparison analogue/digital readout for 1 m<sup>3</sup> steel
- Digitization, from GEANT4 energy deposits in gas layers to hits
- Simulation for CLIC: definition of HCAL and small prototype for TB
- TB setup simulation and comparison with data
- Implementation of MICROMEGAS DHCAL in CLIC and SiD detector geometry
- Study of crack effects on HCAL performance



# Conclusions

- Very good basic performance for a DHCAL but strongly depends on electronics
  - HARDROC input stage not optimized for MICROMEGAS signals Work on a new ASIC on-going
  - Several options for spark protection are being investigated
- First 1 m<sup>2</sup> MICROMEGAS prototype available end of April 2010 and ready for beam test at the end of June
  - Equipped with HR2, so limited performance expected However, a lot to learn for next 1 m<sup>2</sup> prototypes
  - Next prototypes should be equipped with a different chip
    - × One plane with DIRAC if spark protection issue solved
    - × Next planes with a new chip, probably resulting from the collaboration between LAL and LAPP

## Acknowledgments

#### the LAPP group

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#### collaborators

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