## Tunnel Electronics for Klystron Cluster System

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### Outline

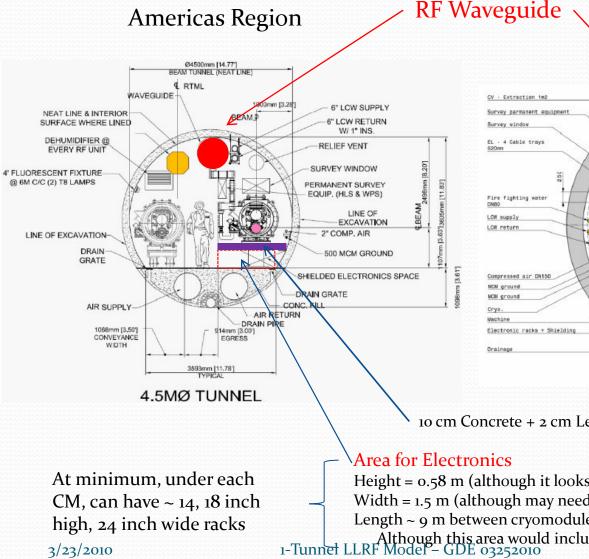
Klystron Cluster Concept Cryomodule Signal Summary Proposed Hardware Solution Chassis and Rack Space Estimates Conclusion

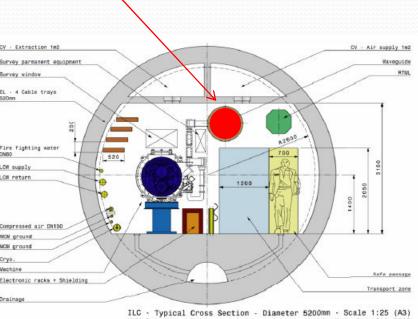
### **Conceptual Design**

- Proposed by C. Adolphsen
  - All klystrons & modulators located in surface building (Klystron Cluster System KCS)
  - All klystrons drive single large circular waveguide
  - Tap-offs every cavity
  - Cryomodules (CM) consist of 8 or 9 cavities (9-8-9 cavity CM's per klystron)
  - Klystron Cluster drives ~99 CM's ~ 1-km waveguide w/ ~33 klystrons
  - In tunnel electronics shielded, LCW temp stabilized

### 1-Tunnel Layout with KCS

C. Adolphsen et al





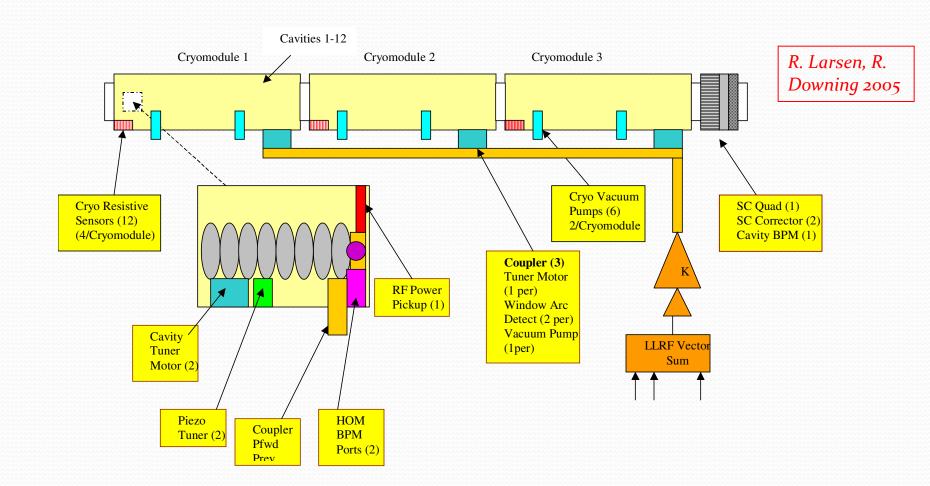
**European Region** 

KLY CLUSTER EUROPE - J.Osborne / A.Kosmicki -November 6th 2009

10 cm Concrete + 2 cm Lead over Electronics

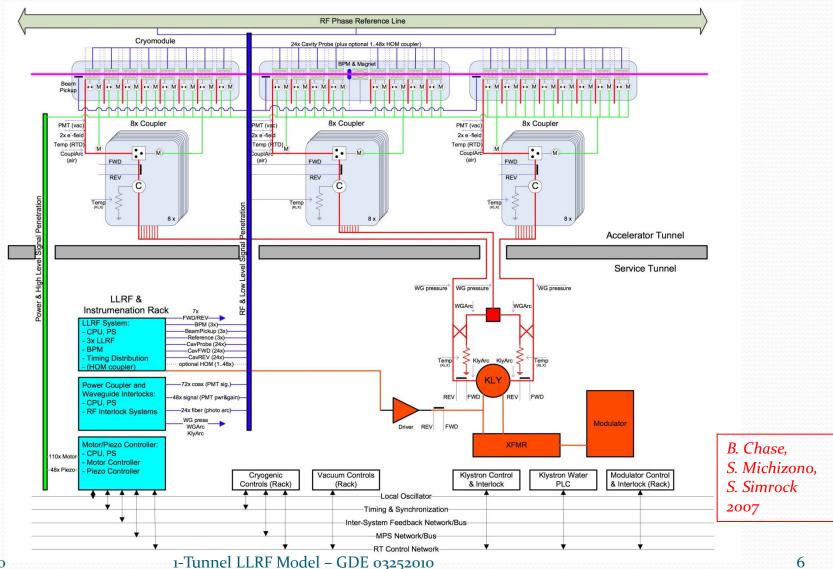
Height = 0.58 m (although it looks like this can be increased by ~ 0.5 m if needed) Width = 1.5 m (although may need a shielding in the front as well) Length ~ 9 m between cryomodule floor supports - see next slide Although this area would include supports for concrete/lead shielding 1-Tunnet LLRF Model – GDE 03252010 4

#### **CM Instrumentation Block Diagram**



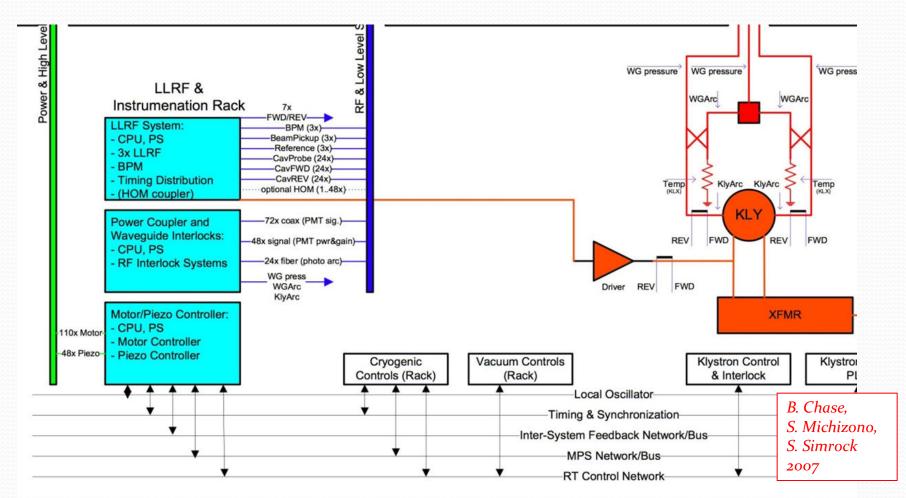
#### 1-Tunnel LLRF Model - GDE 03252010

### 2-Tunnel RF Station w/ 3 CM's



3/23/2010

### **2-Tunnel Signal Details**

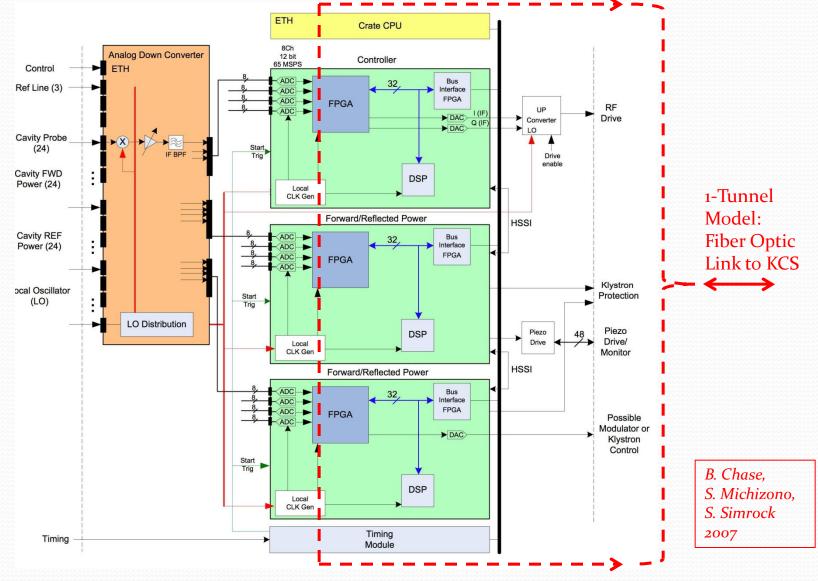


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1-Tunnel LLRF Model - GDE 03252010

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#### 2-Tunnel LLRF ATCA Crate Detail



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1-Tunnel LLRF Model – GDE 03252010

#### CM Instruments Summary- 2 Racks

0	Α	B	C	D	E	F	G	Н		J	K
1	-										
2	Level 1	Level 2	Level 3				Qty / element	Qty / RF Station	Proposed	Cost per Linac	
3									k \$	k \$	
4	Relay Rack #1 - LLRF						1	1			
5	RFI Shielded Relay Rack						1	1	\$ 6.00		
6		Downconverter					1	1	\$ 15.00		
7	1	Vector modulator					1	1	\$ 1.00		
8		Caivty simulator					1	1	\$ 10.00		
9	1	LLRF Craf	te #1 - LLRF				1	1	222		
10			ATCA Crate	(			1	1	\$ 22.00		
11	1		CPU/Crate	Controller	8		1	1	100		
12			32-Channe	LLRF Bo	ard		3	3	\$ 18.00		
13	1		24-Channe	DAC Boa	rd		2	2	\$ 5.00		
14			HOM Board	i			0	0			
15			BPM Board				1	1			
16			Clock Gene	erator & Di	stribution		1	1	s -		
17			Timing Red	eiver	1		1	1	\$ 2.00		
18			Power supp	ly			2	2	s -		
19			Cable mars	halling pa	inel		0	0	s -		
20			Cables/con	nectors to	rack (85)		1	1	\$ 10.89		
21	1			nectors in	ternal to raci	k	1	1	\$ 8.00		
22		Sub-Total							\$ 97.89	S -	
23							1		10 10200 Ph		
24											
25	Relay Rack #2 - Motors & Piezos					1	1				
26	RFI Shielded Relay Rack				1	1	\$ -				
27		1000000000	1	1996			- 18i - 1	300	s -		
28		Subrack-	Piezo motor	drives			1	1	\$ -		B. Chase,
29		3U Eurocrate				1	1	\$ 2.00		S. Michizono,	
30			Power Supply (48V)				2	2	\$ 2.00		S. Simrock
31			8-channel piezo driver				6	6	\$ 2.40		
32			Cable marshalling panel				1	1	\$ 0.50		2007
33	Cables/connectors					1	1	\$ 0.83			
34		Sub-Total							\$ 7.73	S	
35		out-iotal							•		

### **1- Tunnel Electronics Summary**

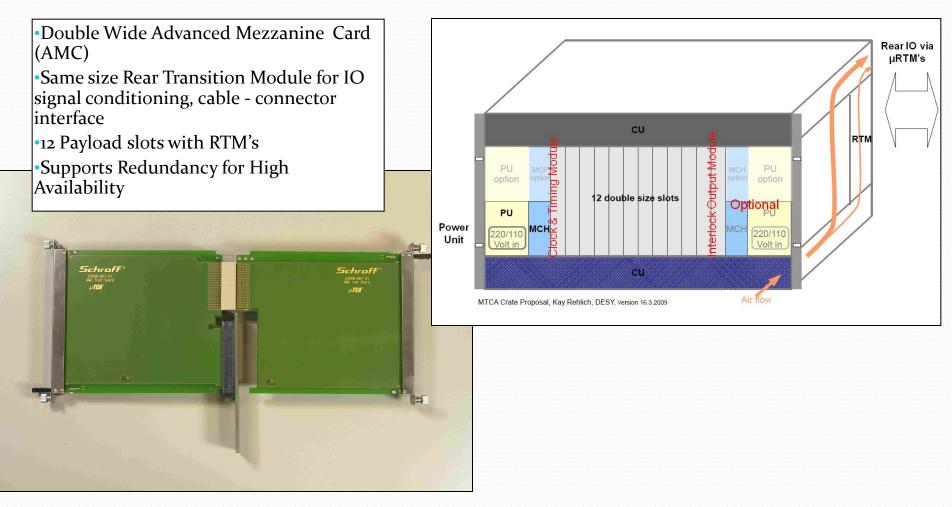
#### Per Cavity

- Cavity voltage probe readout (1)
- Piezoelectric tuner drivers & readout(2)
- Blade tuner driver motor & readout(1)
- Window arc detect PMT readout (2)
- Directional coupler FE, RE readout (2)
- Phase Shifter motor driver & readout (1)
- Power coupler (1)

#### **1-Tunnel Electronics Summary 2**

- Per Cryomodule (CM) (8-9 cavities)
  - Above components (x8-9)
  - Probe down-conversion & digitizing channels (8-9)
  - Vector sum controller per CM
  - Beam position monitor readout (1)
  - SC Quad power supply & protection (1)
  - Vacuum pump power supplies (2)
  - Helium monitoring & control (1)
- Per Girder of 3 Cryomodules
  - Above x<sub>3</sub>

# Proposed Platform: MicroTCA New Standard for Physics



#### 1-Tunnel LLRF Model - GDE 03252010

#### Industry Demonstration Unit



•First 6-Slot Test Prototype Crate from Schroff

•Double-Wide Application Card with Rear Transition Module

•Production Unit will be 12-slot

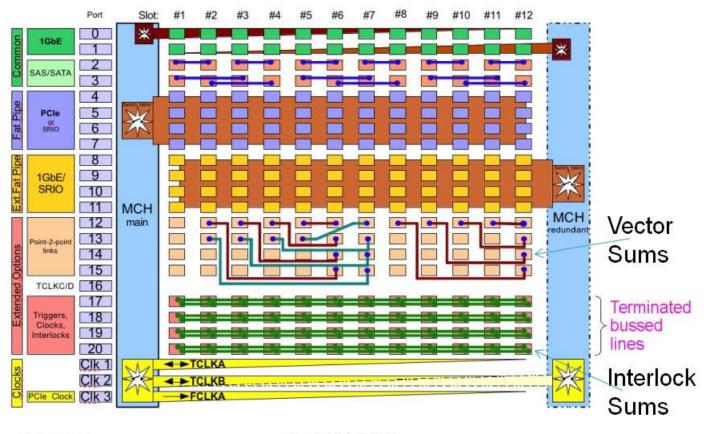
•Supports redundancy, rear cable entry, managed platform, module hot swap

•Quotes received for 12slot units.

Courtesy Schroff, DESY

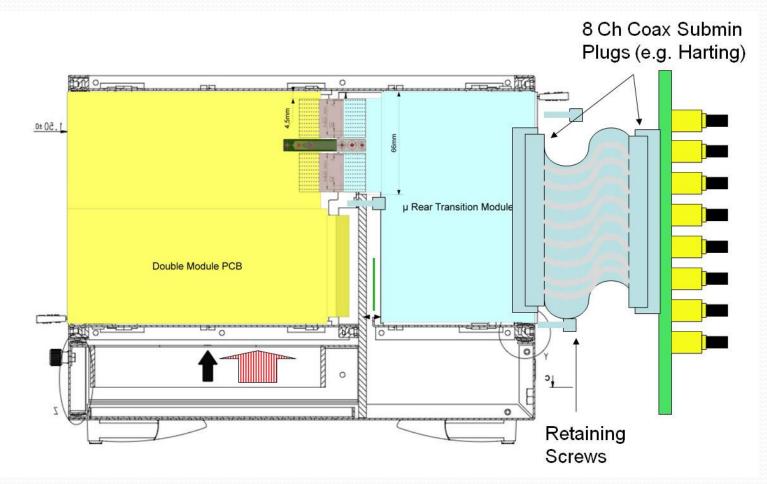
### MicroTCA Backplane w/ Vector Sum, Interlock Sum Support

µTCA Port Usage 4Physics, Proposal



3/23/2010

#### **µRTM Connection Concept**



#### Harting Multi-Coax

#### MULTI-COAXIAL CONNECTOR SYSTEM MINI COAX

The HARTING multi line Mini Coax connector system for board-to-backplane RF interconnection includes connectors for press-in technology with 1 to 10 coaxial lines. The Mini Coax connector range close transcriver of analogue signals in various applications like cellular base transcriver stations (BTS), repeaters and passenger entertainment system at radio frequencies up to 2.5 GHz per line at 50 0 hm. Moreover, these connect and rugged connectors provide a 6 Sigma mating reliability thanks to the closed-entry contact design. The compact size of Mini Coax modules (minimum pitch of RF lines is 4.4 mm), combined with excellent RF-performance, makes this connector system especially suitable for high-end equipment.

The twin modules are available in metric sizes of 1.00, 1.25 and 1.50 SU (SU = System Unit = 25 mm) for both cable assemblies an PCBs with 2 to 10 coaxial lines, as well as a single row version with 1 to 3 coaxial lines.

HARTING offers customised cable assemblies including adaptor cables to the most popular discrete coaxial contacts such as SMA, SMB, BNC, N-Type, etc. A complete range of accessories and tools supports the wide product range.

#### SPECIFIC FEATURES OF THE PRODUCT RANGE



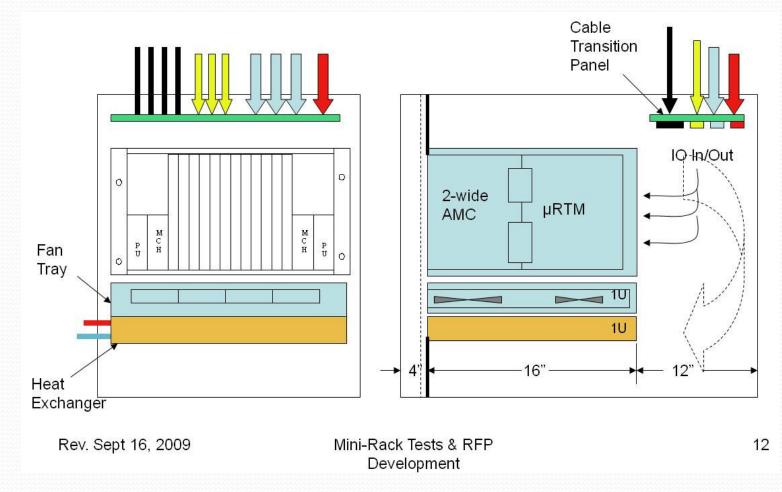


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MARTING

#### Air-Water Cooled Mini-Rack (e.g.)

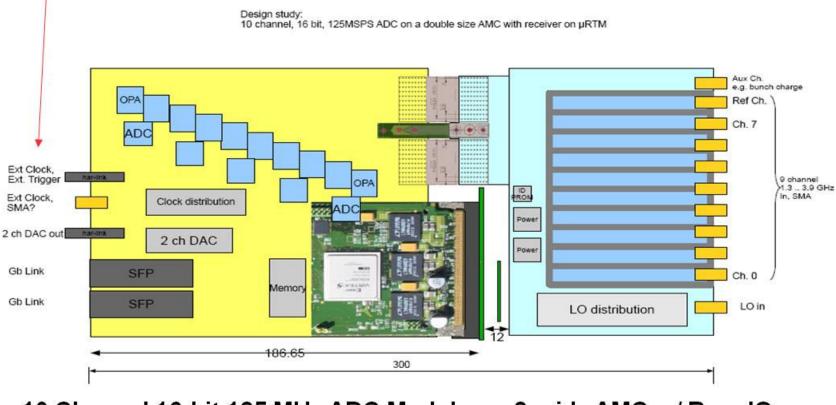


#### 1-Tunnel LLRF Model - GDE 03252010

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#### Generic ADC w/RF Down-Converter

Note – Clocks & triggers will be distributed via Timing module driving extended options region of AMC backplane (RL)



#### 10 Channel 16-bit 125 MHz ADC Module on 2-wide AMC w/ Rear IO

#### **Overall Packaging Concept**

#### ADC Conversion

- Design applications to mate with *generic* ADC's on 2-wide AMC via *application-specific* µRTM's
- 100 MS/s, 10 MS/s, 1 MS/s, 100kS/s speed ranges, 16 bits
- AMC's have FPGA's for all real-time operations
- DAC Outputs
  - Fast outputs for RF drive feedback (same card as fast ADC)
- Fast Digital Outputs
  - Needed for klystron –modulator interlocks for arc-detect located in tunnel
- Slow Monitoring and control (e.g. motors)
  - Commercial Industry Pack modules mounted on AMC cards
  - All IO routed via RTM's
- Chassis
  - Redundant power, MCH (Controller Hub) options
  - Timing as needed via locally installed module in each crate
  - Local controller sets up, directs traffic
  - All external communications by Ethernet
- Rack
  - Install applications in µTCA 12-slot chassis
  - Mount chassis in short rack installed *horizontally* under each CM unit to minimize lengths, standardize cable runs
  - Racks are sealed, air-water cooled as in Baseline proposal

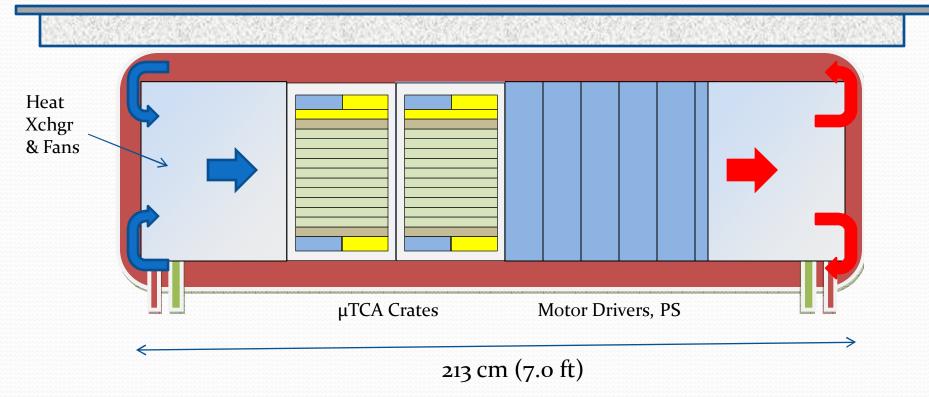
#### 1-Tunnel LLRF Model – GDE 03252010

#### AMC-µRTM Boards per Cryomodule

Item	Chan.	Function	AMC RTM	Channels/Unit	Extend	Rack Ht
Probes	9	125 MS/s Vc	1	10 @ 125 MS/s)		
PMT's	18	10 MS/s Intlks	2	10@ 10 MS/s		
BPM	4	125 MS/s	1	10@125 MS/s		
Piezos	18	10MS/s DAC	5			
Motors	36	Tuners, Couplrs	0	8	5@3U	15U
FE/RE	18	10 MS/s Intlks	2	10@ 10 MS/s		
Intlk Sum		1 per chassis	2			
Quad Supply	1	1 per CM			1@ 1U	1U
Cntrlr		1 per chassis	2			
Timer		1 per chassis	2			
Chassis		2 per CM		12 AMC cards	2@9U	18U
Rack 3/23/2010		1 per CM 1-Tunnel LLRF Model	17 min - GDE 0324	52010	48U (213 cm)	34U Min. for Payload

### **Crymodule Horizontal Rack**

#### Lead-Concrete Shielding



### **Concluding Remarks**

- All estimates of numbers of cards, chassis and rack space are *preliminary*
- Approximately 2 m of standard rack space is needed per Cryomodule
- The height of the CM's may have to be increased slightly to allow adequate room for cabling & cooling channels
- The rack may have to be slightly longer (taller) to accommodate redundant heat exchangers
- Prototype crates & cards are on order from which better estimates can be made. In general the µTCA chassis and modules are more compact.
- The estimates for motor drivers are based on a known catalog unit but the piezo and quad drivers are guesses.
- For completeness a study should be done of the entire system concept to verify the assumptions of the architecture down to the card level.
- Costs should be comparable with the Baseline since only slight changes in partition and function are assumed.

### Acknowledgment

 Brian Chase and John Carwardine provided very useful information from the cost analyses done for the Baseline Controls and LLRF Models.