Silicon tracking test infrastructures

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These teams propose to build a set of tracking test infrastructures based on the state of the art Silicon strips sensors, Front End Electronics, related DAQ system and alignment associated system, to be adapted to the specifics needs of a Si-tracking/calorimeters test infrastructure and a Silicon/gaseous tracking infrastructure. This will be based on the experience and advances obtained both in the SiLC R&D collaboration and the EUDET-FP6 project [1].

One test infrastructure will consist of several layers of false double sided Silicon strips detector adapted to the request of combined test infrastructure with the calorimeters. The other test infrastructure will be coupled to the TPC test infrastructure and will be an extension of what is presently developed in EUDET-FP6 programme.

1) *The Si layers for the tracking/calorimeters infrastructure*

A set of 4 false double sided Silicon strips detector system will be prepared to be set in front of the calorimeters. The dimension of the Silicon tracking detectors will be adapted to the dimensions required for this test infrastructure in order to cover the overall active surface in front of the calorimeters *(input needed from Felix et al.)*

The Silicon strips will be made of the state of the art Silicon strips sensors, i.e.: 6'' (or possibly 8'') wafers, at most 300 µm thickness, 50 µm readout pitch and including an intermediate floating pitch.

This will constitute the baseline strip sensors used to build this infrastructure.

A friendly aligned version will be also included in this framework, based on IR transparent sensors. There are already commercially available such strip sensors, but the goal is to use if available new IR sensors developed in the previous EUDET project [2] with higher transmittance. An active edge option will also be used when available [3].

The total number of channels to be read out are anticipated to be of the order of several ten thousands, with about 2000 per modules. The signal processing and readout on the detector will be achieved with the latest version of the chips presently developed in the EUDET project [4]. This is a mix-mode analogue and digital micro-electronics system, based on deep sub micron electronics (currently CMOS 130nm) most probably in 90nm CMOS version. This micro-system includes a low noise and long shaping time very front-end part, pulse-height reconstruction and time stamping, zero suppression, full digital control (highly fault tolerant, flexible and entirely programmable), and power cycling. In the current 130nm version each chip handle 128 channels, the new 90nm version will include 256 channels per chip, thus 7 chips will be needed to read one module.

The connection and cabling of the chips on the modules will be done by wiring and possibly another technology if or when available.

The DAQ system developed in the EUDET framework is linkable to the overall DAQ system both from the software and the hardware points of view.

2) *The Silicon tracking coupled to the gaseous tracking: tracking infrastructure*

The same strip and related electronics technology will be used for equipping the test infrastructure coupled to the gaseous tracking. What is different of course is the design of the modules to be used in this test infrastructure as well as the support structure. This has to be defined between the two tracking technologies.

Also included in this framework is a dedicated alignment system to align two different sub-detectors and based on a system with Silicon pixel detectors and associated processing electronics [5]. Two layers of false single sided strip detectors will be placed on each side of the gaseous detector infrastructure.

3) List of needed items:

Item	Si-tracking/calorimetry	Si-tracking/gaseoustracking
Strip sensors		
FEE chips		
Connection/cabling		
Faraday cage/cooling(?)		
Si-DAQ hardware/softw.		
Alignment systems: - IR sensors + laser - Inter-sub detectors		
Support structures		
Integration (3D table..)		
Connection to overall DAQ		

Details for each infrastructure: to be define in each application (= each sub –detector: gaseous tracker and calorimeters)

This has to be defined in function of the Silicon/calorimeter and the Si-gaseous tracking infrastructure specific needs.

4) Requested funding

tbd

Bibliography:

[1] Refs on SiLC R&D and Si tracking (SiTRA-JRA2) in the EUDET project
[2] Ref on IR transparent sensors
[3] Ref on active edge strip technology
[4] Ref on FEE chip (NIMA publis)
[5] The ILD-LOI