IP Intra-train FB System at ATF2

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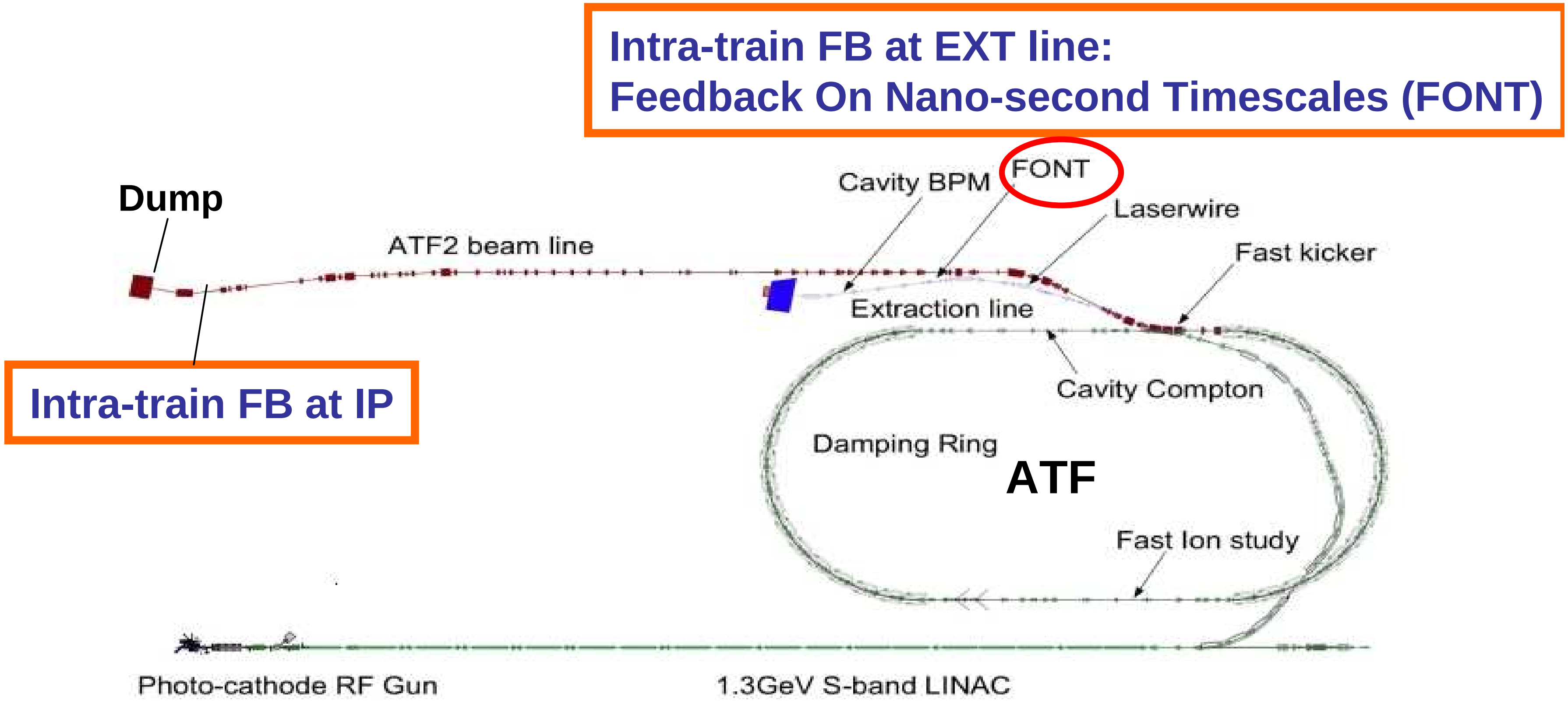
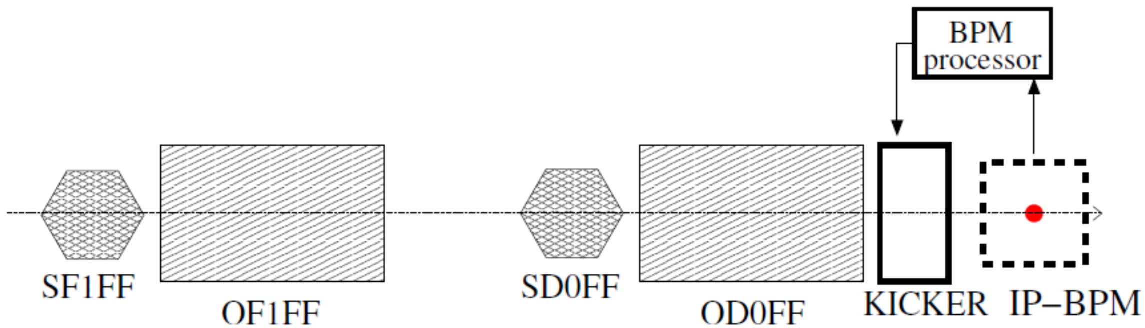
Introduction:
Beam-based intra-train FB systems at ATF2

- ATF-ATF2 schematic layout



Schematic intra-train FB system at IP

- To combat residual jitter at the IP
- Crucial for phase 2 goal (~ 5% σ^{*}_{y} ≈ 2 nm beam stability level)



Key components:

Cavity IP-BPM **(Y. Honda et al.)** with nanometer level resolution: up-to-date resolution measurements ≈ 8.7 nm. Further improvement is necessary

Stripline kicker located upstream of the IP-BPM

Latency issues

- Irreducible latency:
  - Time-of-flight from kicker to BPM: $t_f \approx 3$ ***ns*** (if distance kicker – BPM =1 m)
- Reducible latency:
  - IP-BPM signal processing: $t_p \approx 20$ ***ns***
  - Transport time of the signal BPM-kicker: $t_s \approx 5$ ***ns***
  - Digital FB processor: $t_{FB} \approx 77$ ***ns*** (typical value from FONT4)
  - Response time of the Amplifier + kicker: $t_k \approx 38$ ***ns*** (typical value from FONT4)
- TOTAL latency: $t_f + t_p + t_s + t_{FB} + t_s = 143$ **ns**. Enough if operating trains with >~145 bunch separation !

Possibility to reduce latency with an analogue FB processor:

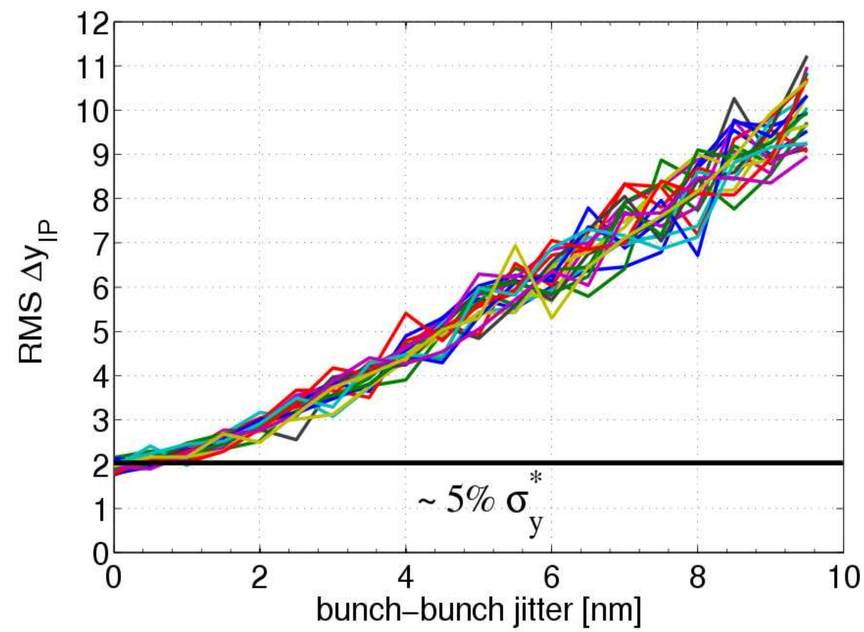
Response time of the Amplifier + kicker: $t_k \approx 5$ ***ns*** (demonstrated with FONT3)

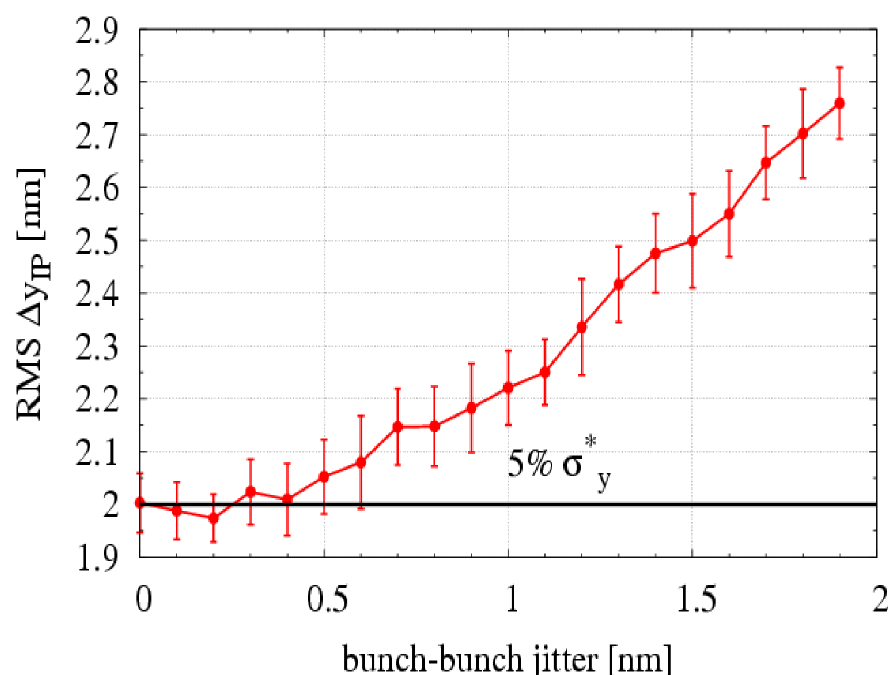
Therefore, possibility to correct trains with ILC-like bunch separation ~140 ns

Simulation Study

Bunch-to-bunch jitter tolerance

- Simulation using a PI control loop
- Considering a set of pulse offsets in the range [0,100] nm
- Scan RMS y position at the IP vs vertical position bunch-bunch jitter
- Each point is the average over 100 pulses (3 bunches per pulse)
- IP-BPM resolution ~ 2 nm





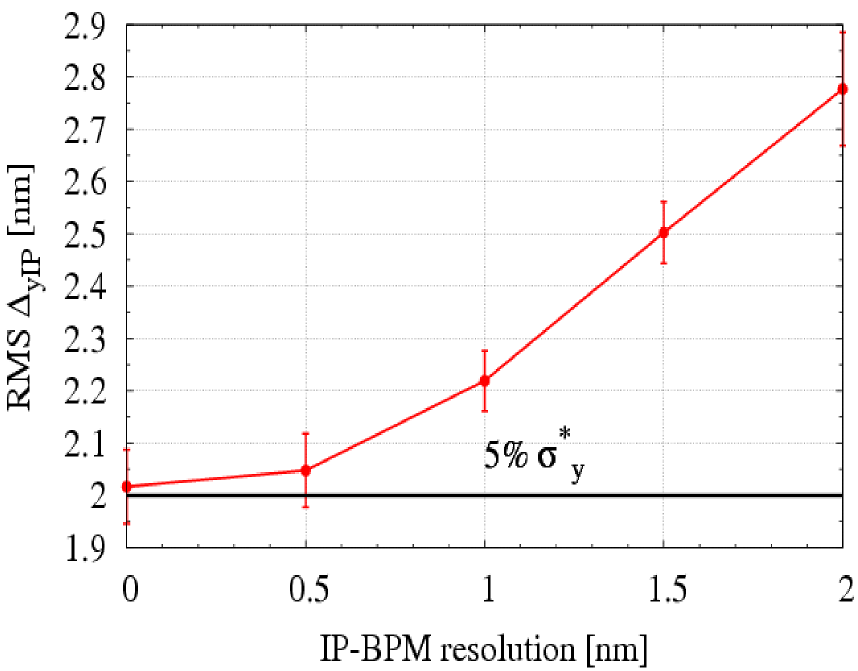
Tolerable IP bunch-to-bunch jitter ~< 0.4 nm $\xrightarrow{R^{-1}}$ ~< 12 nm at extraction
(assuming only y,y' backward propagation, no x-y coupling effects)

Simulation Study

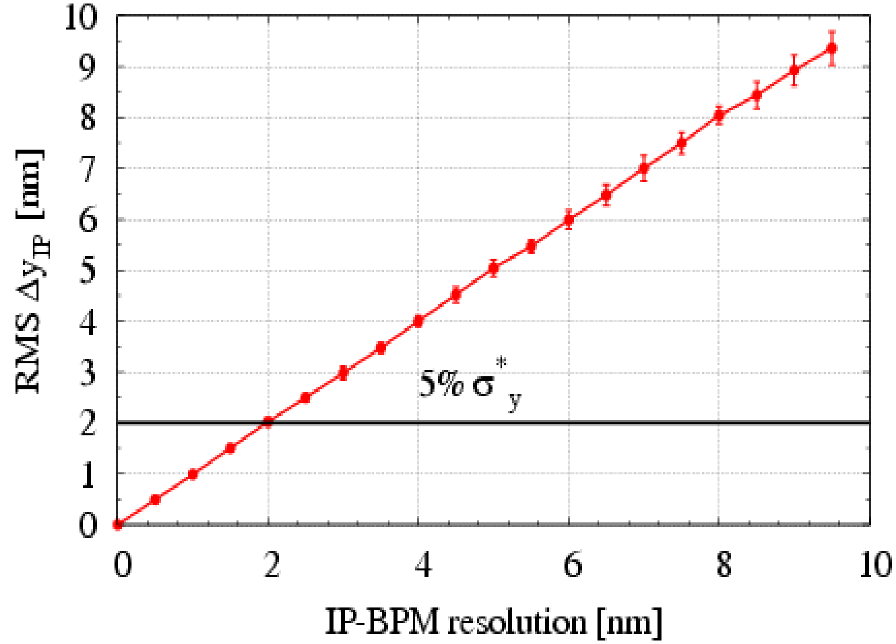
IP-BPM resolution

- Scan RMS y position at the IP vs IP-BPM resolution

Assuming 2 nm bunch-to-bunch jitter at the IP

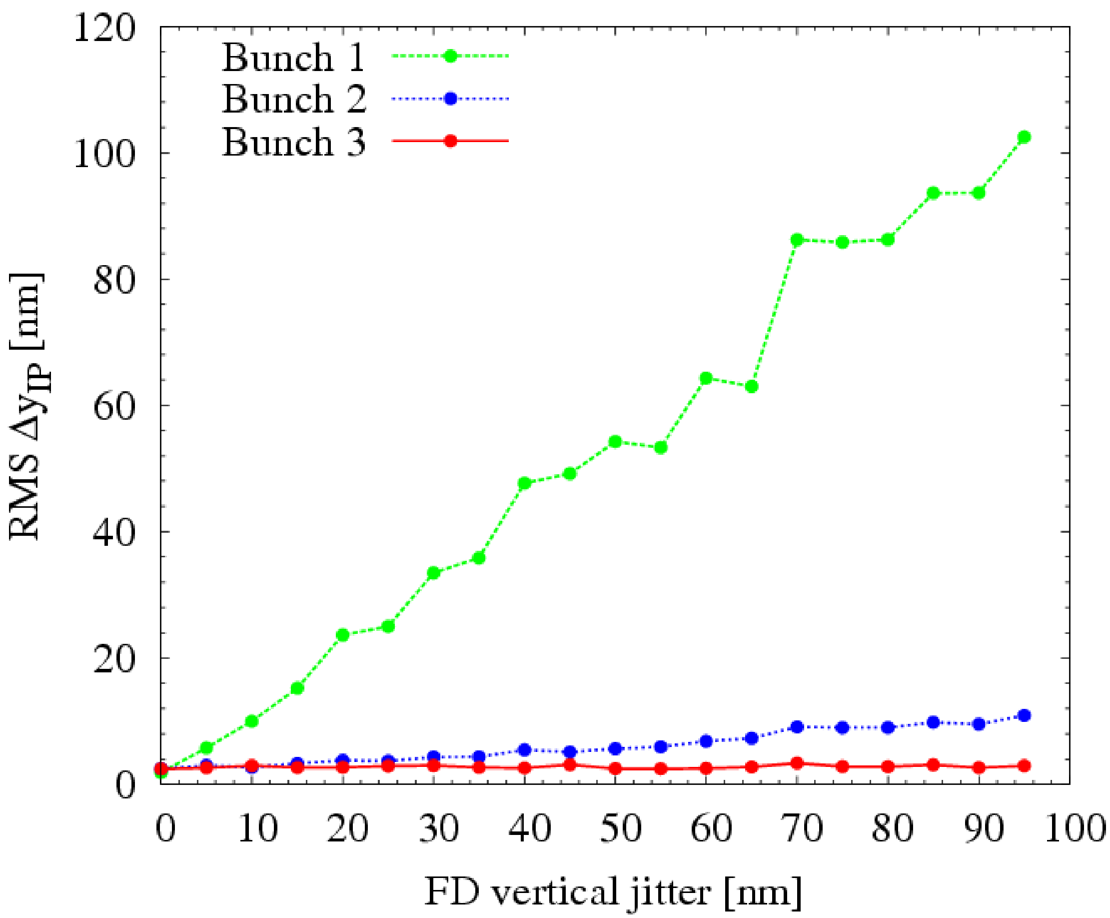


Assuming 100% bunch-to-bunch correlation



Simulation Study

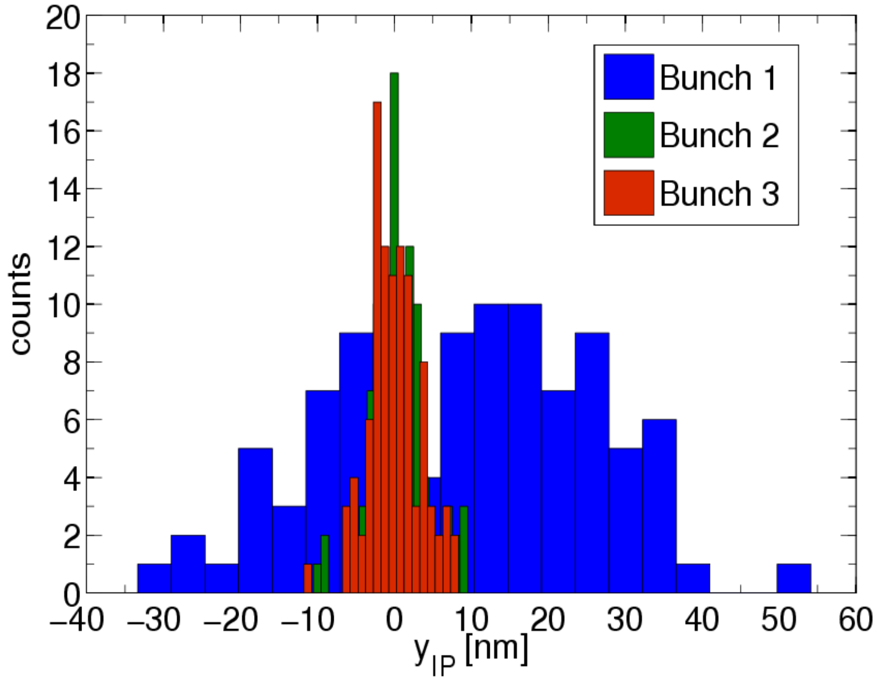
FD vertical jitter tolerance



3[rd] bunch: good correction rms y_{IP}< 5 nm for ~< 100 nm FD vertical position jitter

The IP intra-train FB system can significantly help to relax the FD jitter tolerance

Simulation study



Full beam tracking considering 100 pulses with:

- Initial 40% σ_y pulse-to-pulse jitter at the entrance of the EXT line (≈ 464 nm)
- 4% σ_y bunch-to-bunch jitter

Bunch 1: rms y_{IP} =19.06 nm
Bunch 2: rms y_{IP}=3.628 nm
Bunch 3: rms y_{IP}=3.414 nm

Some items to be addressed toward ~ nm beam level stabilization at the IP

- Define exact characteristics of the kicker. In principle a 10 cm stripline BPM can be used
- Define exact amplifier characteristics
- Improvement of IP-BPM resolution < 8 nm (~ 2nm will take important efforts)
- For good intra-train FB corrections with RMS y_{IP} ~ 2 nm, bunch-to-bunch jitter < 0.5 nm at the IP, which means almost perfect bunch-to-bunch correlation
- Improvement of the quality and stability of the multi-bunch trains