Status of the TimePix/Ingrid module for the Large Prototype

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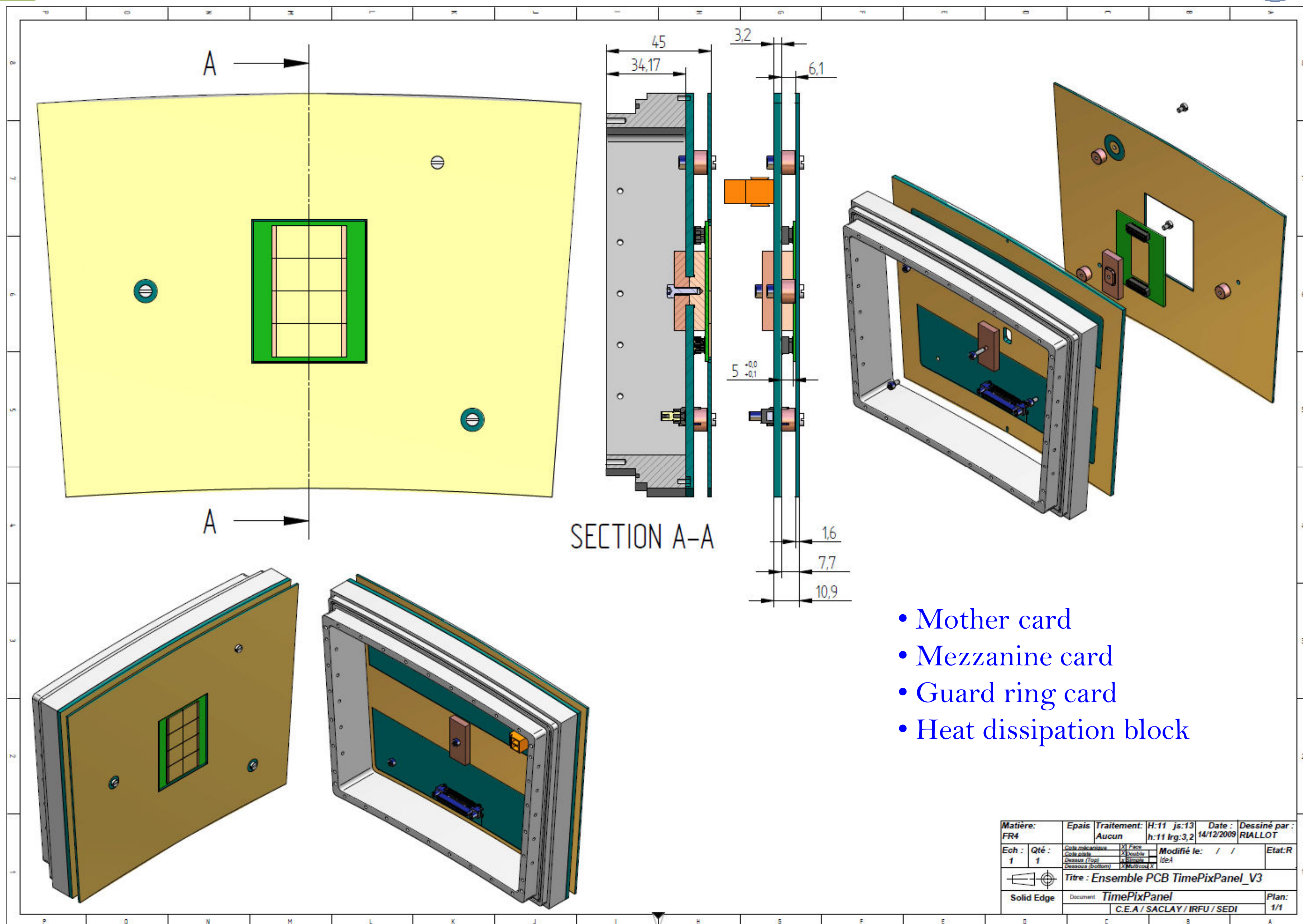
irfu
cea
saclay

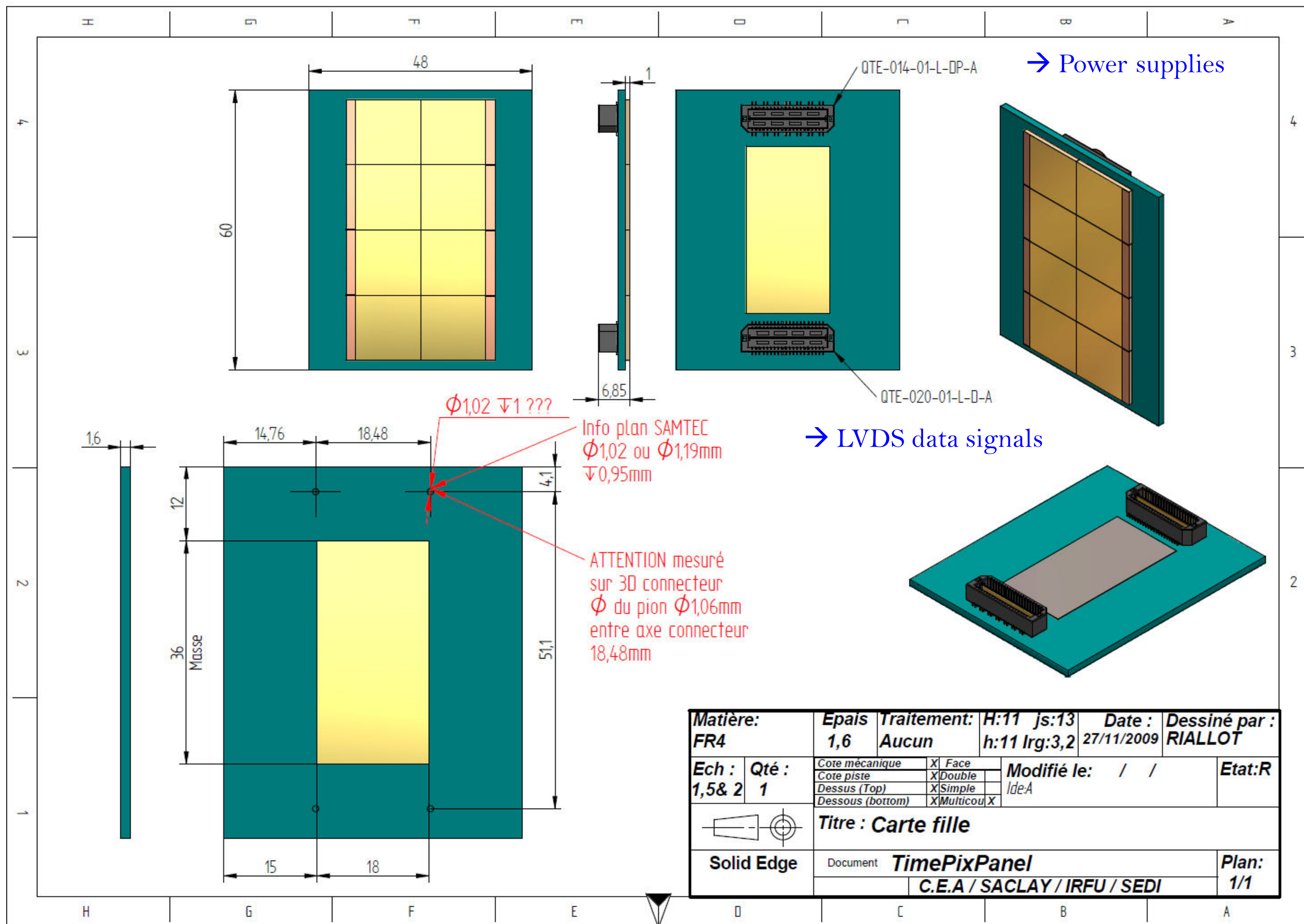
LCTPC WP Phone meeting 97
January 7, 2010

2×4 TimePix/InGrid matrix module for the LPTPC



- Mother card
- Mezzanine card
- Guard ring card
- Heat dissipation block

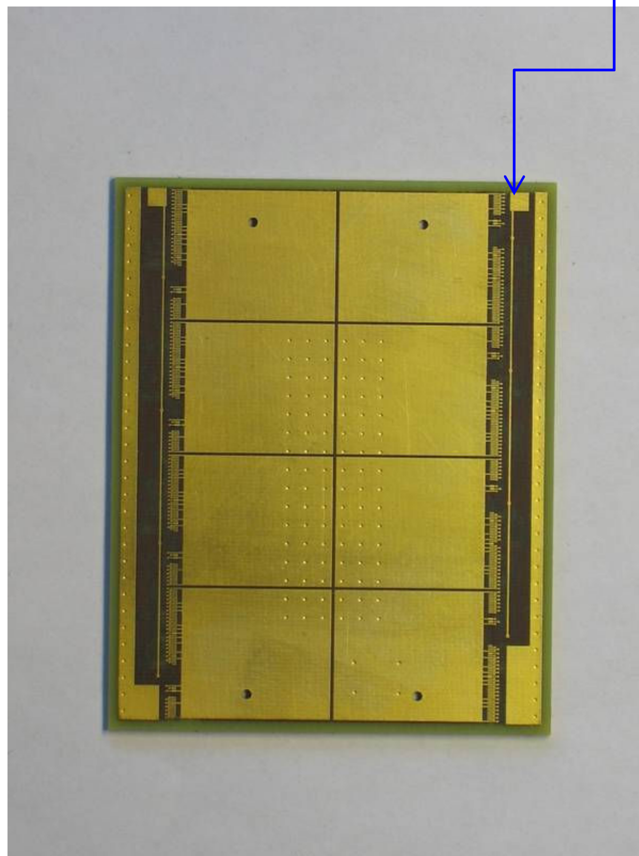
Mezzanine card for the 8-chip matrix

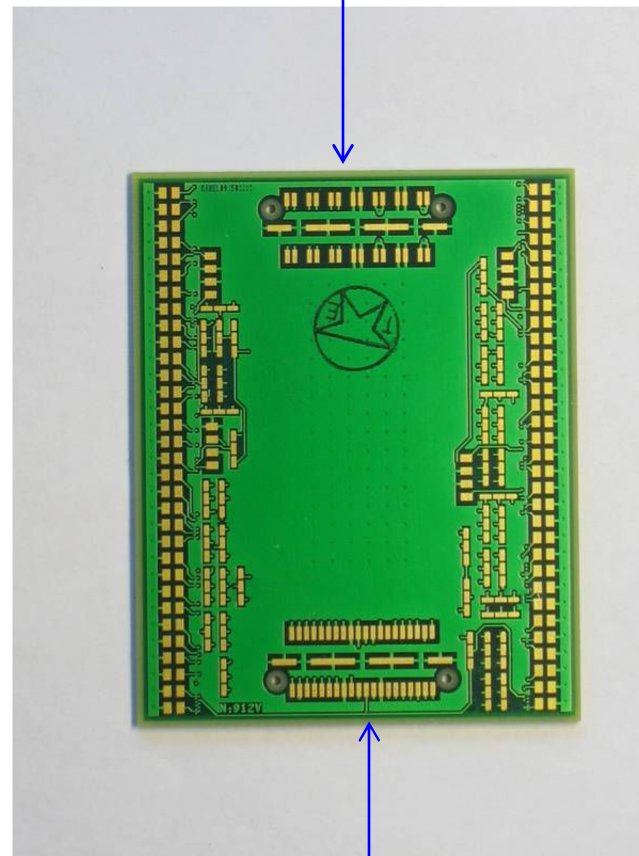


Mezzanine card

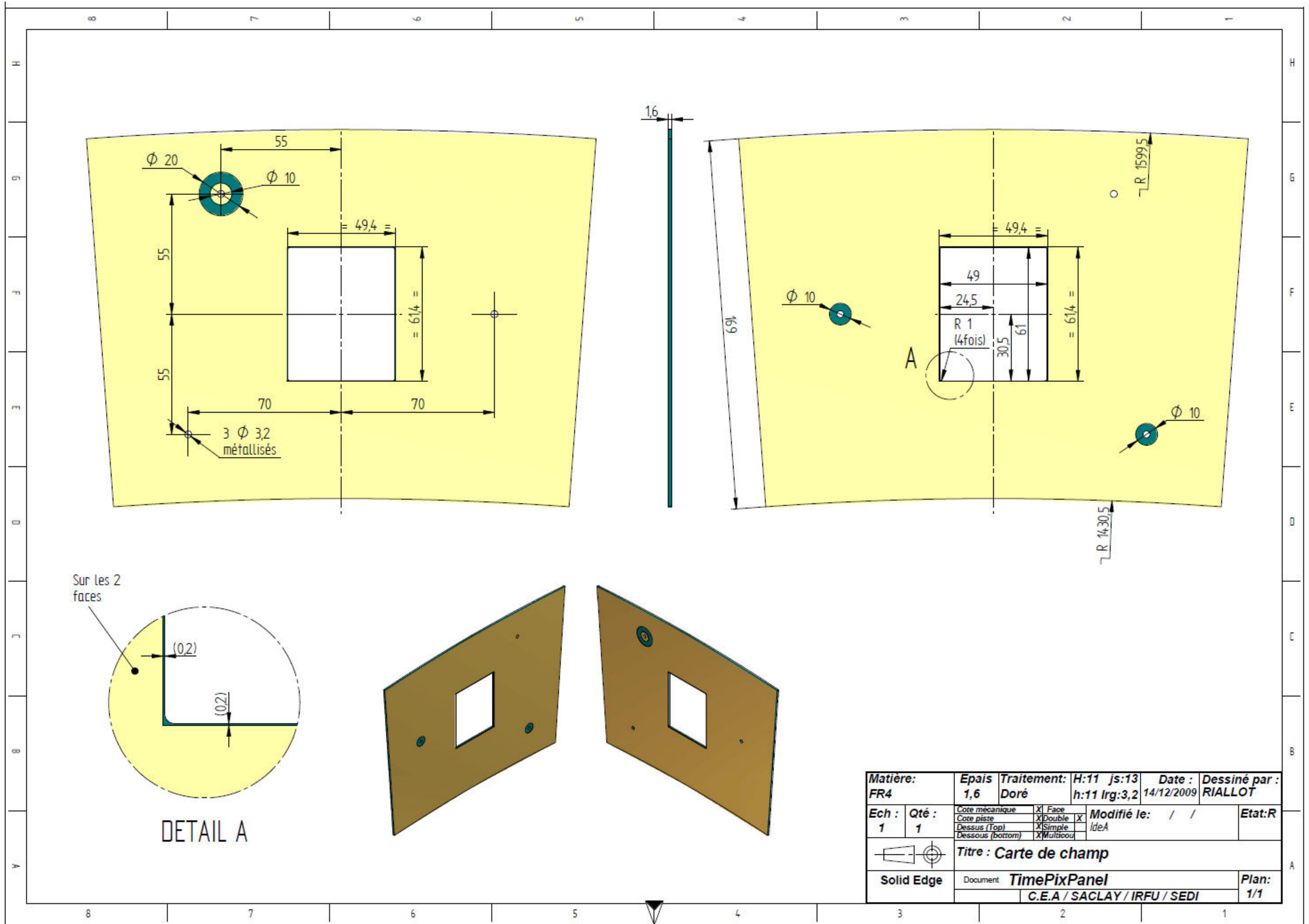
Top

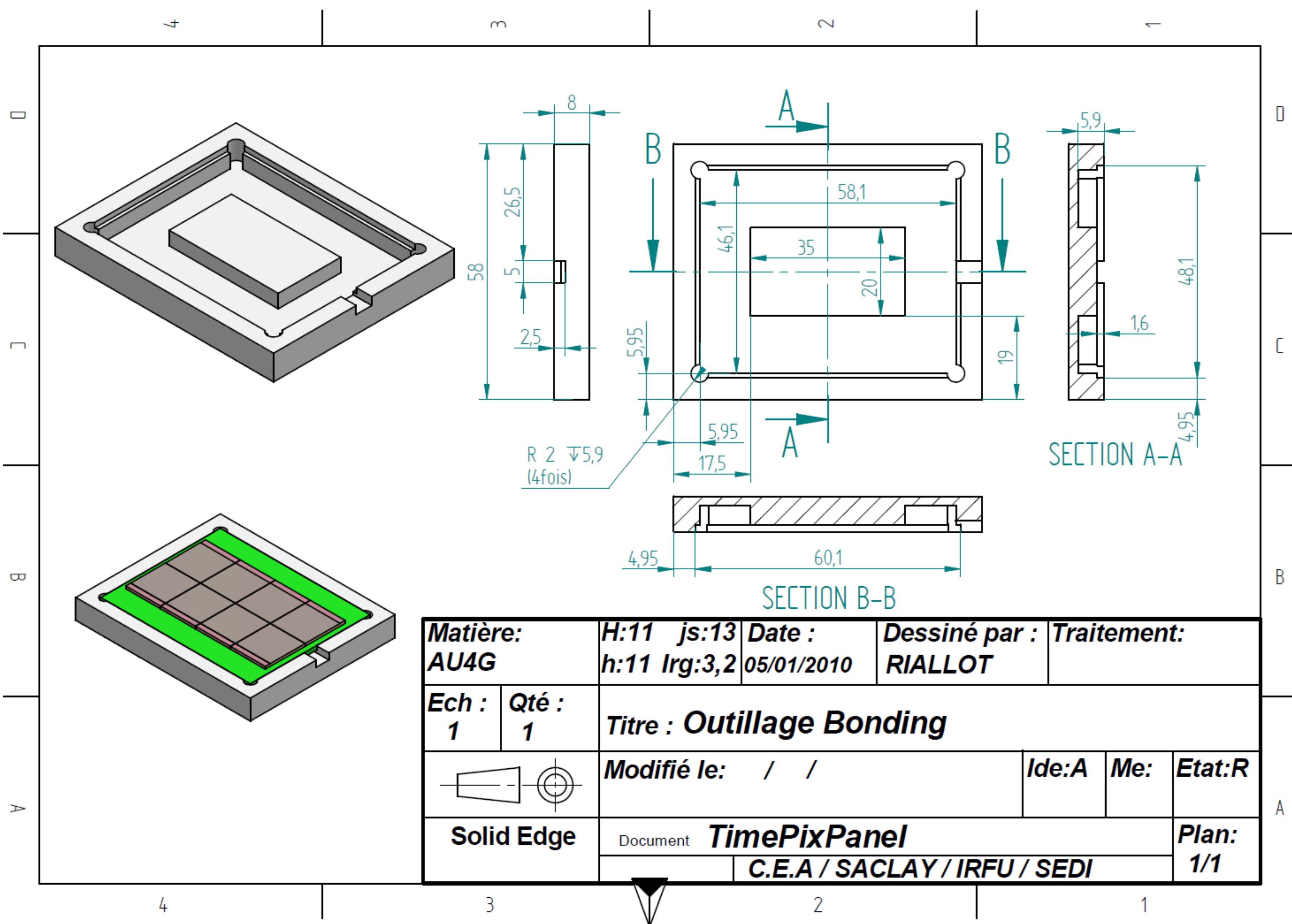
Bottom





Guard ring card for HV homogeneity




8
58
26,5
5
2,5
A
B
B
58,1
46,1
35
20
19
5,95
5,95
17,5
A
R 2 ↧5,9
(4fois)
5,9
48,1
1,6
4,95
SECTION A-A
4,95
60,1
SECTION B-B
Matière:
AU4G
H:11 js:13
h:11 lrg:3,2
Date :
05/01/2010
Dessiné par :
RIALLOT
Traitement:
Ech :
1
Qté :
1
Titre : Outillage Bonding
Modifié le: / /
Ide:A
Me:
Etat:R
Solid Edge
Document TimePixPanel
C.E.A / SACLAY / IRFU / SEDI
Plan:
1/1

Next stages

- The mezzanine card will be first tested using 8 naked TimePix chips
- The mother card will be send to factory in the next days
- Support tool could be built in Saclay

Open questions:

- who will do the bonding of the chip + Ingrid HV
- ready for March ?