AHCAL DIF.

Status and Outlook

Frantisek Krivan, Mathias Reinecke

DIF task force meeting

LLR (Palaiseau), Nov. 27th, 2009

HELMHOLTZ GEMEINSCHAFT

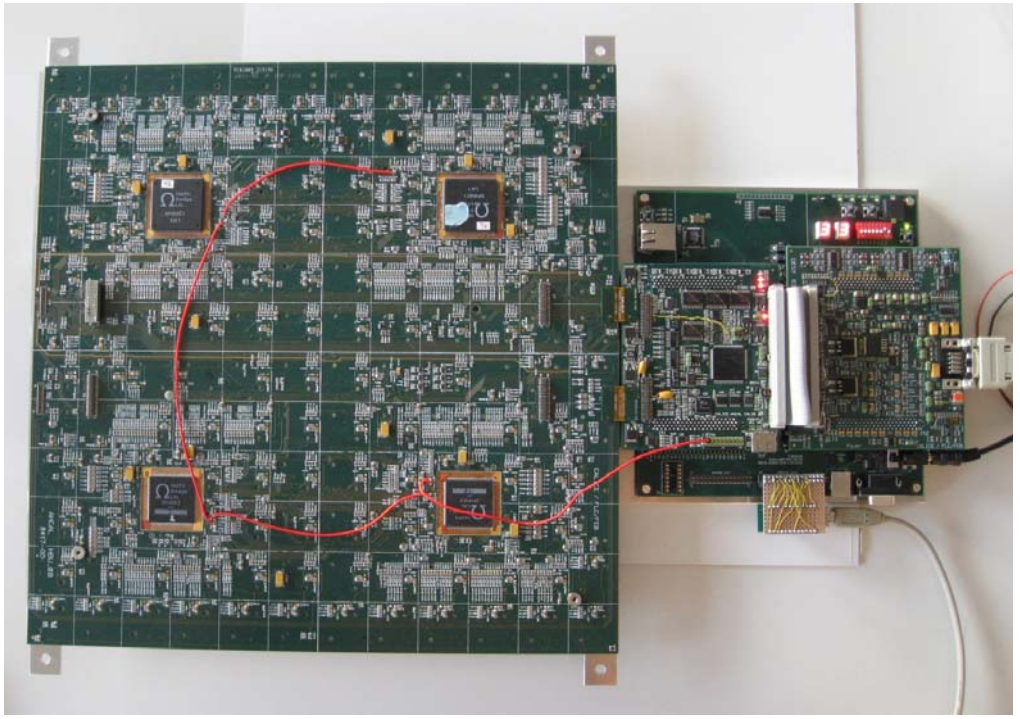
CALICE Calorimeter for ILC

EUDET

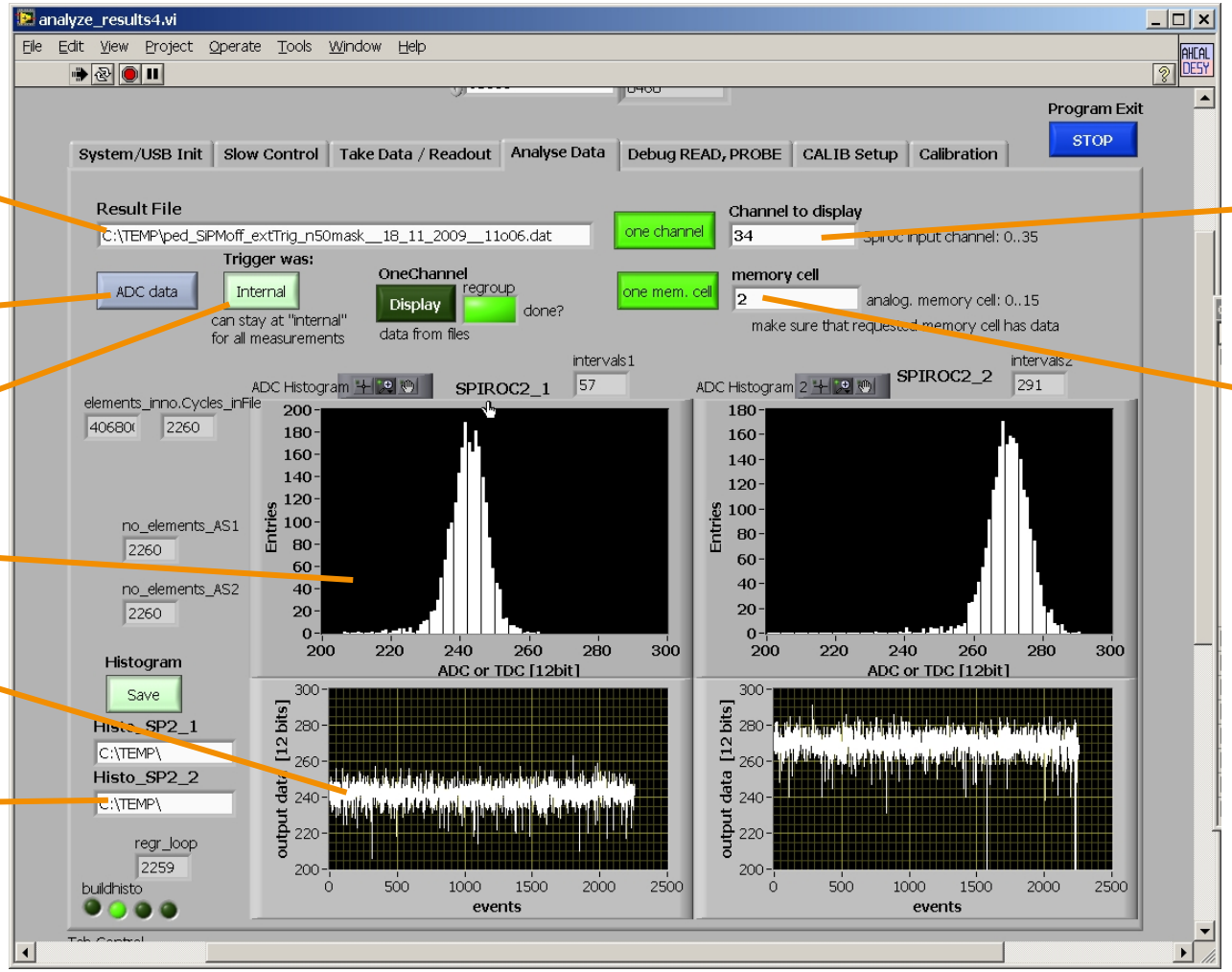
DESY

Outline

- Labview and AHCAL electronics status
- DIF firmware
  - Top-level blocks
  - Inter-Block signals (records?) / top-level FSM implementation / block sharing
- USB interface
- One slide to testbeam
- Next steps
  - CALICE DAQ integration
  - DESY testbeam preparation
  - Module Redesigns



Labview tools – Result Display



Result File

ADC/TDC

Trigger

Histogram

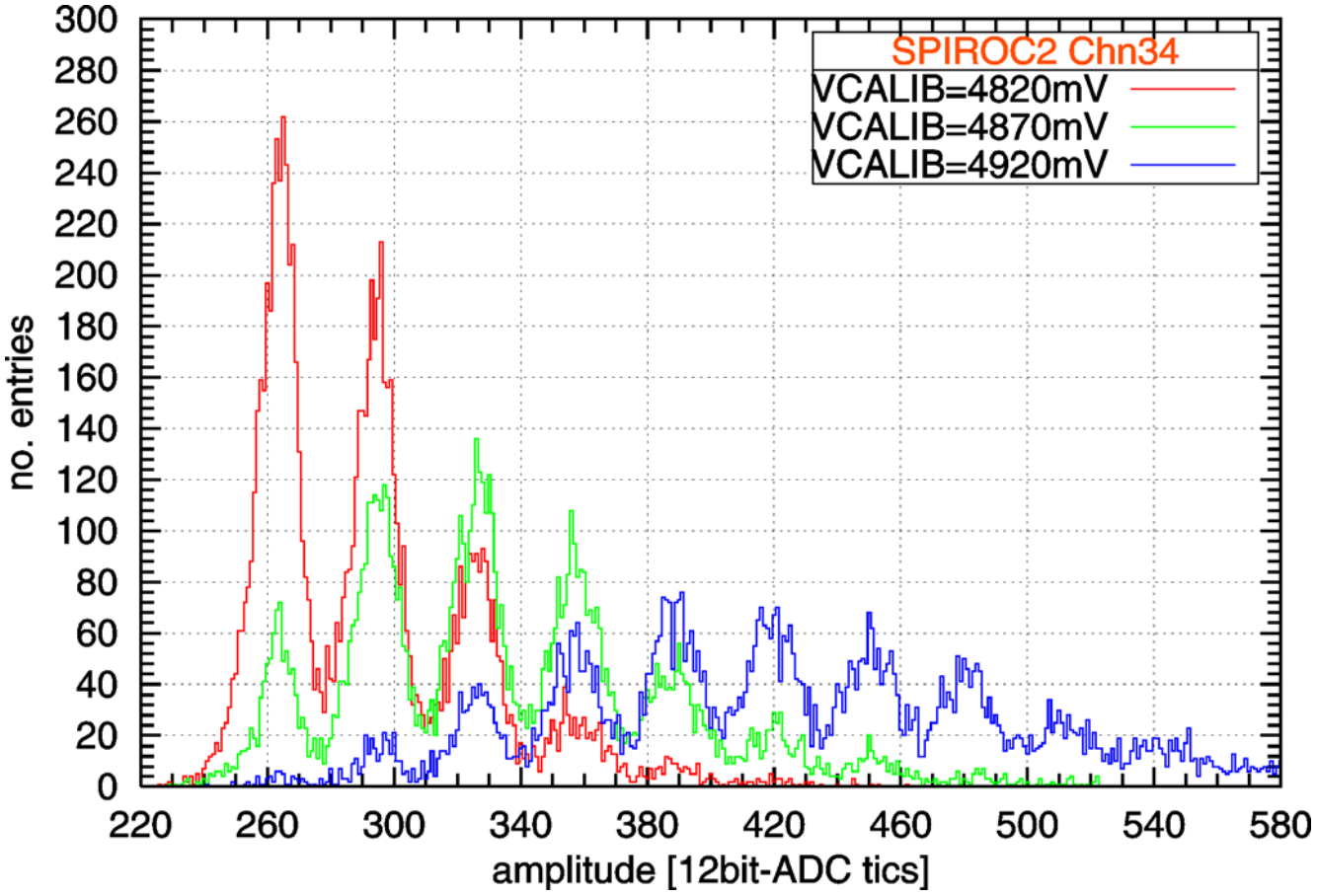
“Event-wise”

Save Histo

Channel: 0..35

Memory Cell: 0..15

First Single-Photon Peaks (single channel)

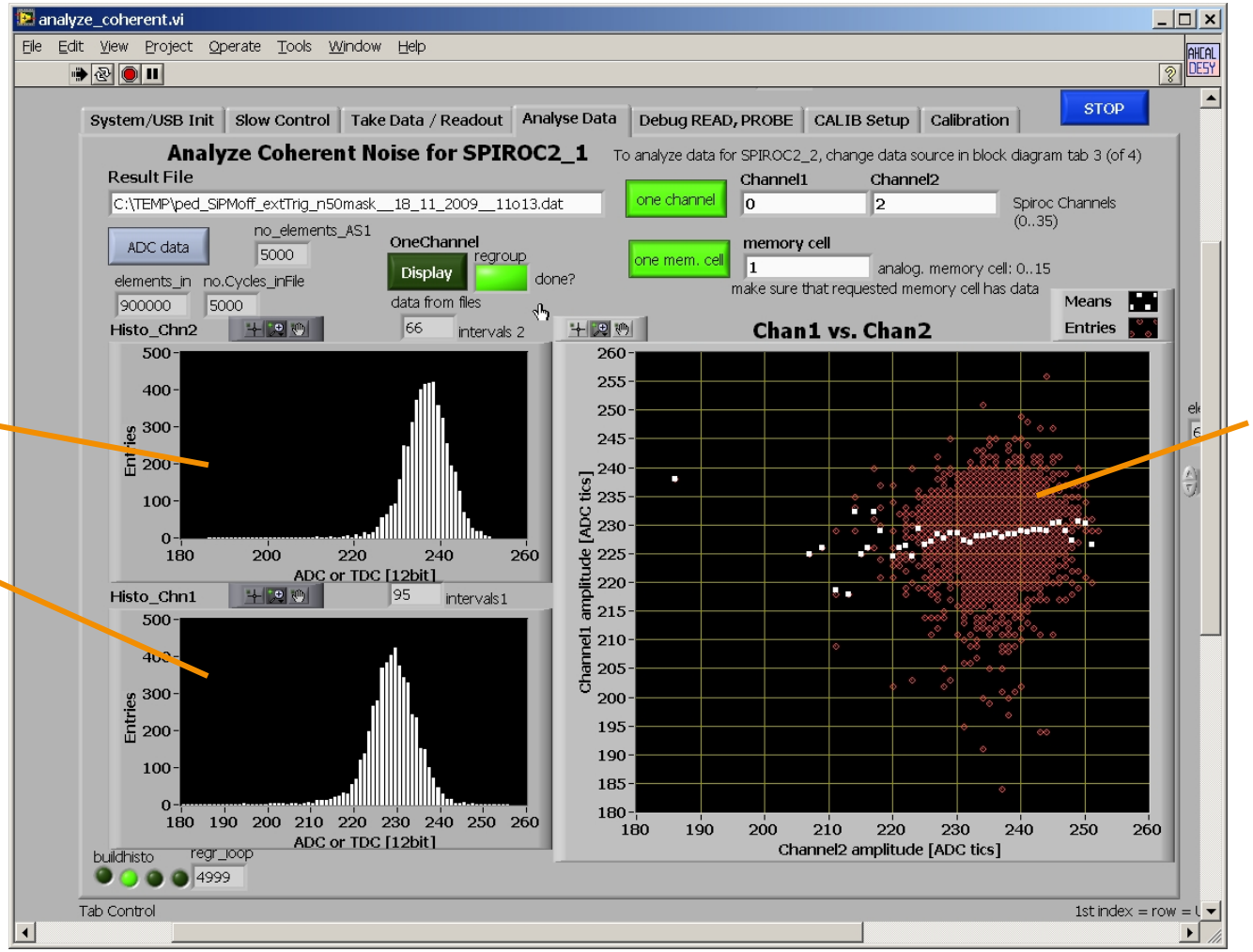


Labview tools – Coherent Channel Noise

Histogram:

Chn2

Chn1

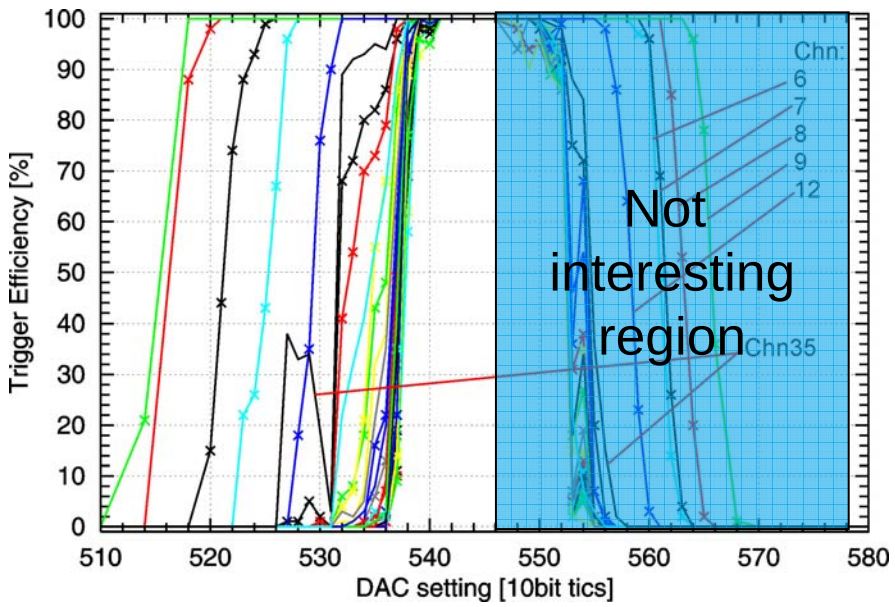


Chn2 vs. Chn1

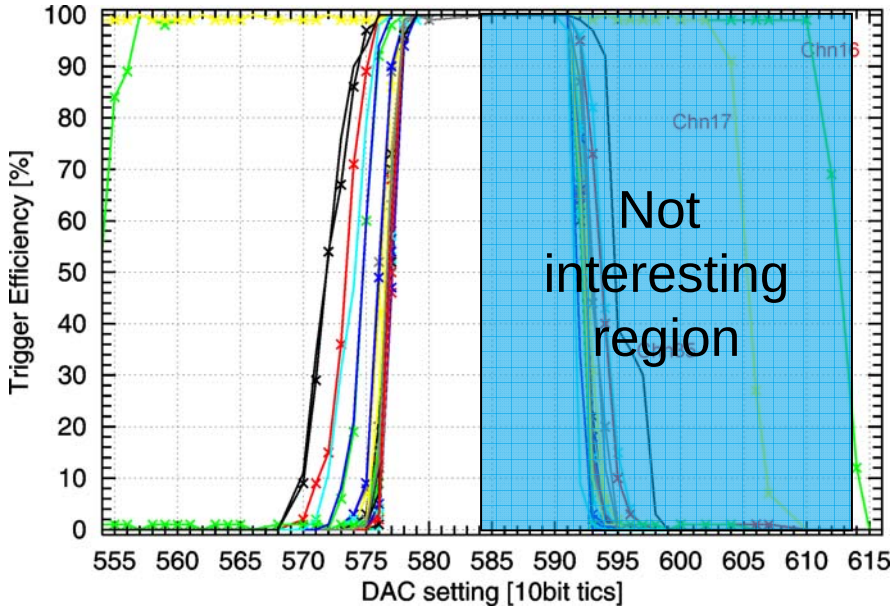
(white pts: mean)

Labview tools – S-Curve analyzation

SPIROC2_1

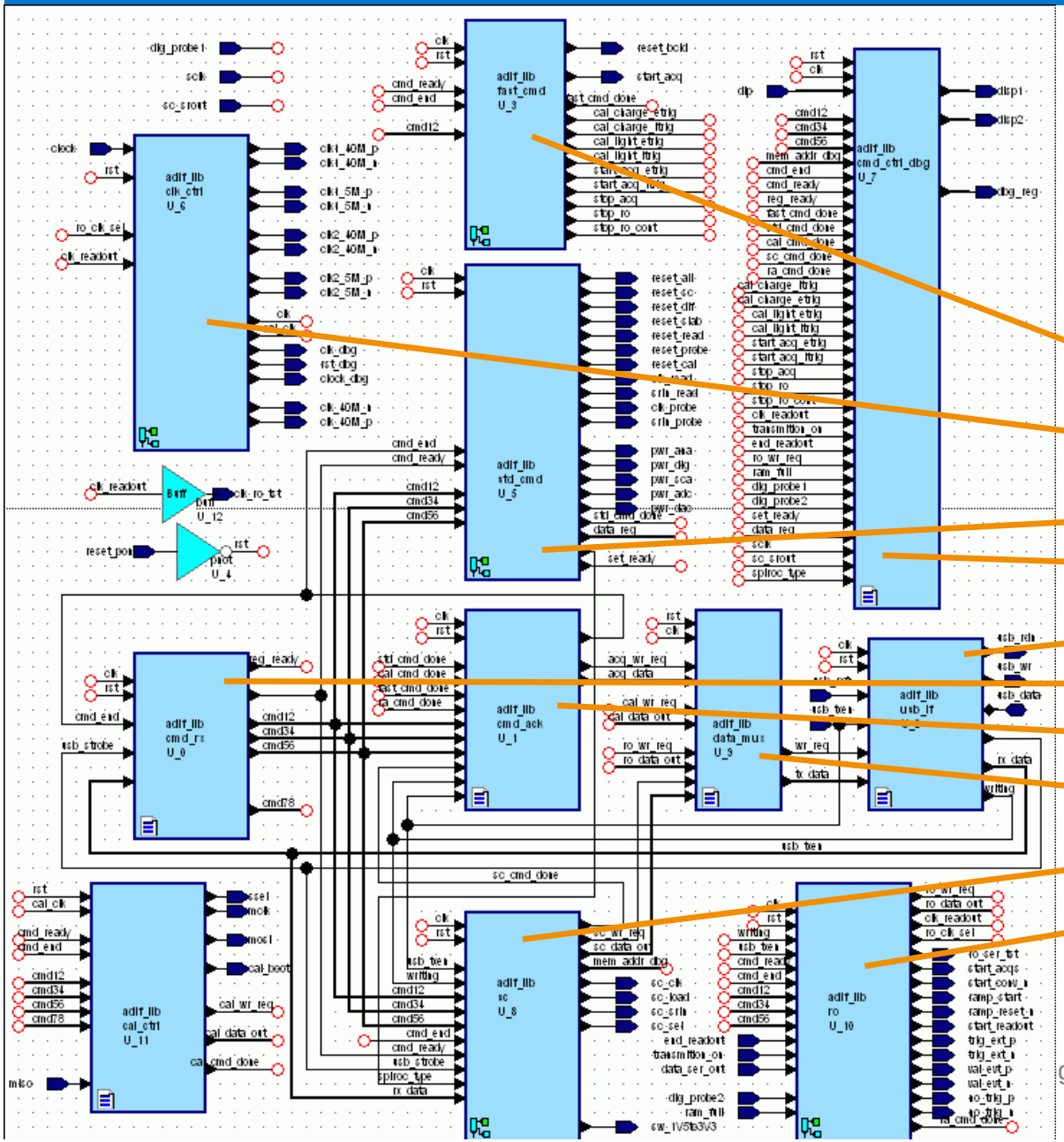


SPIROC2_2



- “Hit Bit” in SPIROC digital output data used for the first time.
- “Noise is in general ok” (Christophe, Stephane): ~ -2.6mV per DAC tic
- Noisy channels for SPIROC2_1 clearly correlated with connected SiPMs
- Chn16 and 17 for SPIROC2_2: Crosstalk from e.g. clock line?

AHCAL DIF firmware – Top-Level



Firmware divided into funct. blocks.

Firmware development: Frantisek Krivan

- FAST Cmds
- Clk+Cntr
- Block-Transf Cmds
- Debug
- USB
- Cmd-Receiver
- Acknowledge
- Data-to-DIF
- Slow-Control
- Readout

AHCAL DIF firmware – top level block structure

Design Hierarchy	Design Unit Na...	Name	Language	Size
adif_top	adif_top	adif_top	VHDL	73 KB
adif_top	adif_top	adif_top	VHDL	73 KB
struct [root]	adif_top	adif_top(struct)	VHDL	230 KB
U_0	cmd_rx	cmd_rx(rtl)	VHDL '93	6 KB
U_1	cmd_ack	cmd_ack(rtl)	VHDL '93	6 KB
U_10	ro	ro(struct)	VHDL	92 KB
U_0	ro_ctrl	ro_ctrl(rtl)	VHDL '93	15 KB
U_2	acq_ctrl	acq_ctrl(struct)	VHDL '93	10 KB
U_11	cal_ctrl	cal_ctrl(rtl)	VHDL '93	10 KB
U_2	usb_if	usb_if(rtl)	VHDL '93	3 KB
dif2usb_...	dif2usb	dif2usb(rtl)	VHDL '93	3 KB
usb2dif_...	usb2dif	usb2dif(rtl)	VHDL '93	3 KB
U_3	fast_cmd	fast_cmd(struct)	VHDL	50 KB
U_0	fast_cmd_dec	fast_cmd_dec(rtl)	VHDL '93	6 KB
U_5	std_cmd	std_cmd(struct)	VHDL	76 KB
U_0	std_cmd_dec	std_cmd_dec(rtl)	VHDL '93	14 KB
U_1	pwr_ctrl	pwr_ctrl(rtl)	VHDL '93	5 KB
U_6	clk_ctrl	clk_ctrl(struct)	VHDL	154 KB
U_20	clk_gen	clk_gen(struct)	VHDL '93	3 KB
U_7	cmd_ctrl_dbg	cmd_ctrl_dbg(rtl)	VHDL '93	9 KB
U_8	sc	sc(struct)	VHDL	67 KB
U_1	sc_ctrl	sc_ctrl(rtl)	VHDL '93	15 KB
U_9	data_mux	data_mux(rtl)	VHDL '93	2 KB

DIF firmware

- Top-Level FSM not implemented yet. (e.g. now possible: start measurement without slow-conrol config). Will be done when agreed on in DIF task force.
- Remi's proposal about record-type inter-block communication not implemented yet, but can be done! Specs needed for generalization!

DIF USB – Communication Protocol

Remi's proposal (1 byte per line), from PC to DIF:

USB Data	Explanation	in AHCAL up to now (prelim.)
START	0xAA	0xCC (we can easily change)
Header	2b config, 5b address, 1b r/w	type_modifier (significant byte)
Size	Size data block MSB	Size data block MSB
Size	Size data block LSB	Size data block LSB
Data	Data to DIF	Data to DIF
...	...	...
Data	Data to DIF	Data to DIF
STOP	STOP or RESTART	

- 'Data' is most often 2-bytes command data (see command manual)
- Missing in AHCAL 'header': address for partition/slab/ROchain (3b). Could be in 'Size MSB' or 'Data MSB' ??

DIF USB – Communication Protocol II

In AHCAL: DIF answers on commands with an Acknowledge (6 bytes):

USB Data	in AHCAL: Acknowledge
START	0xCC (we can easily change)
Header	type_modifier (significant byte)
Size	Size data block MSB
Size	Size data block LSB
Data	Command Data Word MSB
Data	Command Data Word LSB

- Simple Commands: Acknowledge is echo.
- Readout of settings (temperature, registers, voltages, …):
  DIF sends data first and Acknowledge afterwards
- FAST Commands: echo.

DIF USB – Readout ROC Data

Field	SubField	Comments
PACKETTYE (16b)		DIFBT_PKT_DATA = 0x"0001"
PACKETID (16b)		Arbitrary ID (automatic increment)
TYPEMODIFIER (16b)		0x000e
DATALENGTH (16b)		Number of 16b words in the DATA field
DATA	localDIFID (6b)+ ROpacketID (10b)	Read-out data specific header
	ROLastPacket(1b) + ROChainID (3b) + ROSequenceID (12b)	Read-out data specific header
	ROCData 1 to 505 x 16b words	Data slice from the ROCs, w or w/o empty chips (a slice of **DIF_MaxROPacket_Size** – 7 words max)
CRC	16b	Inserted by 8b/10b itf

In AHCAL up to now:

- No CRC.
- Data Section 100bytes maximum.
- Some fields filled with dummy data up to now.

OK, or something more simple for USB?

DIF USB – Slow Control Data

Field	Subfield	Comments
PACKETTYPE (16b)		
PACKETID (16b)		
TYPEMODIFIER (16b)		
DATALENGTH (16b)		
DATA	localDIFID (6b) + ROpacketID (10b)	16 bit
	SCDataSet (1b) + ROChainID (3b) + ASICAddress (12b)	16 bit
	SCData	1 to 505 16bit-words
CRC (16b)		

Table 26: Block Transfer packet structure for the transfer of Slow-Control data

SC packet structure for CALICE DAQ
(cf. command manual)

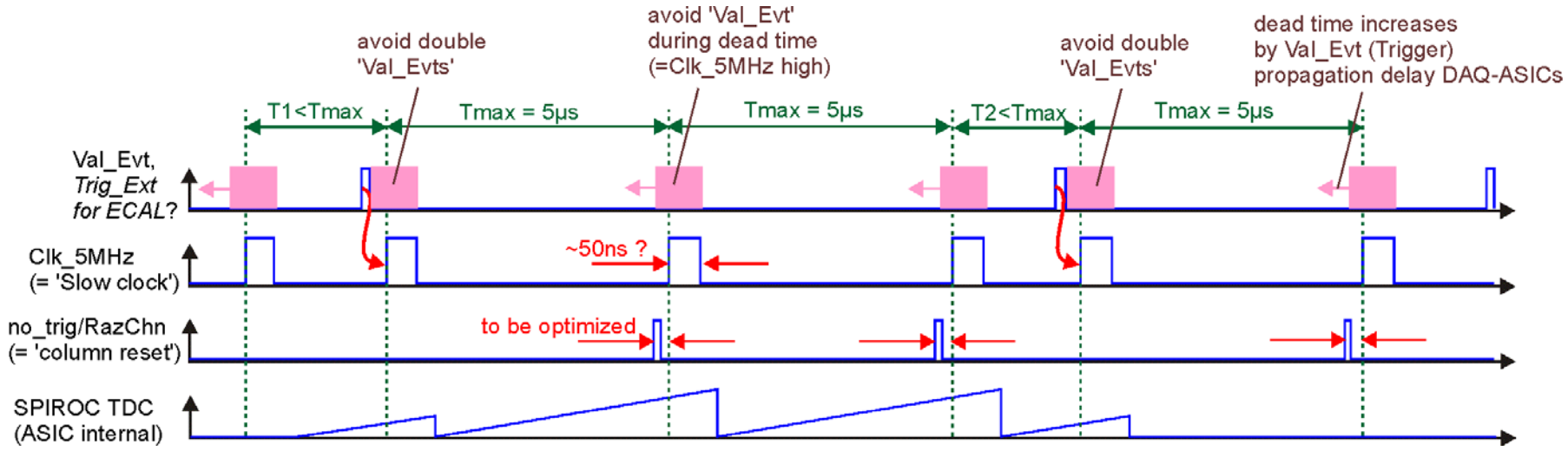
In AHCAL up to now: 1byte header:
2b partition + 5bit ROCaddress + 1bit SCSet

SC-data is transferred ROC-wise.

Will be changed if we agree on CALICE-DAQ scheme for USB!

Testbeam (AHCAL and all)

- See: email about testbeam trigger (last week)
- Reason for Validate-Signal: High SiPM noise: Would fill SPIROC immediately.



- Dead time: CK_5M='1' (all detectors)

Next Steps

- DESY testbeam: Implementation of external trigger, Val_Evt, no_trig/RazChn. No power-pulsing at first.
- DIF Redesign / ECAL DIF implementation (+ HBU, CALIB, POWER redesigns) towards EUDET module (ILC dimensions)
- CALICE DAQ integration: Probably no integration to AHCAL before spring 2010 (ahead: SPIROC and HBU tests, Prague LED system, DESY testbeam, redesign of modules).

Conclusions and Outlook

- USB frame format: Can be changed (when agreed on) to Remi's proposal, but not before DESY testbeam.
- Top-level FSM can be added to firmware when agreed on.
- Firmware is divided into blocks of the needed tasks => sharing possible.
- Commands correspond to DIF Command Manual.
- CALICE DAQ not yet implemented.
- DIF FPGA XC3S1500: filled to ~35% (not critical). Block RAM needed for readout data buffering (could be more critical in full extension).
- January: SPIROC3, SKIROC submission. Last wish-list to LAL (e.g. empty chips transmit Chip-ID, …). Agree on in DIF group ?!

SPIROC2 “features” (digital part)

- Channel-wise trigger threshold deterioates general threshold (AHCAL only?),
- Data of 1st event (trigger) =“0”,
- Single-channel readout failures (significant amount, few %),
- Probe register dead,
- Slow-control programming only possible with 1.8V VDD,
- Bandgap reference off specs (2.6V instead of 2.5V), therefore problems with all related bias voltages, e.g. ADC input range.
- Not really a bug: SPIROC without data does not respond during readout. => DIF has to do first data processing – was not foreseen.