

DIF Firmware Development

Status

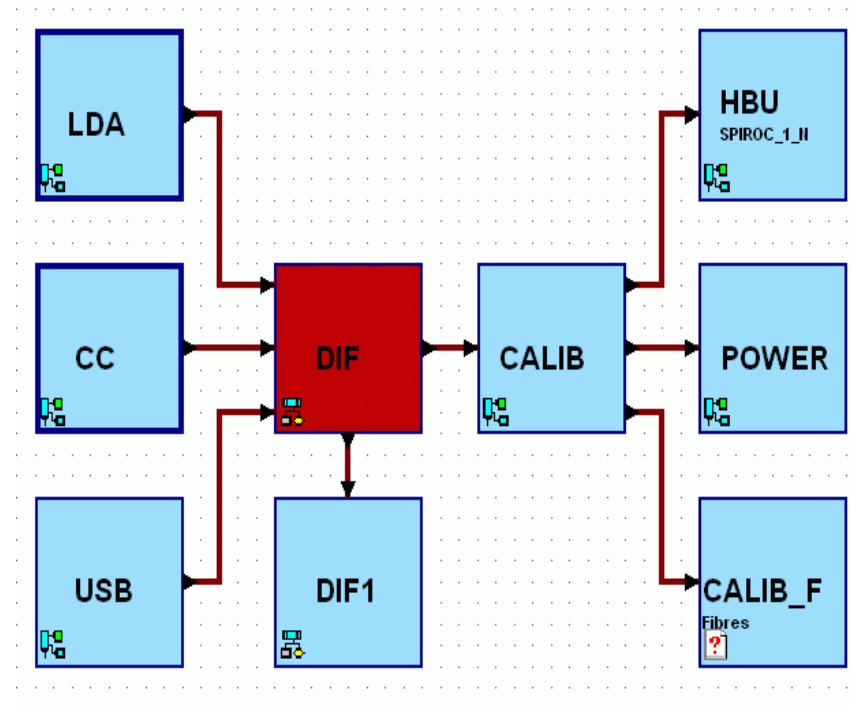
Presented by Frantisek Krivan



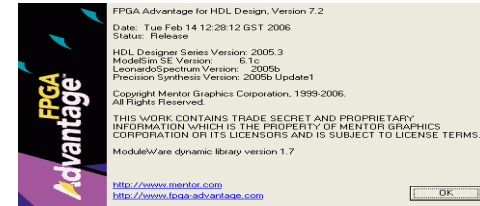
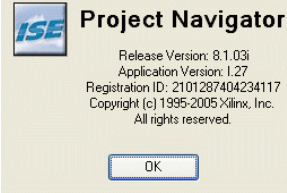
- ❑ Definition of the DIF communication with other parts of the system
- ❑ Base DIF firmware development for lab tests
- ❑ Beam test modification
- ❑ DIF communication with LDA and C&C
- ❑ Readout modification
- ❑ Standardization

(25/02/2008)

- ❑ LDA
- ❑ C&C - machine clock and fast signals
- ❑ DIF - redundancy against loss of LDA link
- ❑ Slab - SPIROC ASIC
- ❑ Calib module
- ❑ Power module



- DIF Commands Proposal
- DIF - ASIC Timing diagrams
- DIF Development for ECAL, DCAL
- SPIROC I. and II. Technical Information - Omega Webpage
- Calice LDA Docs - Marc Kelly
- Format of the read-out data of the DIF
- E-mail discussions
- Spartan Docs, USB Docs, SPI Docs, ...
- ...



The screenshot displays a complex software environment with three main windows:

- LabVIEW Front Panel (Left):** Titled "ahcal_vers6.vi Front Panel", it shows the "Operation of AHCAL Calibration System (CALIB)". It includes sections for "Set Delay Lines", "ADC operation", and "Enable Section". The "ADC operation" section features a table of ADC channels:

R_ADC1	R_ADC2	R_ADC3	R_ADC4
Temp1 0	V_CALIB1 0	V_DAC 0	H11 0
Temp2 0	V_CALIB2 0	IDAC 0	H1 0
Temp3 0	V_COD 0	VREF 0	H2 0
Temp4 0	I_COD 0	TRF 0	H2 0
Temp5 0	V_ODA 0	VADCKEF 0	H3 0
Temp6 0	I_ODA 0	reserved 0	H3 0
reserved 0	reserved 0	reserved 0	reserved 0
VADCKEF 0	VADCKEF 0	VADCKEF 0	VADCKEF 0

Below the table, it states: "voltages in V, currents in mA, temperatures in degrees C".

- ISE Design Manager (Middle):** Shows the project structure for "adif" and "adif_top". It includes a Design Explorer and a Design Tree.
- ModelSim Code Browser (Right):** Displays the VHDL code for "0: sc_clk.vhd". The code includes signal declarations and process blocks for clock management and data transfer.

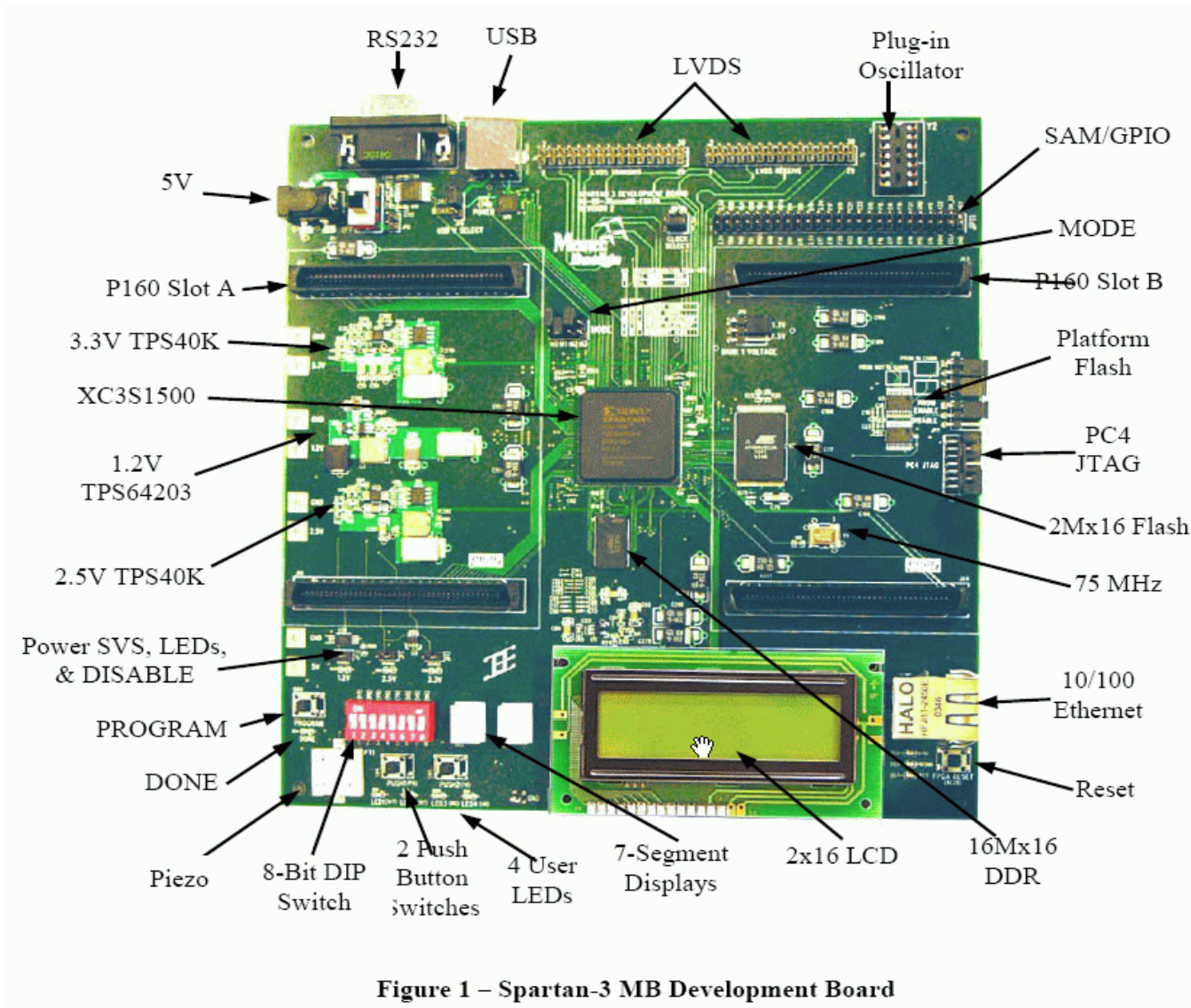
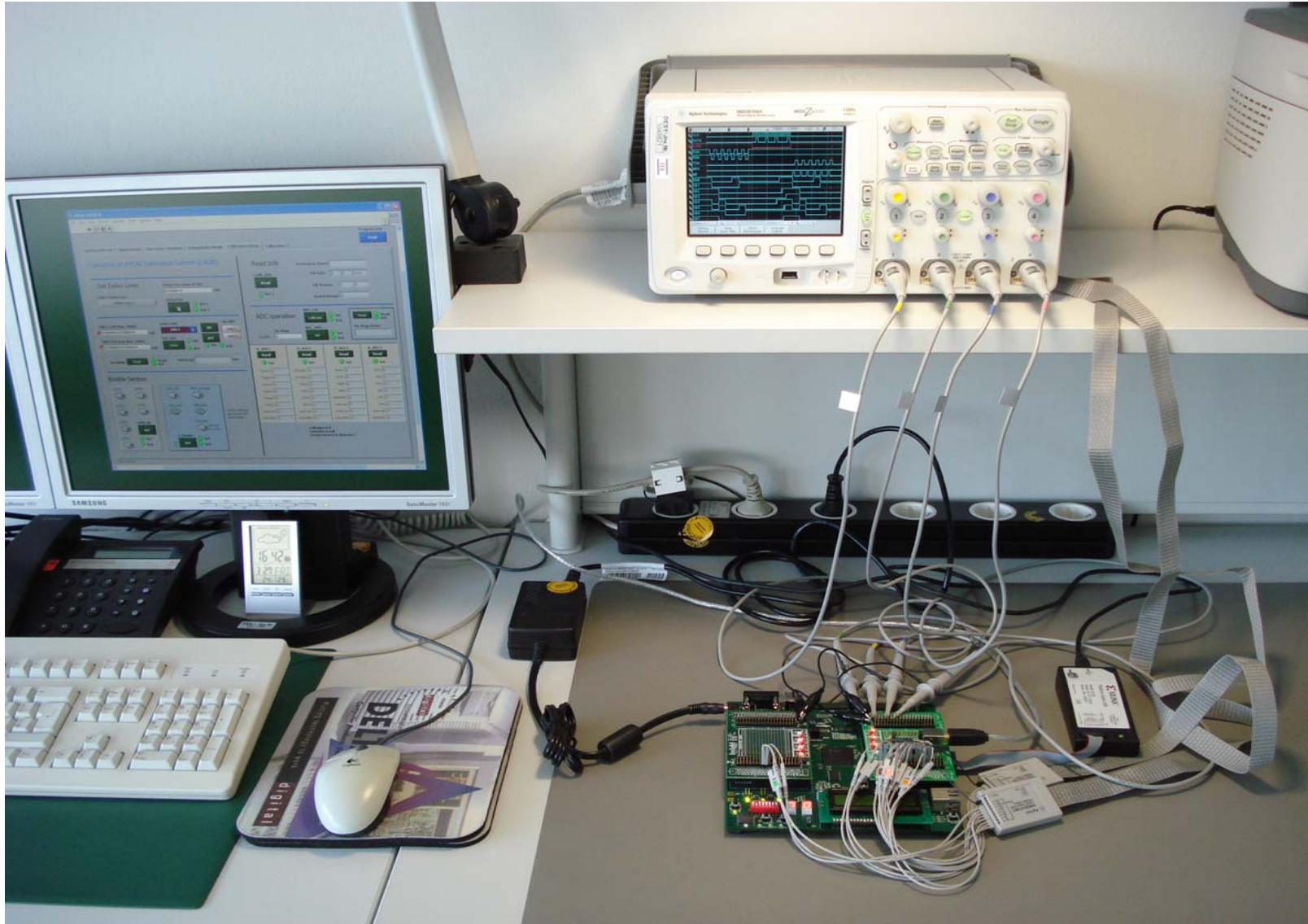


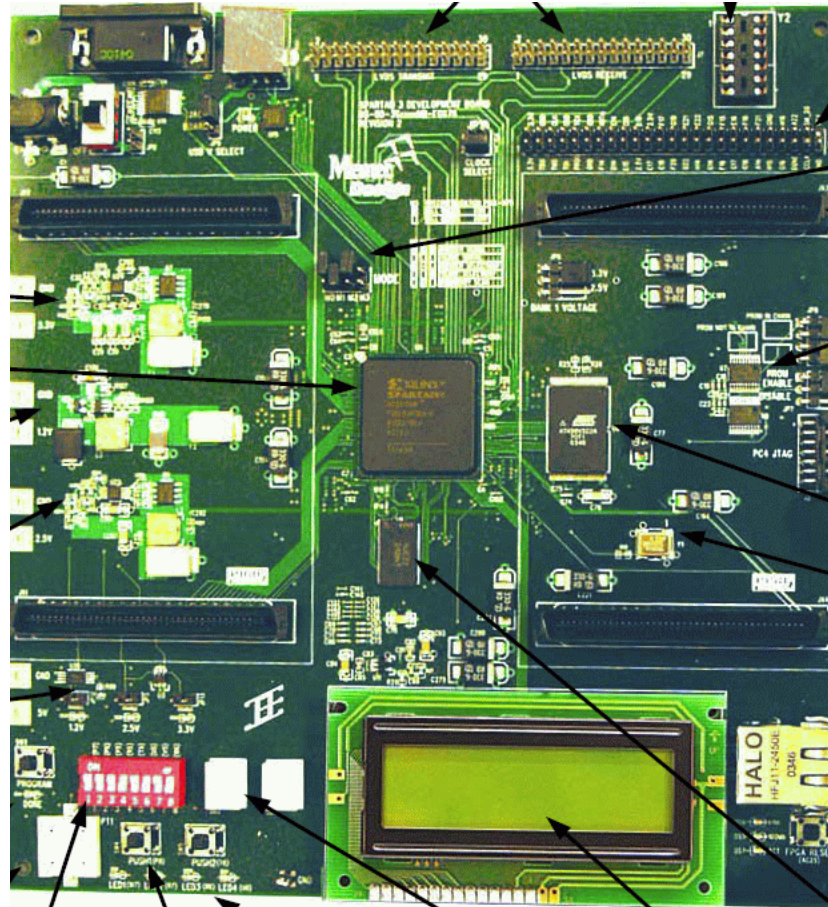
Figure 1 – Spartan-3 MB Development Board



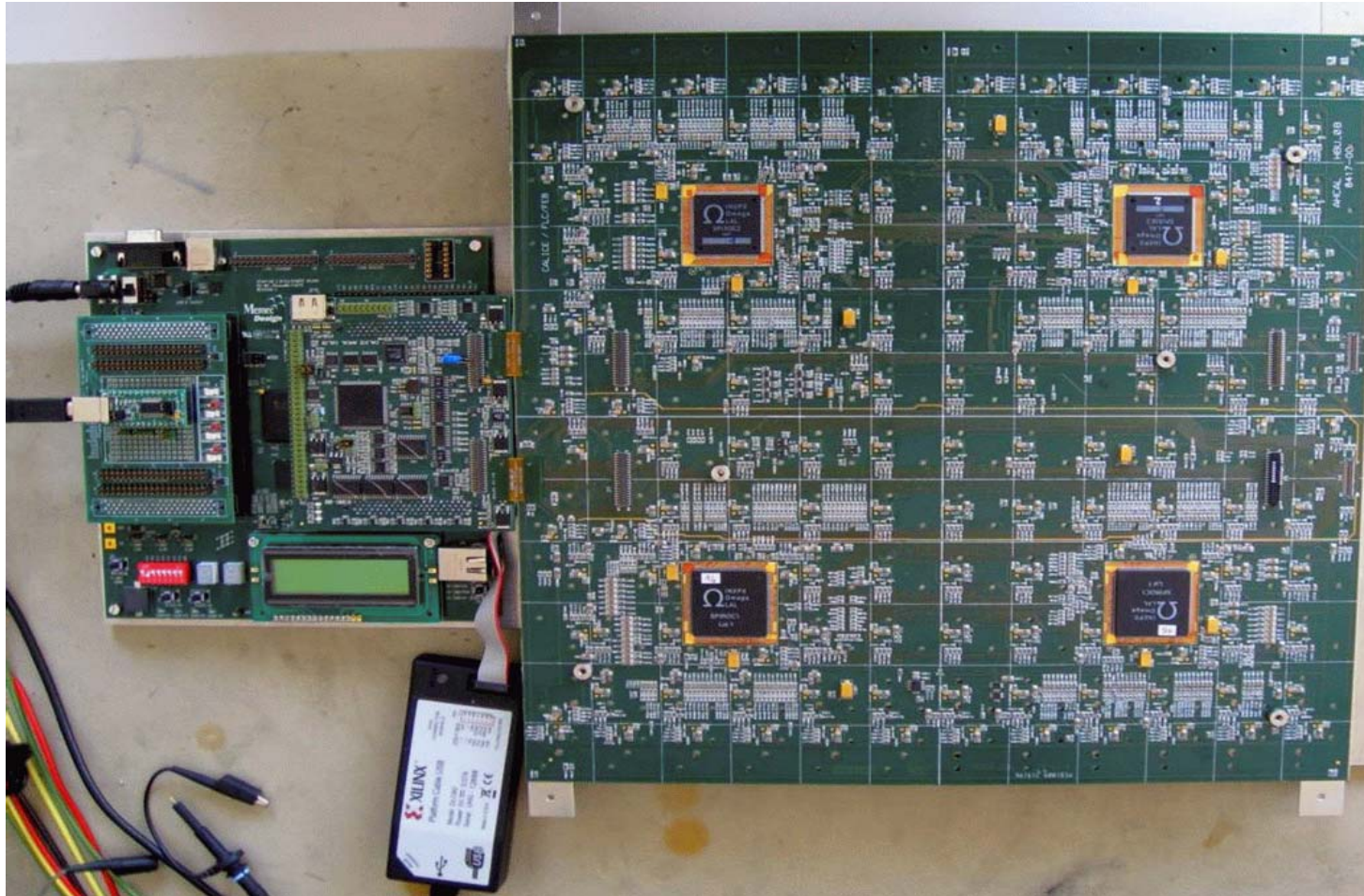
DIF Firmware

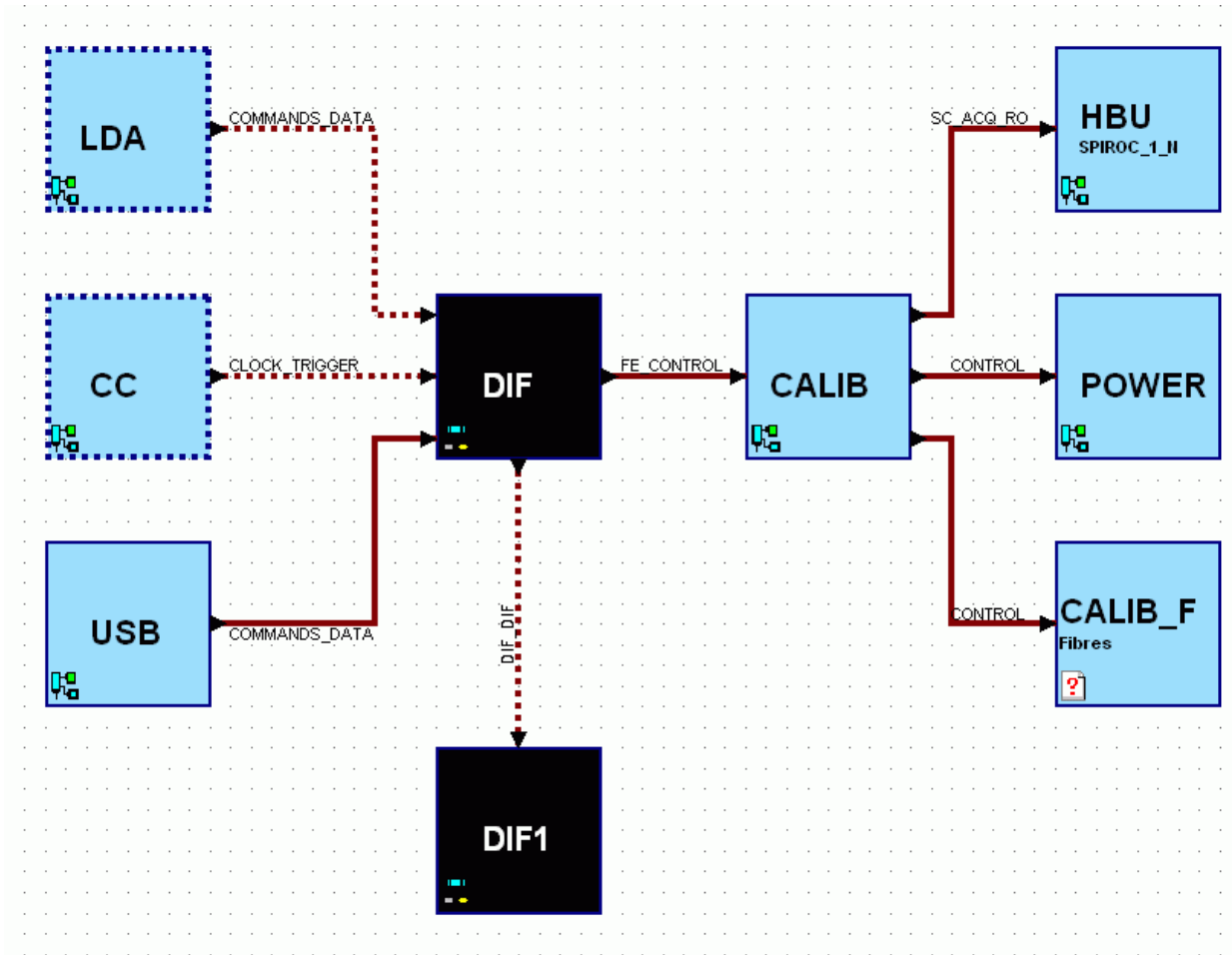
Real or Virtual? Status and Comments (31/03/2009)

Imagine there's
(no) LDA
it's easy
if you try,
...

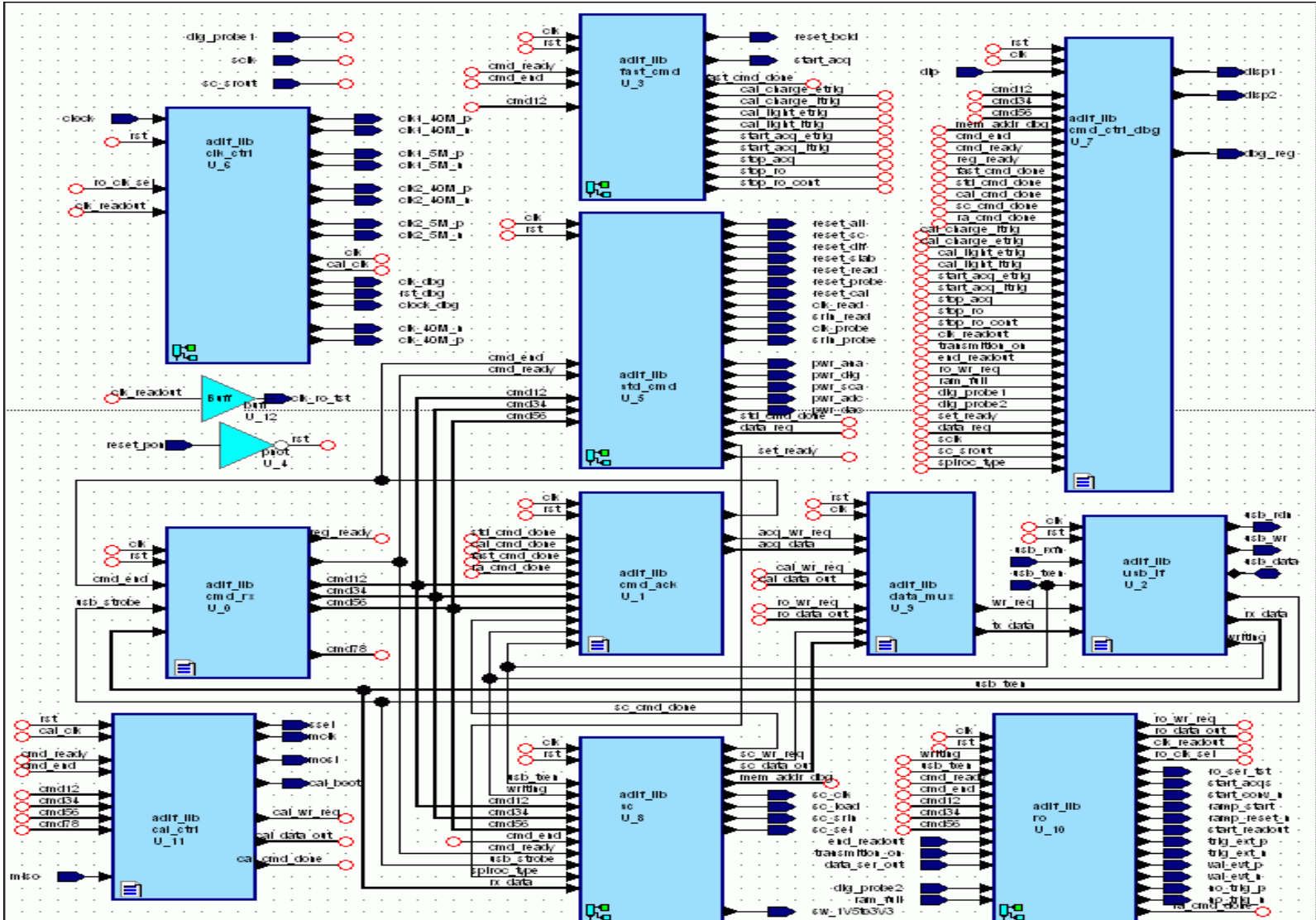


Imagine there's
(no) SPIROC
it's easy
if you try,
...

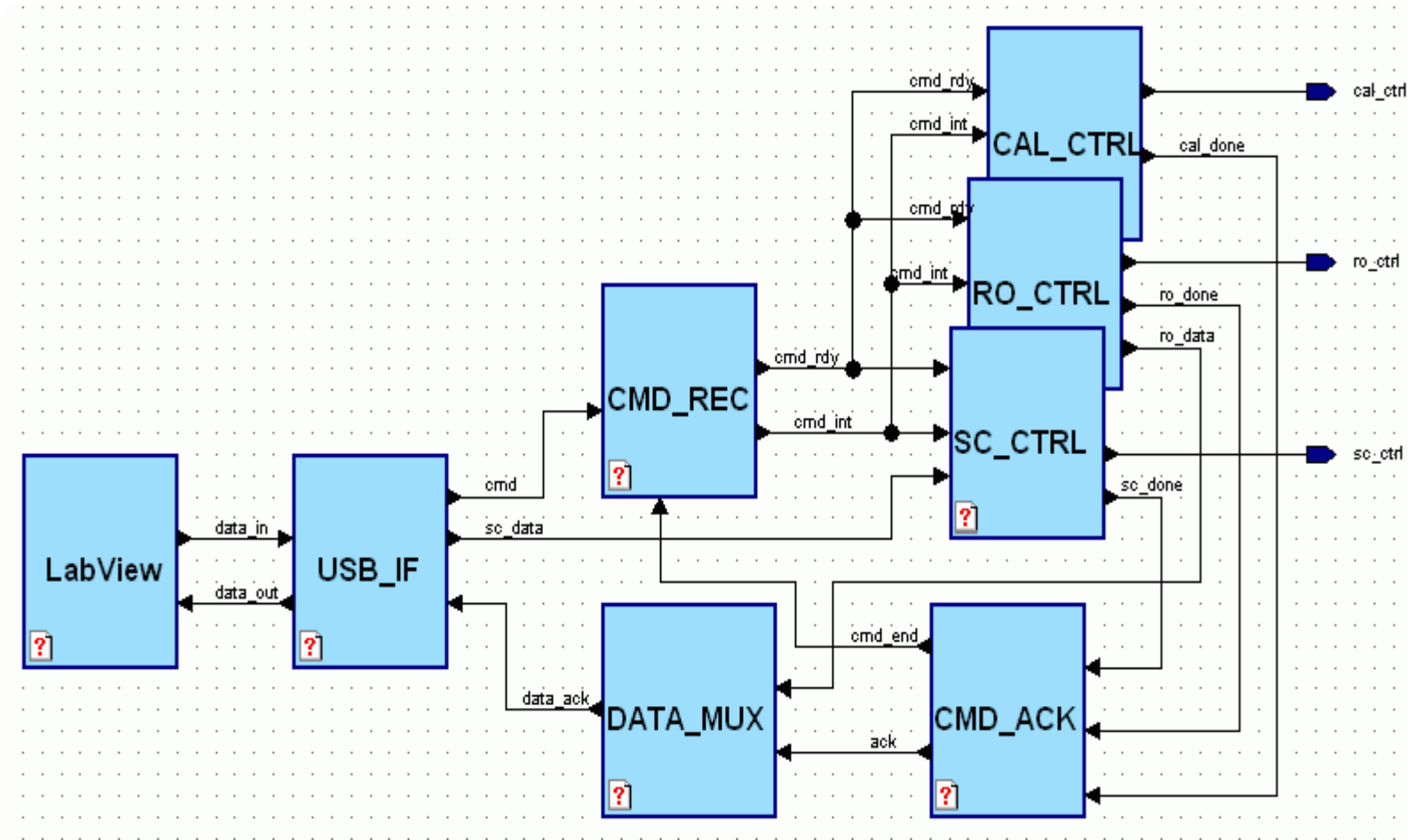




DIF Top Hierarchy



Design Hierarchy	Design Unit Na...	Name	Language	Size
[-] adif_top	adif_top	adif_top	VHDL	73 KB
[-] adif_top	adif_top	adif_top	VHDL	73 KB
[-] struct [root]	adif_top	adif_top(struct)	VHDL	230 KB
[-] U_0	cmd_rx	cmd_rx(rtl)	VHDL '93	6 KB
[-] U_1	cmd_ack	cmd_ack(rtl)	VHDL '93	6 KB
[-] U_10	ro	ro(struct)	VHDL	92 KB
[-] U_0	ro_ctrl	ro_ctrl(rtl)	VHDL '93	15 KB
[-] U_2	acq_ctrl	acq_ctrl(struct)	VHDL '93	10 KB
[-] U_11	cal_ctrl	cal_ctrl(rtl)	VHDL '93	10 KB
[-] U_2	usb_if	usb_if(rtl)	VHDL '93	3 KB
[-] dif2usb_...	dif2usb	dif2usb(rtl)	VHDL '93	3 KB
[-] usb2dif_...	usb2dif	usb2dif(rtl)	VHDL '93	3 KB
[-] U_3	fast_cmd	fast_cmd(struct)	VHDL	50 KB
[-] U_0	fast_cmd_dec	fast_cmd_dec(rtl)	VHDL '93	6 KB
[-] U_5	std_cmd	std_cmd(struct)	VHDL	76 KB
[-] U_0	std_cmd_dec	std_cmd_dec(rtl)	VHDL '93	14 KB
[-] U_1	pwr_ctrl	pwr_ctrl(rtl)	VHDL '93	5 KB
[-] U_6	clk_ctrl	clk_ctrl(struct)	VHDL	154 KB
[-] U_20	clk_gen	clk_gen(struct)	VHDL '93	3 KB
[-] U_7	cmd_ctrl_dbg	cmd_ctrl_dbg(rtl)	VHDL '93	9 KB
[-] U_8	sc	sc(struct)	VHDL	67 KB
[-] U_1	sc_ctrl	sc_ctrl(rtl)	VHDL '93	15 KB
[-] U_9	data_mux	data_mux(rtl)	VHDL '93	2 KB



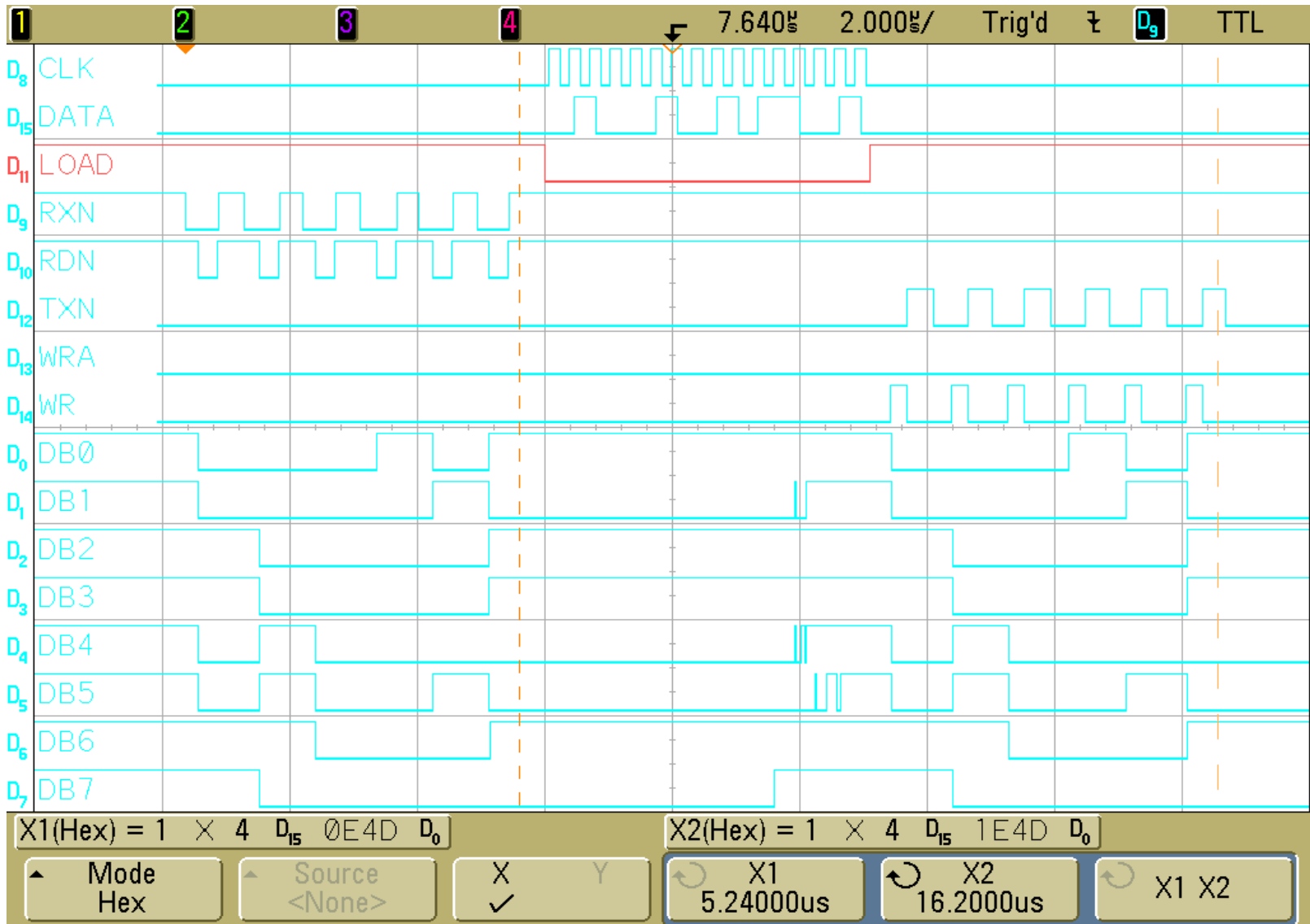
- Fast Commands**
- Standard Commands**
- Slow Control Commands**
- Acquisition and Readout Commands**
- Calib Commands**

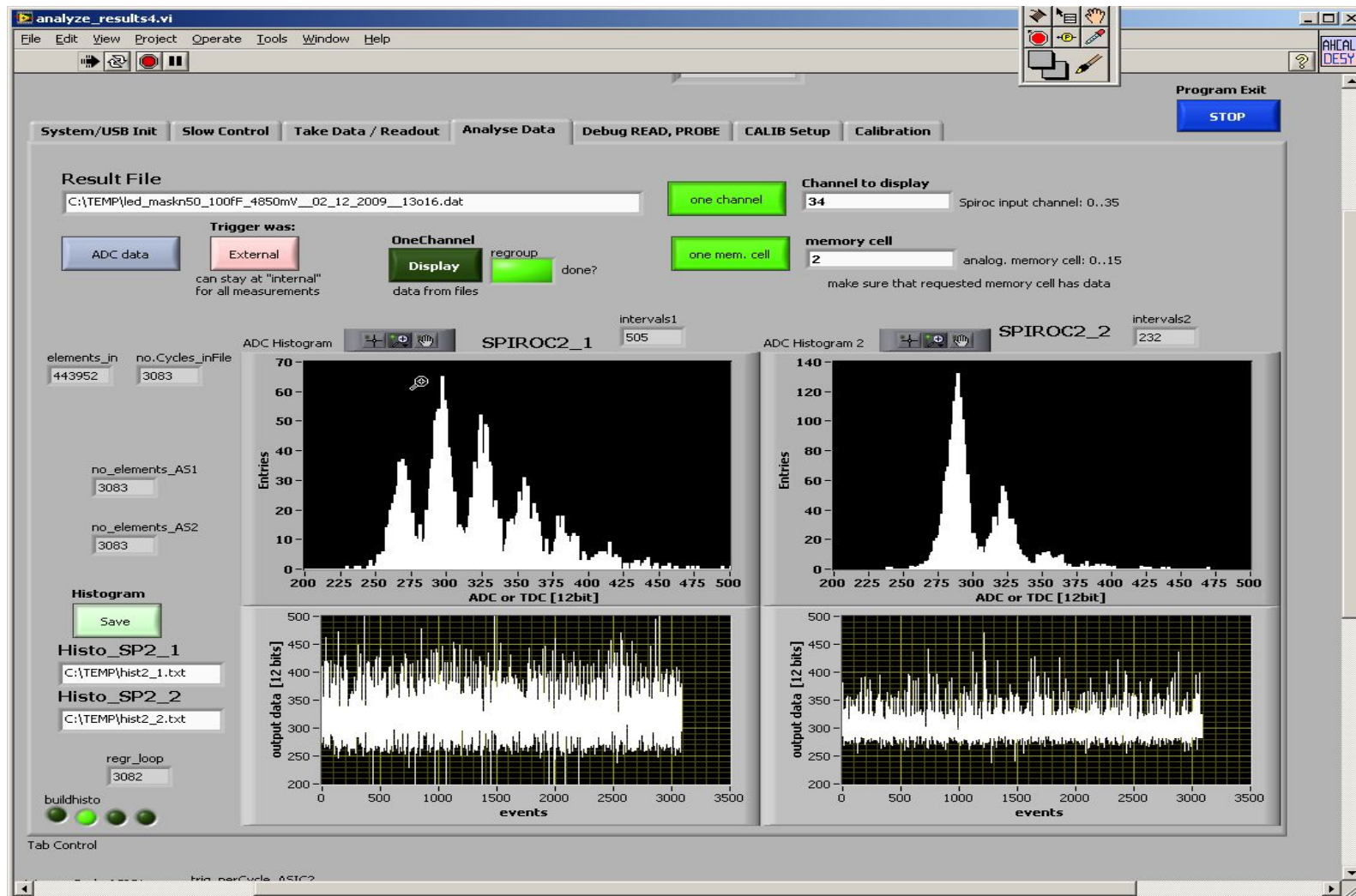
The screenshot displays the LabView interface for the AHCAL calibration system. The main window is titled "ahcal_vers6.vi" and features a menu bar (File, Edit, View, Project, Operate, Tools, Window, Help) and a toolbar with execution and debugging icons. The interface is organized into several functional sections:

- System/USB Init**: Contains a "Program Exit" button and a "STOP" button.
- Operation of AHCAL Calibration System (CALIB)**:
 - Set Delay Lines**: Includes a "Delay Line Value (8-bit)" field set to "01001101" (LSB), a "Select Delay Line" dropdown menu (currently "Delay Line 2"), and "Set" and "Ack" buttons.
 - DAC1 (LED Bias, 16bit)**: Value "0100000101000010" (LSB), "Set" and "Ack" buttons, and "ON/Off?" controls.
 - DAC2 (Charge Bias, 16bit)**: Value "0100000101000010" (LSB), "Set" and "Ack" buttons, and "ON/Off?" controls.
 - ReadDAC**: "Read" button, "Read Ack" indicator, and "DACRead" field (hex).
- Enable Section**:
 - LVDS**: Controls for LVDS1-6, "LVDS all" button, and "Set/Ack" buttons.
 - PWR**: Controls for PWR_LED, PWR_Charge, Slab_Pow, SIPM_Bias, Pre_Bias (with "off: 10V on: full V" label), and "C_Power" (with "Set ALL" label). Includes "Set" and "Ack" buttons.
- Read Info**: "Si Serial no. (hex)" field, "SW Date" (0 0 0000), "SW Version" (0 0), "Board Version" (0), and a "Read" button.
- ADC operation**: "ADC_Cal" (Calibrate, Set, Ack), "ADC_AVG" (Set, Ack), "No. Avgs" (1.255, 1), and "Read" and "Read Ack" buttons.
- ADC Readouts**: Four columns (R_ADC1 to R_ADC4) each with "Read" and "Set" buttons. Below each column is a list of parameters (Temp1-6, VCalIB1-2, VDD, IDDD, VDDA, IDDA, reserved, VADCREf) with numerical values (mostly 0).
- Legend**: "voltages in V", "currents in mA", "temperatures in degrees C".

SPI Commands for CALIB Board from DIF Board					
Command:	Hex	Data		Return Value	
Group 1:			System informationen		
Read Silicon Serial Number	0x11	--	--	6 Byte	SiliconNumber
Read Software data	0x12	--	--	4 Byte	Datum: DD MM JJJJ
Read Software version	0x13	--	--	1 Byte	0.0 - 15.15 (0xFF)
Read Board version	0x14	--	--	1 Byte	0 - 31
Group 2:			Set Delay Line		
Set DelayLine 1	0x21	1 Byte	0-255	--	--
Set DelayLine 2	0x22	1 Byte	0-255	--	--
Set DelayLine 3	0x23	1 Byte	0-255	--	--
Group 3:			Enable Transmitter and Power		
Enable LVDS Repeat en_1	0x31	1 Byte	0 or 1	--	--
Enable LVDS Transm. en_2	0x32	1 Byte	0 or 1	--	--
Enable LVDS Transm. en_3	0x33	1 Byte	0 or 1	--	--

SPI Command Example





- It works !

Need to be done :

- Beam test modification
- DIF communication with LDA and C&C
- Readout modification (circular buffer, dual port memory)

ahcal_vers6.vi

File Edit View Project Operate Tools Window Help

System/USB Init Slow Control Take Data / Readout Debug READ, PROBE Calibration Setup Calibration

Program Exit STOP

Enter SC-Data File Name with Path
C:\temp\test2.txt

Information in File (first line):
SPIROC1-dummy

slab SPIROC set header_sc
2 [1..4] 3 [1..24] 2 [1..2] 01000101 Byte

Send as many data sets to DIF as there are ASICs connected - before pressing 'Load'.

SC_Data from USB to DIF FPGA

SC_Write1 Write SC_Tx Ackn.

Load_SC Load Ack. Transfer data from DIF to ASICs

RESET_SC RESET Res_SC Ack. Reset Slow_control Register in ASICs

afterwards

Readback SC-Data from DIF (One Set of Data)

slab SPIROC set
1 [1..4] 1 [1..24] 1 [1..2]

SC_ReadB READ Tx_RB Ackn. 2 header_sc 00000000 Byte

Before pressing 'READ', define which set to read back.

Bytes Read 0

BytesSent 88

SC_data_Tx 2

```
!#$%&()*+,-./
0123456789:
;<=>?@ABCDEF
GHIJKLMNPOQRS
TUVWXYZ[]
^_`abcdefghijklmnopqrstuvwxyz
```

Before ASCII conversion SC_data_Tx

33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48

Tab Control

- ❑ Parameters Size
 - ❑ Chain 1 - 4
 - ❑ ASIC 1 - 24
 - ❑ Set 1 - 2

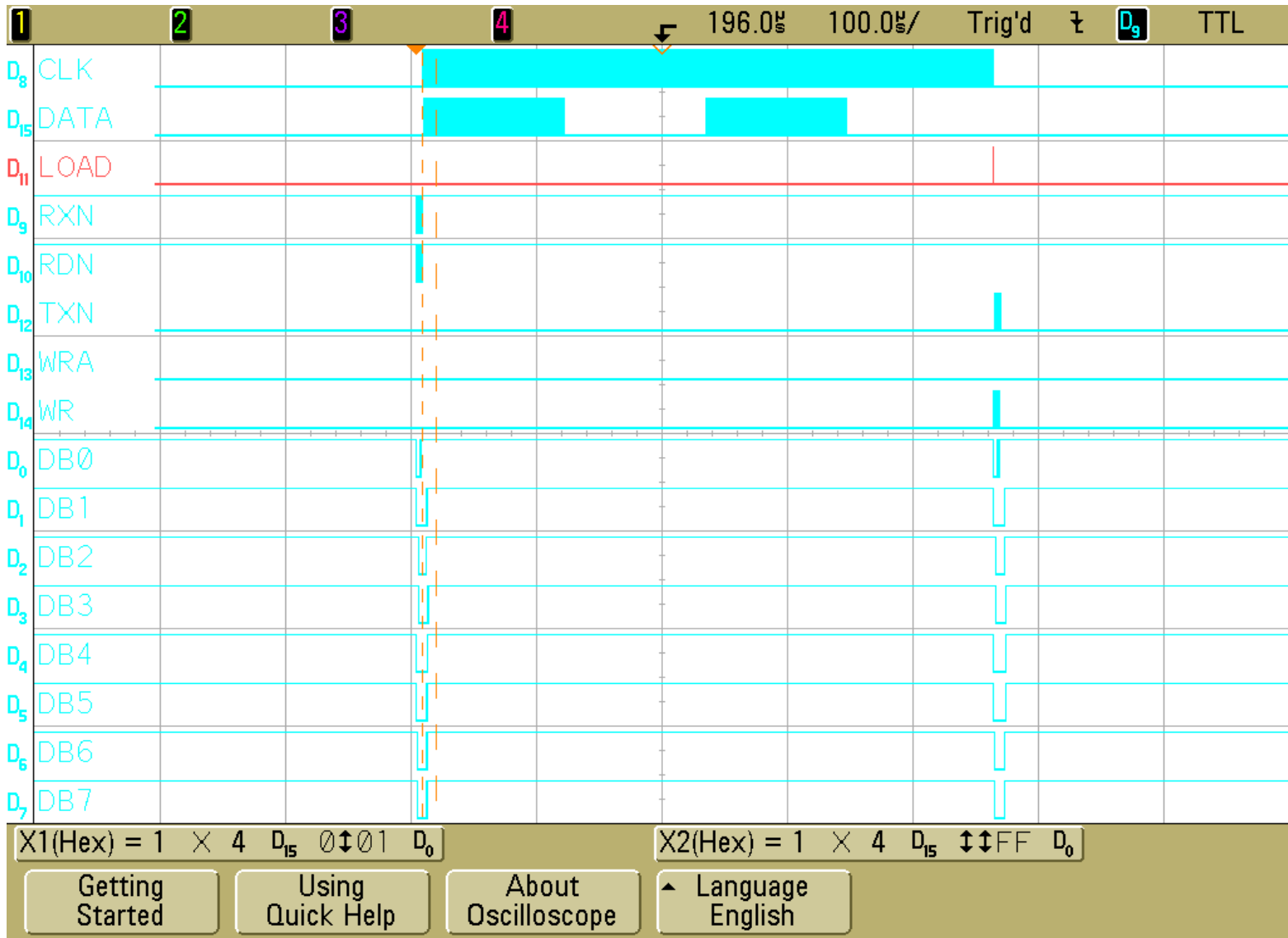
- ❑ Alternate versus Continual Mapping
 - ❑ Alternate Set 1/2
 - ❑ Alternate Chain 1/2/3/4

- ❑ Block size 128 bytes - 88 used / 40 free

- ❑ 88 bytes - 704 bits
 - we skip 1 bit from 1 byte



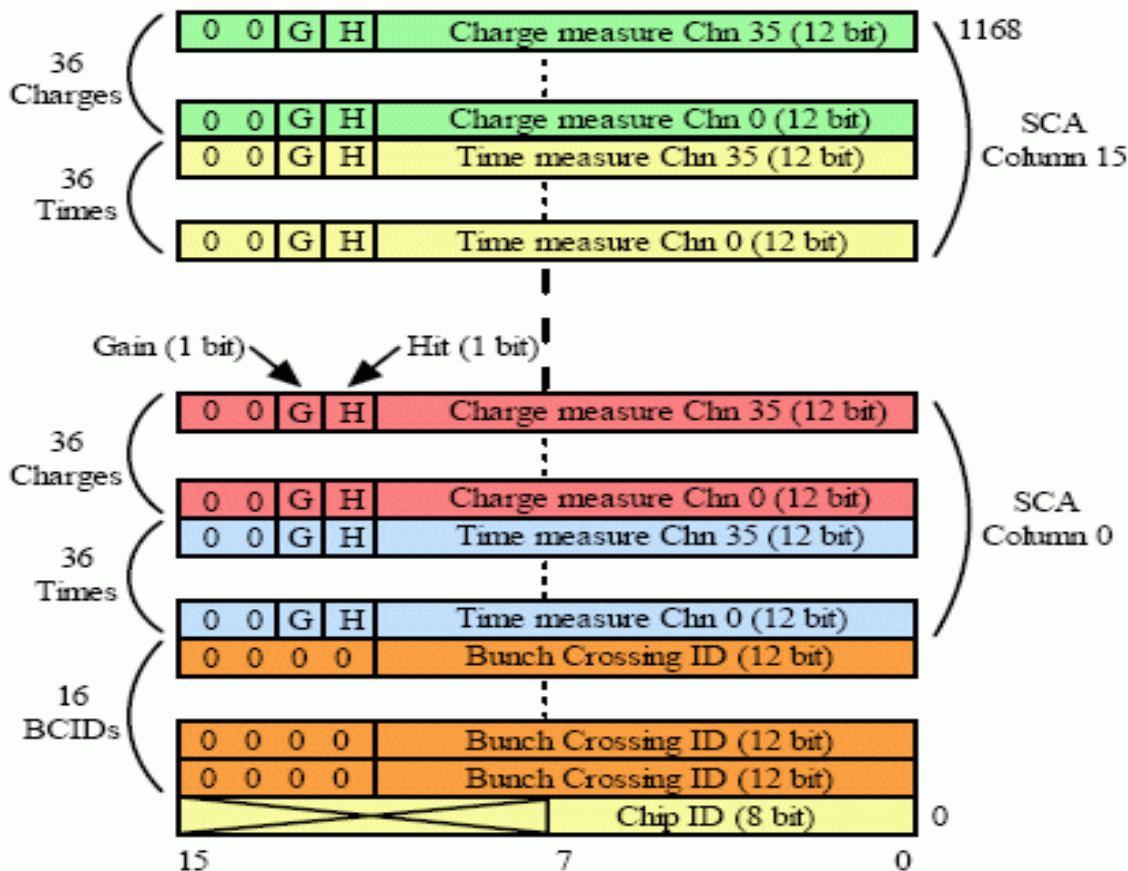
SC Load DIF to ASIC's



DATASHEET

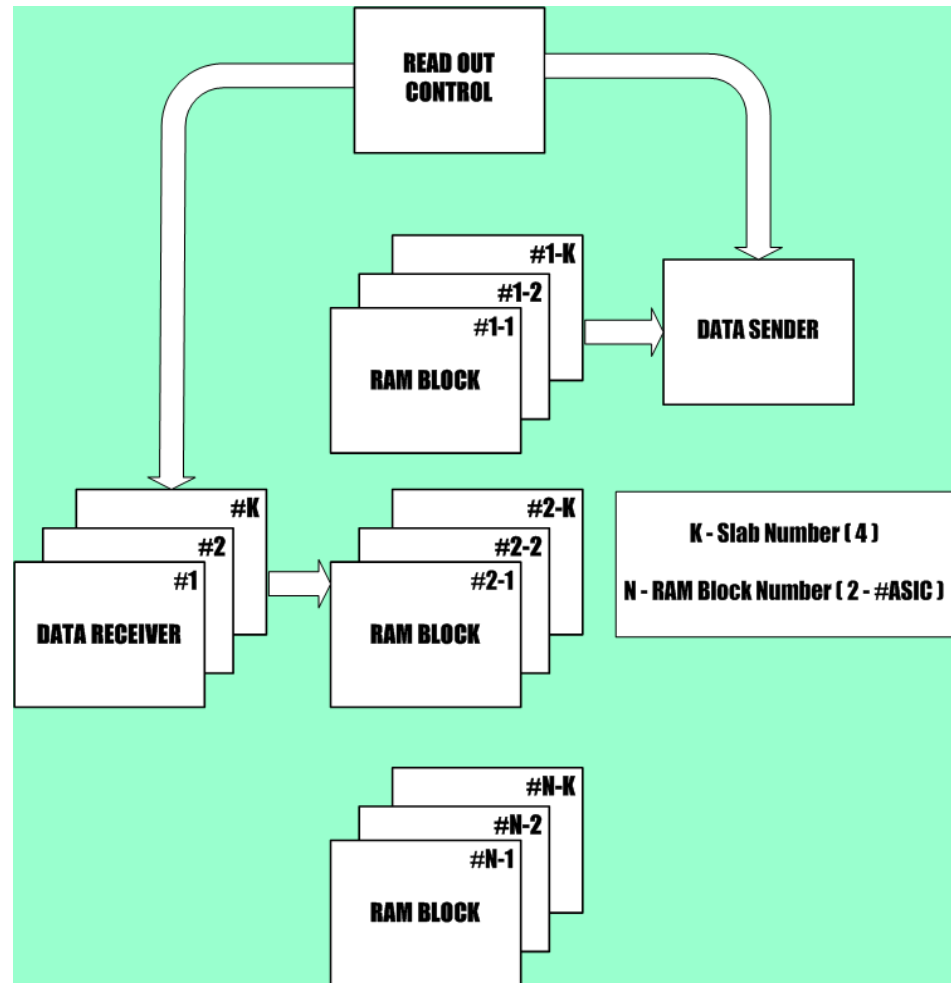


12 Spiroc RAM mapping



- ❑ Dual Port Memory
 - ❑ More effective using of the memory space

- ❑ RAM Block FIFO
 - ❑ Data reordering
 - ❑ Data reduction (global cut, local cut, area cut)



- ❑ Counter solution
 - ❑ Counter step definition (100us - 12bits, 1us - 18bits)
 - ❑ Synchronisation
 - ❑ Register definition (1 ON, 1 OFF, 1 default value)
 - ❑ Common counter for RO / Power Signals
- ❑ LUT solution
 - ❑ After table loading no more setup needed