DIF Firmware Development

Status

Presented by Frantisek Krivan

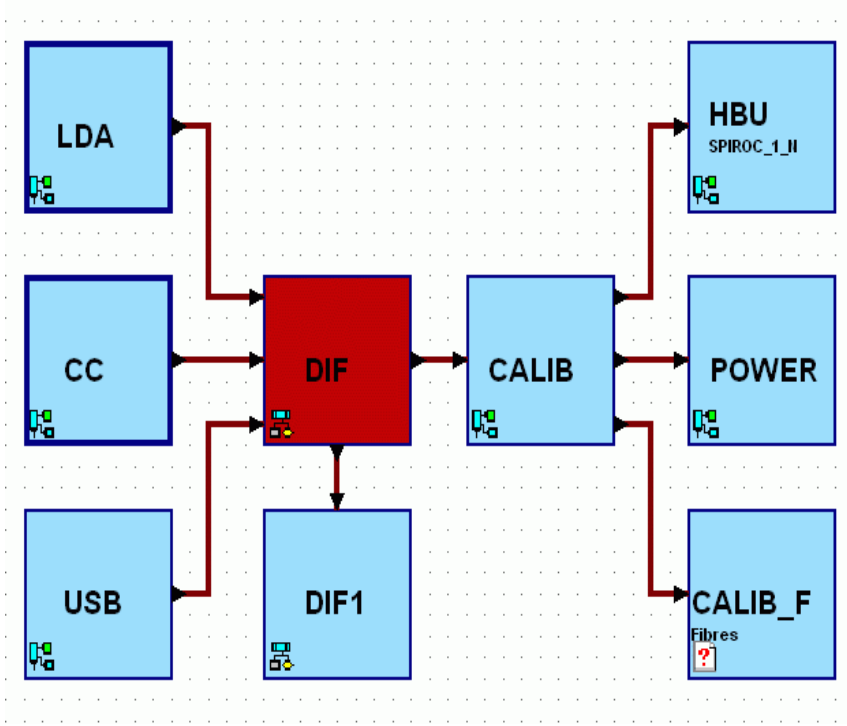
Development Sequence

- Definition of the DIF communication with other parts of the system
- Base DIF firmware development for lab tests
- Beam test modification
- DIF communication with LDA and C&C
- Readout modification
- Standardization

DIF - Signals Definition

(25/02/2008)

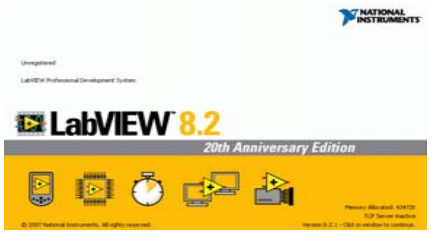
- LDA
- C&C – machine clock and fast signals
- DIF - redundancy against loss of LDA link
- Slab – SPIROC ASIC
- Calib module
- Power module

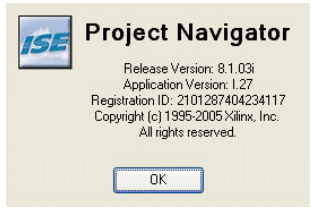


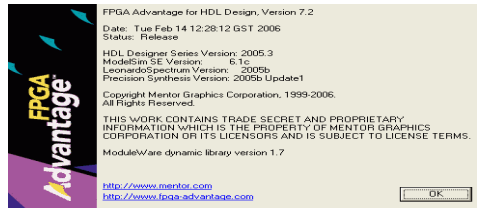
DIF Documents

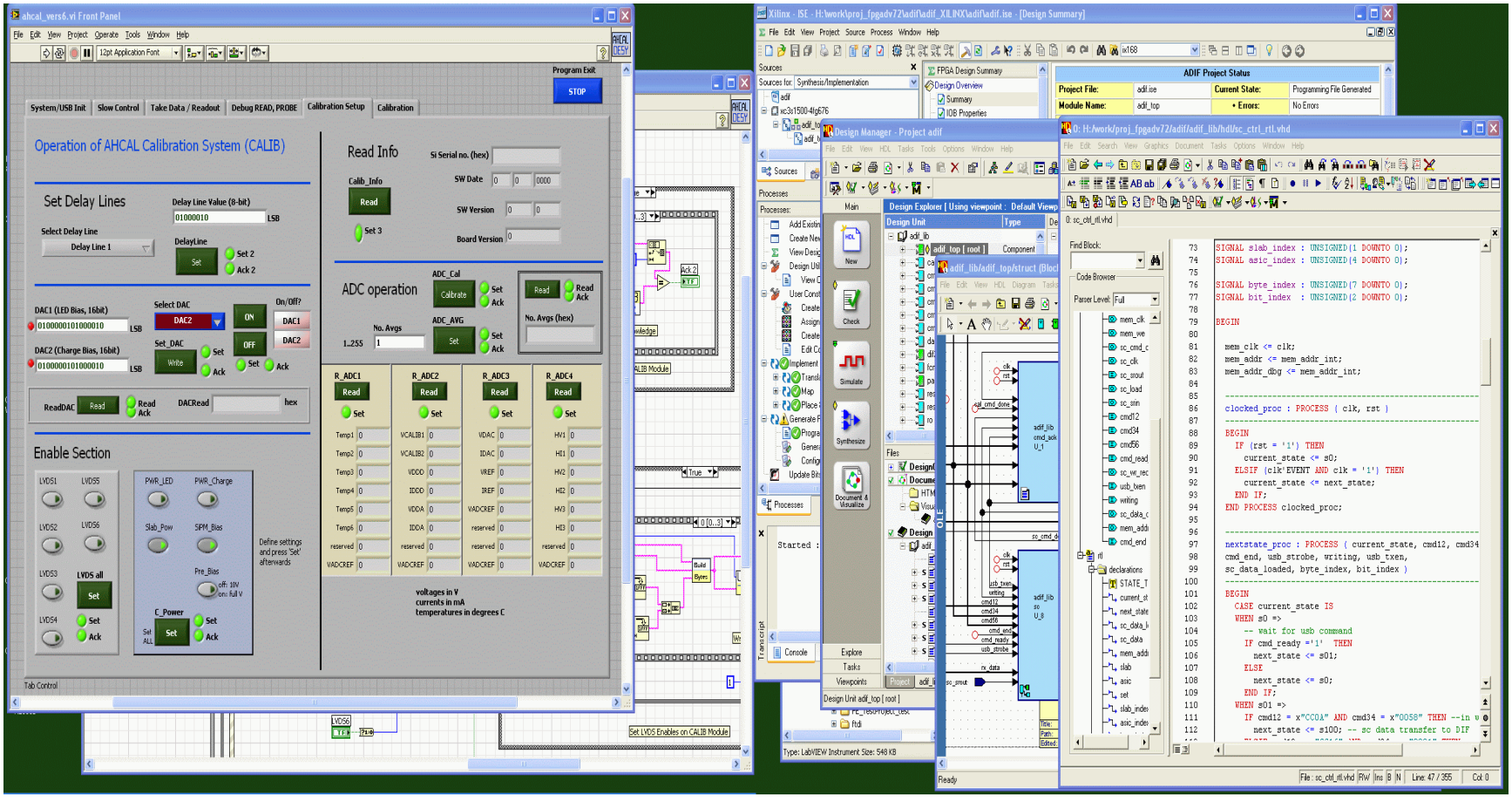
- DIF Commands Proposal
- DIF - ASIC Timing diagrams
- DIF Development for ECAL, DCAL
- SPIROC I. and II. Technical Information – Omega Webpage
- Calice LDA Docs - Marc Kelly
- Format of the read-out data of the DIF
- E-mail discussions
- Spartan Docs, USB Docs, SPI Docs, …
- …

Software Environment









Hardware Sandbox

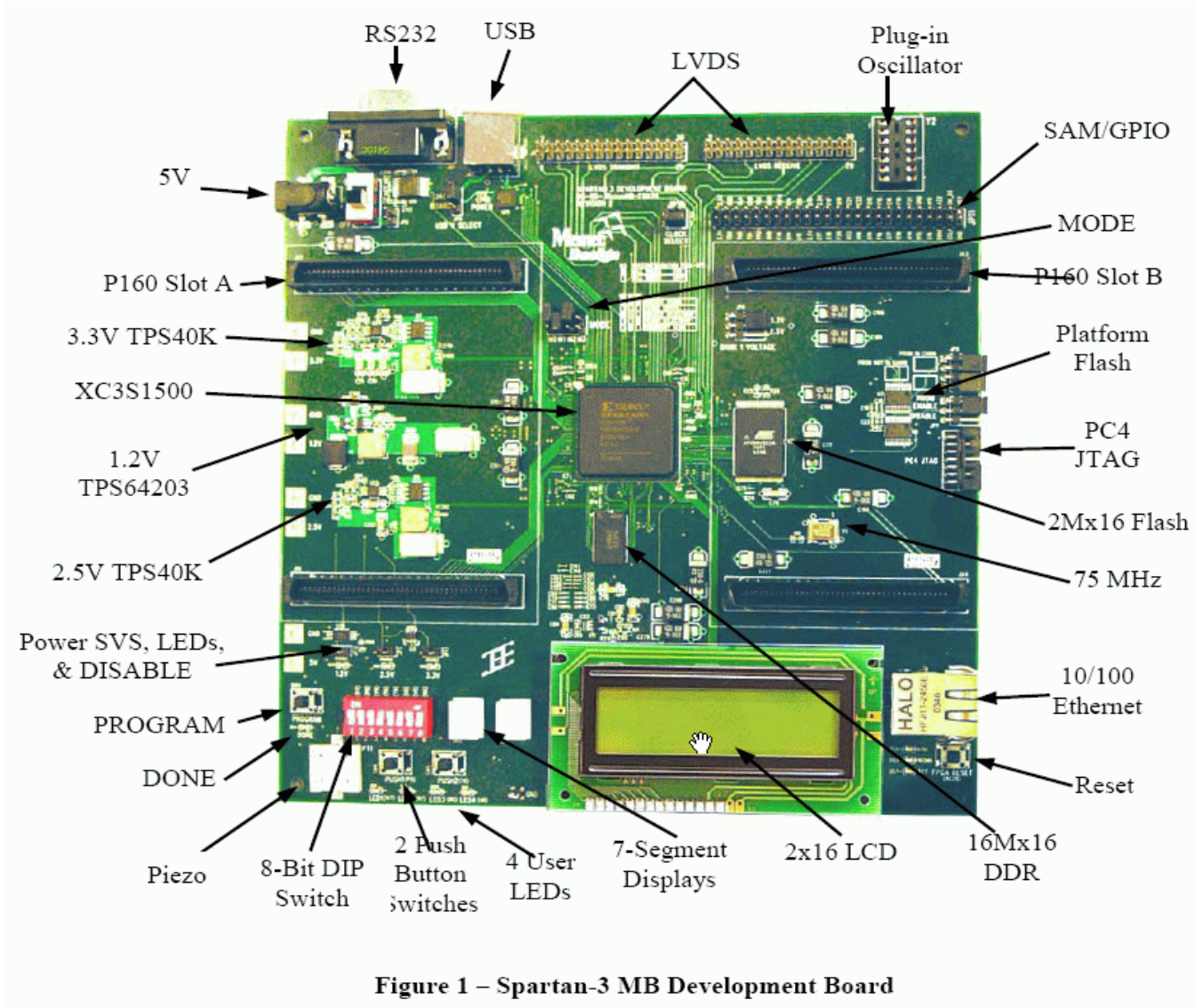
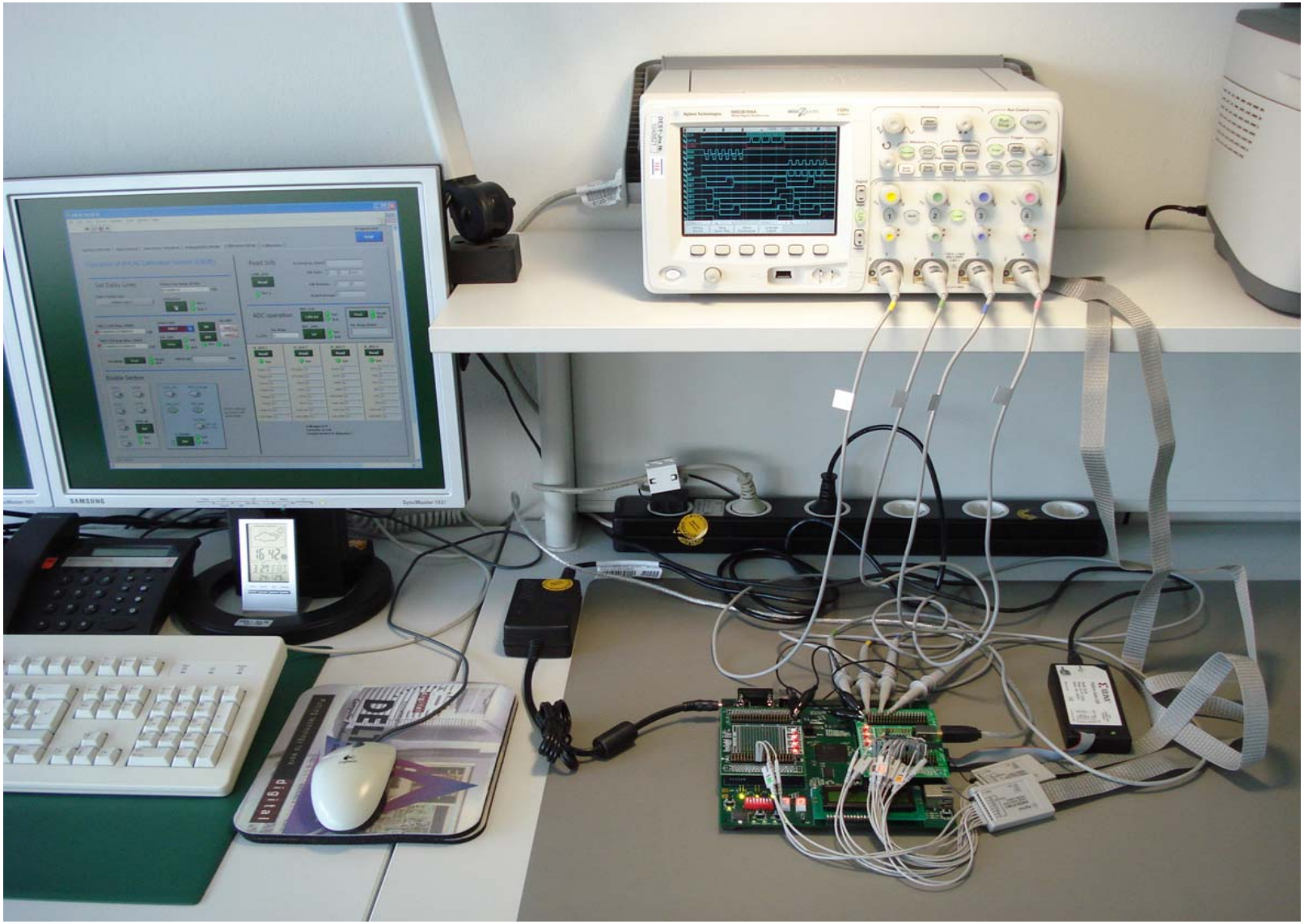


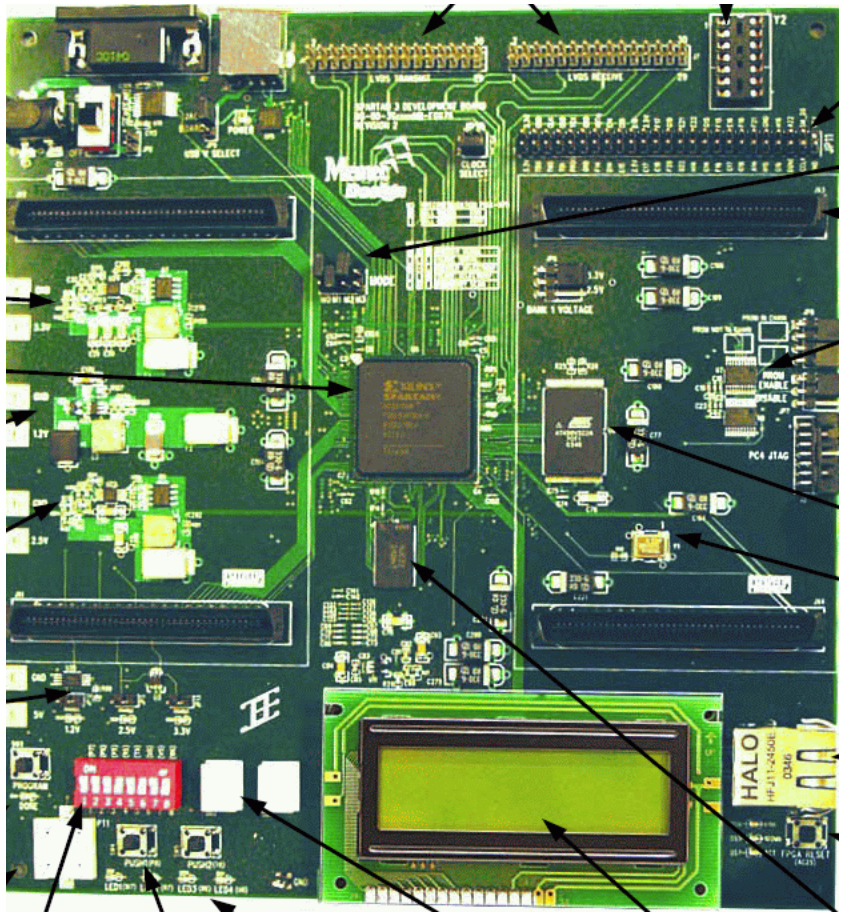
Figure 1 – Spartan-3 MB Development Board

Hardware Sandbox II.



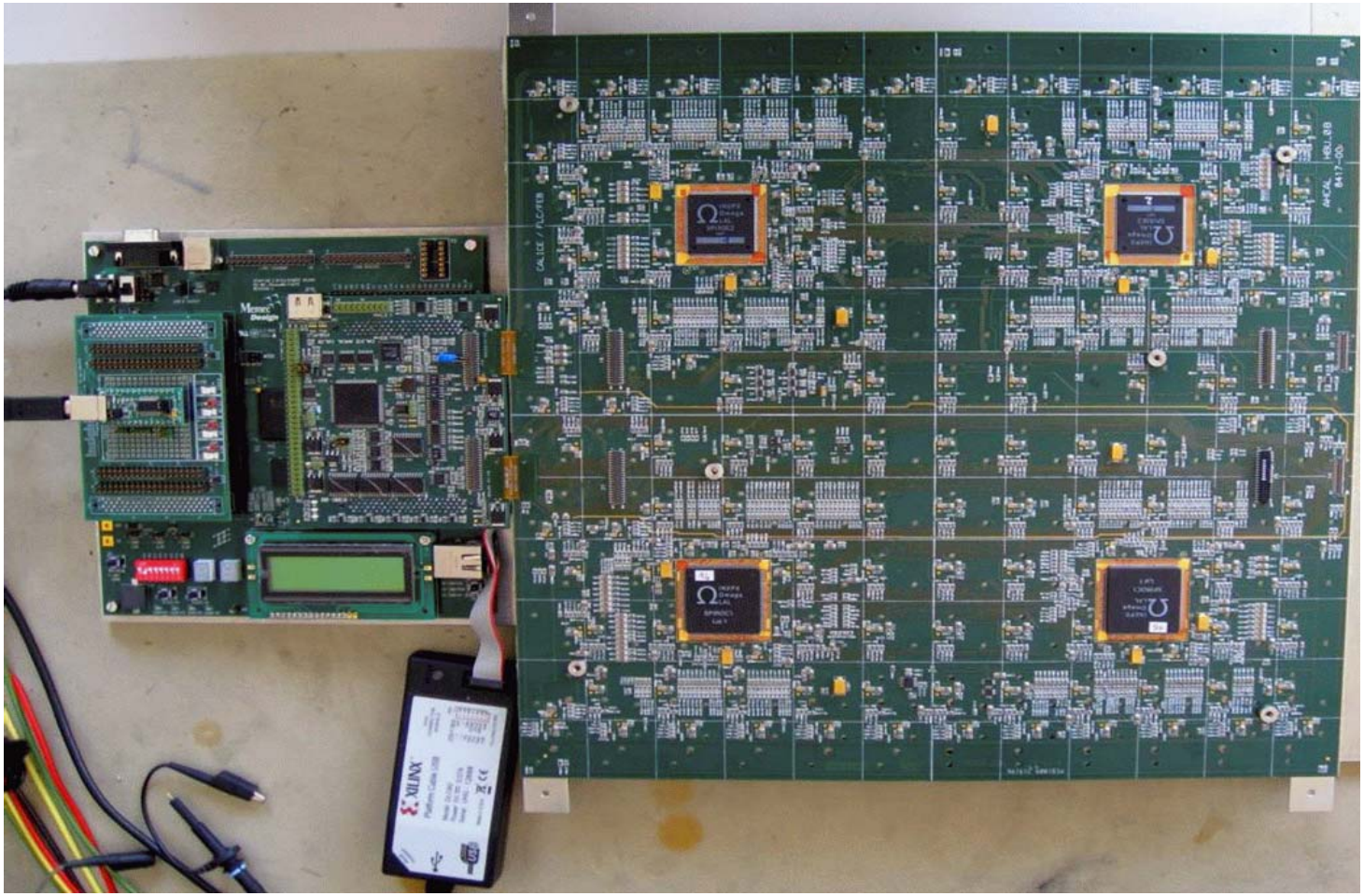
DIF Firmware
Real or Virtual? Status and Comments
(31/03/2009)

Imagine there's
(no) LDA
it's easy
if you try,
...

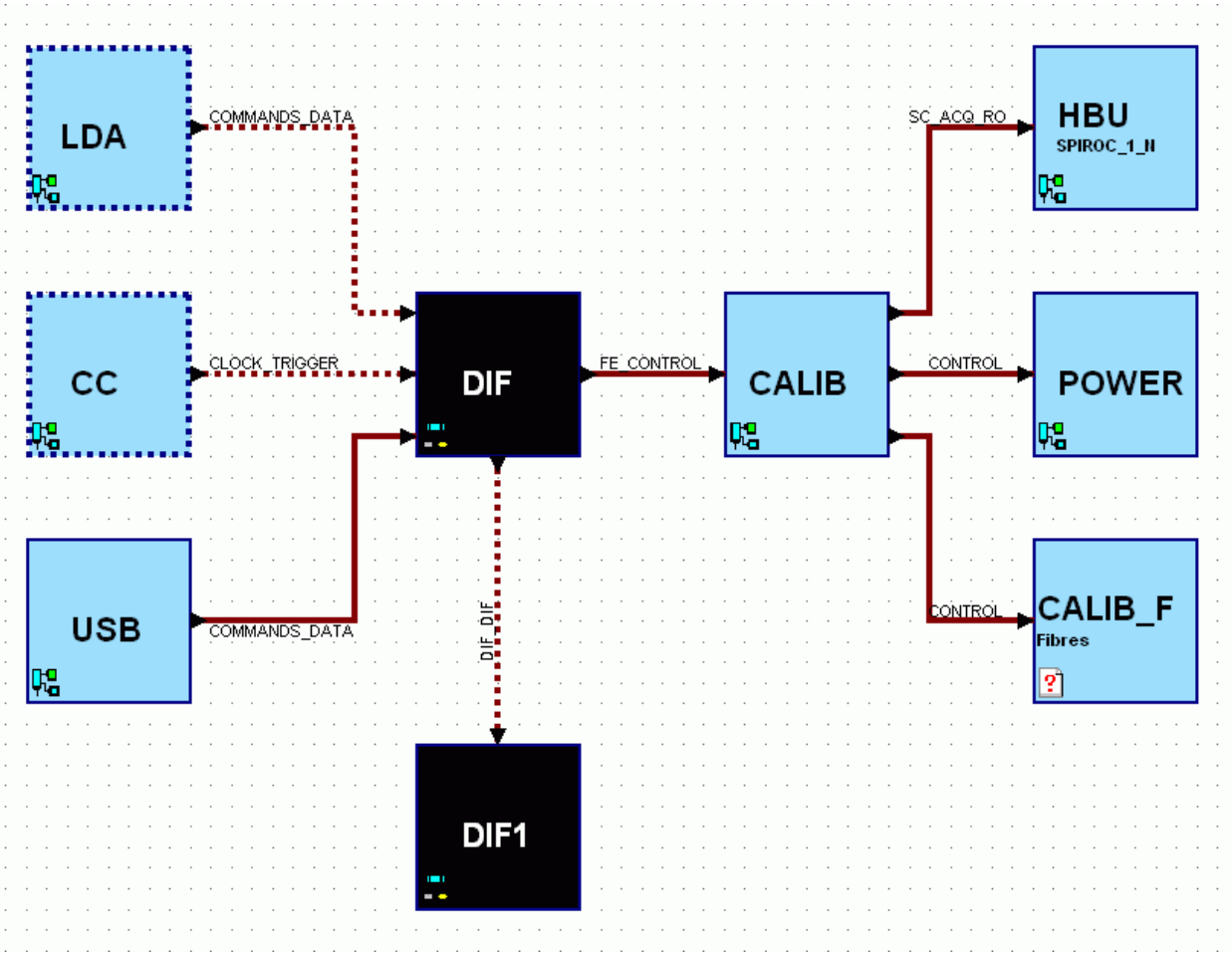


Imagine there's
(no) SPIROC
it's easy
if you try,
...

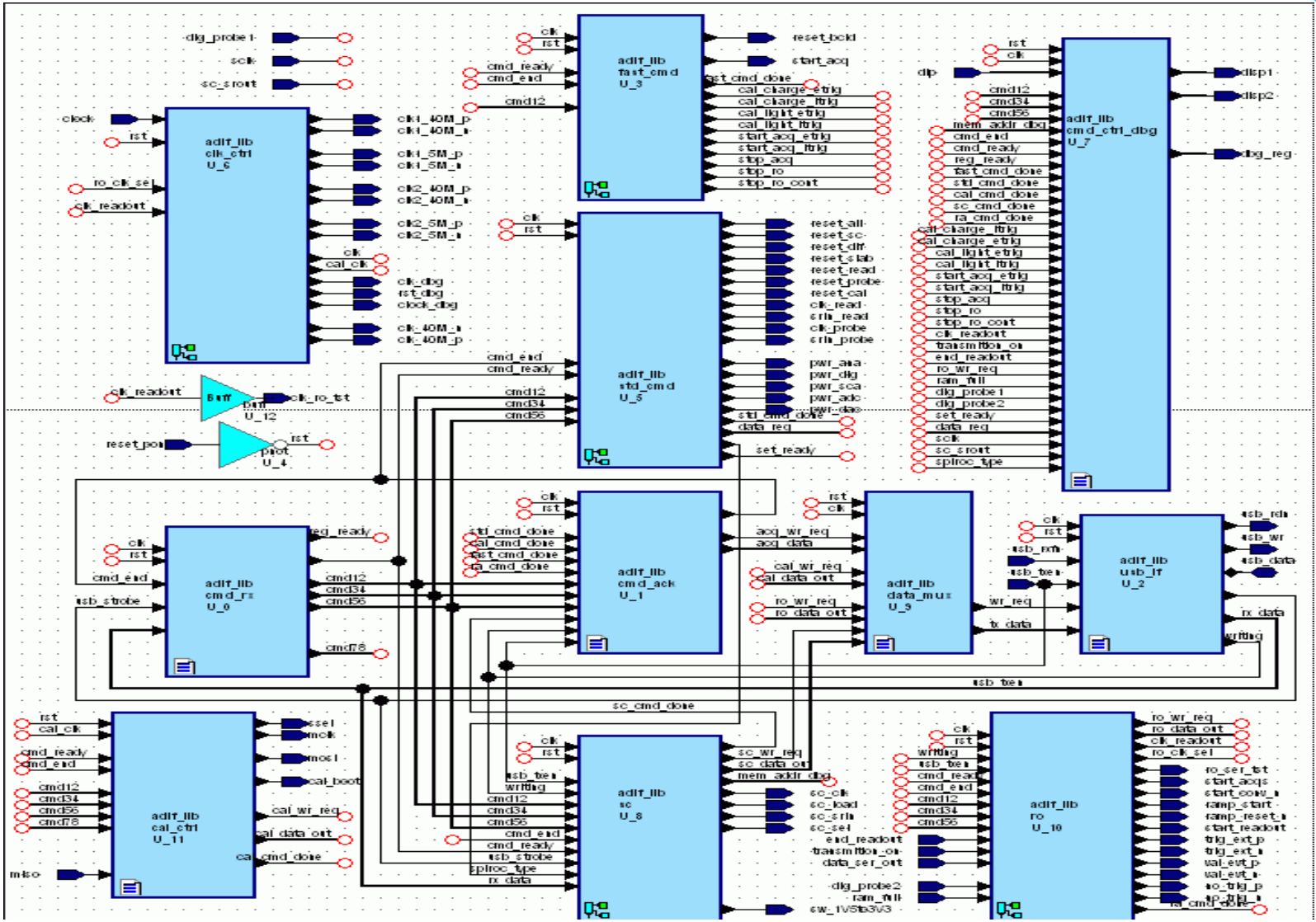
DIF, HBU, CALIB, …



BLOCK DIAGRAM



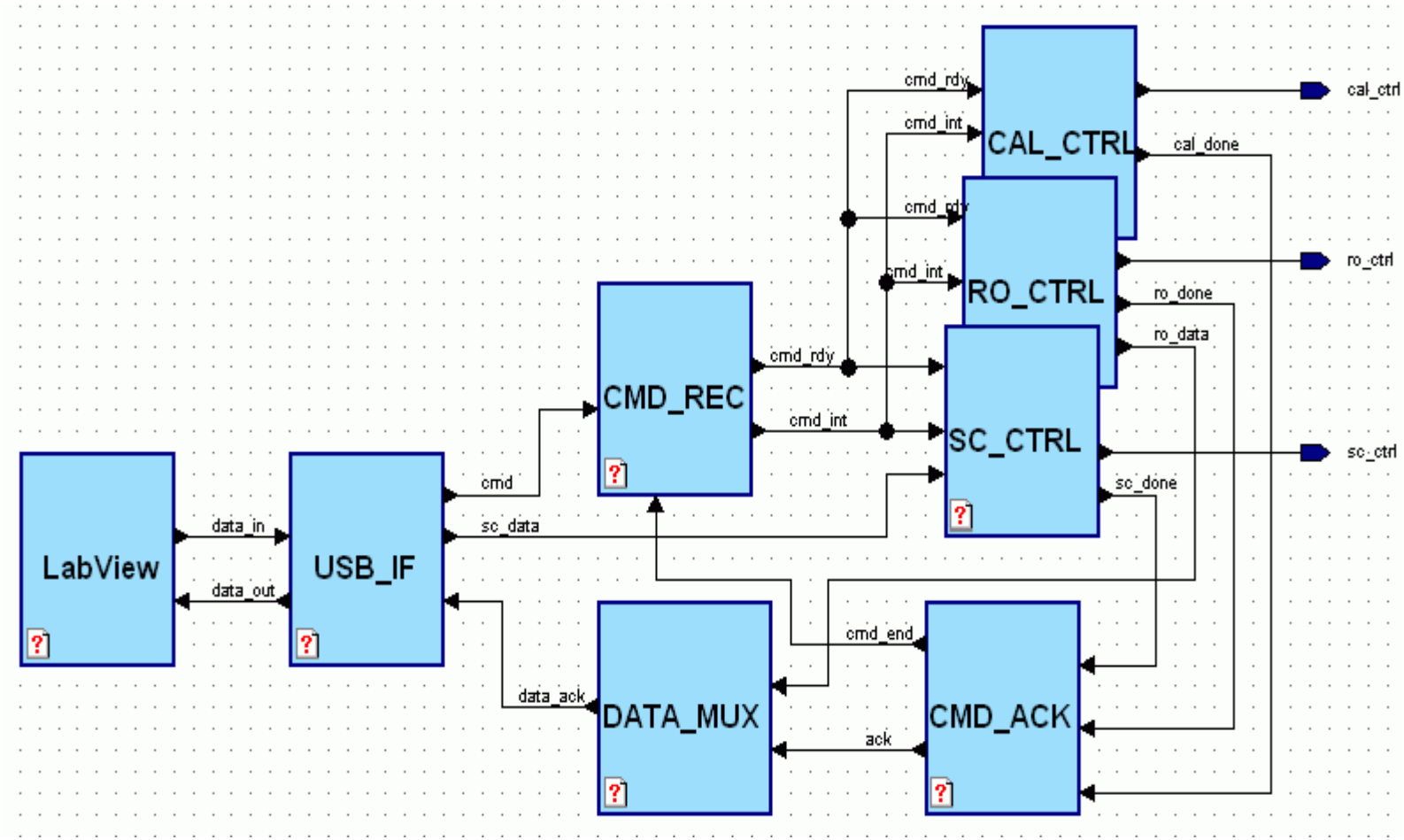
DIF Top Hierarchy



DIF Design Hierarchy

Design Hierarchy	Design Unit Na...	Name	Language	Size
adif_top	adif_top	adif_top	VHDL	73 KB
adif_top	adif_top	adif_top	VHDL	73 KB
struct [root]	adif_top	adif_top(struct)	VHDL	230 KB
U_0	cmd_rx	cmd_rx(rtl)	VHDL '93	6 KB
U_1	cmd_ack	cmd_ack(rtl)	VHDL '93	6 KB
U_10	ro	ro(struct)	VHDL	92 KB
U_0	ro_ctrl	ro_ctrl(rtl)	VHDL '93	15 KB
U_2	acq_ctrl	acq_ctrl(struct)	VHDL '93	10 KB
U_11	cal_ctrl	cal_ctrl(rtl)	VHDL '93	10 KB
U_2	usb_if	usb_if(rtl)	VHDL '93	3 KB
dif2usb_...	dif2usb	dif2usb(rtl)	VHDL '93	3 KB
usb2dif_...	usb2dif	usb2dif(rtl)	VHDL '93	3 KB
U_3	fast_cmd	fast_cmd(struct)	VHDL	50 KB
U_0	fast_cmd_dec	fast_cmd_dec(rtl)	VHDL '93	6 KB
U_5	std_cmd	std_cmd(struct)	VHDL	76 KB
U_0	std_cmd_dec	std_cmd_dec(rtl)	VHDL '93	14 KB
U_1	pwr_ctrl	pwr_ctrl(rtl)	VHDL '93	5 KB
U_6	clk_ctrl	clk_ctrl(struct)	VHDL	154 KB
U_20	clk_gen	clk_gen(struct)	VHDL '93	3 KB
U_7	cmd_ctrl_dbg	cmd_ctrl_dbg(rtl)	VHDL '93	9 KB
U_8	sc	sc(struct)	VHDL	67 KB
U_1	sc_ctrl	sc_ctrl(rtl)	VHDL '93	15 KB
U_9	data_mux	data_mux(rtl)	VHDL '93	2 KB

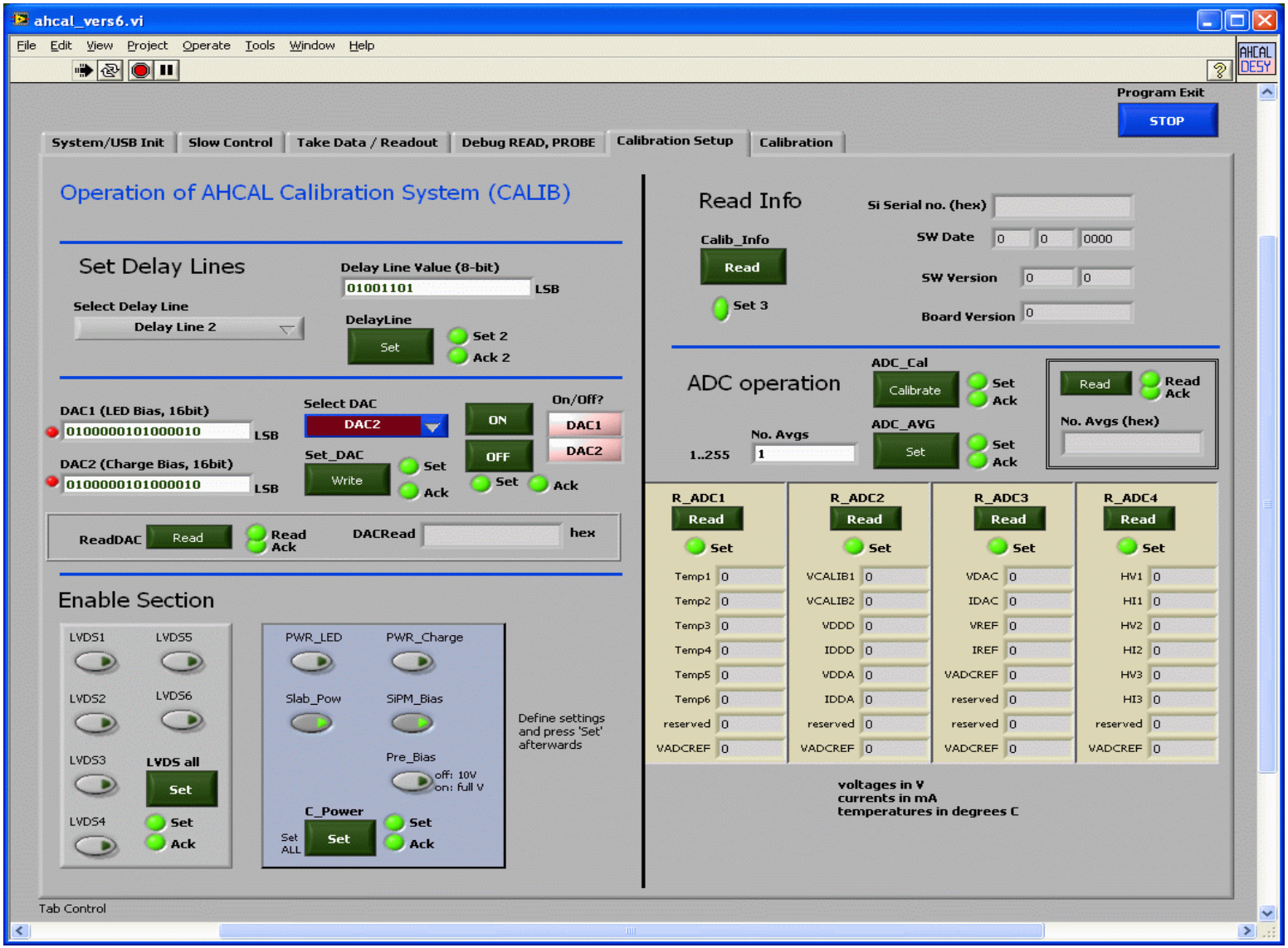
Command Flow



DIF Commands Set

- Fast Commands
- Standard Commands
- Slow Control Commands
- Acquisition and Readout Commands
- Calib Commands

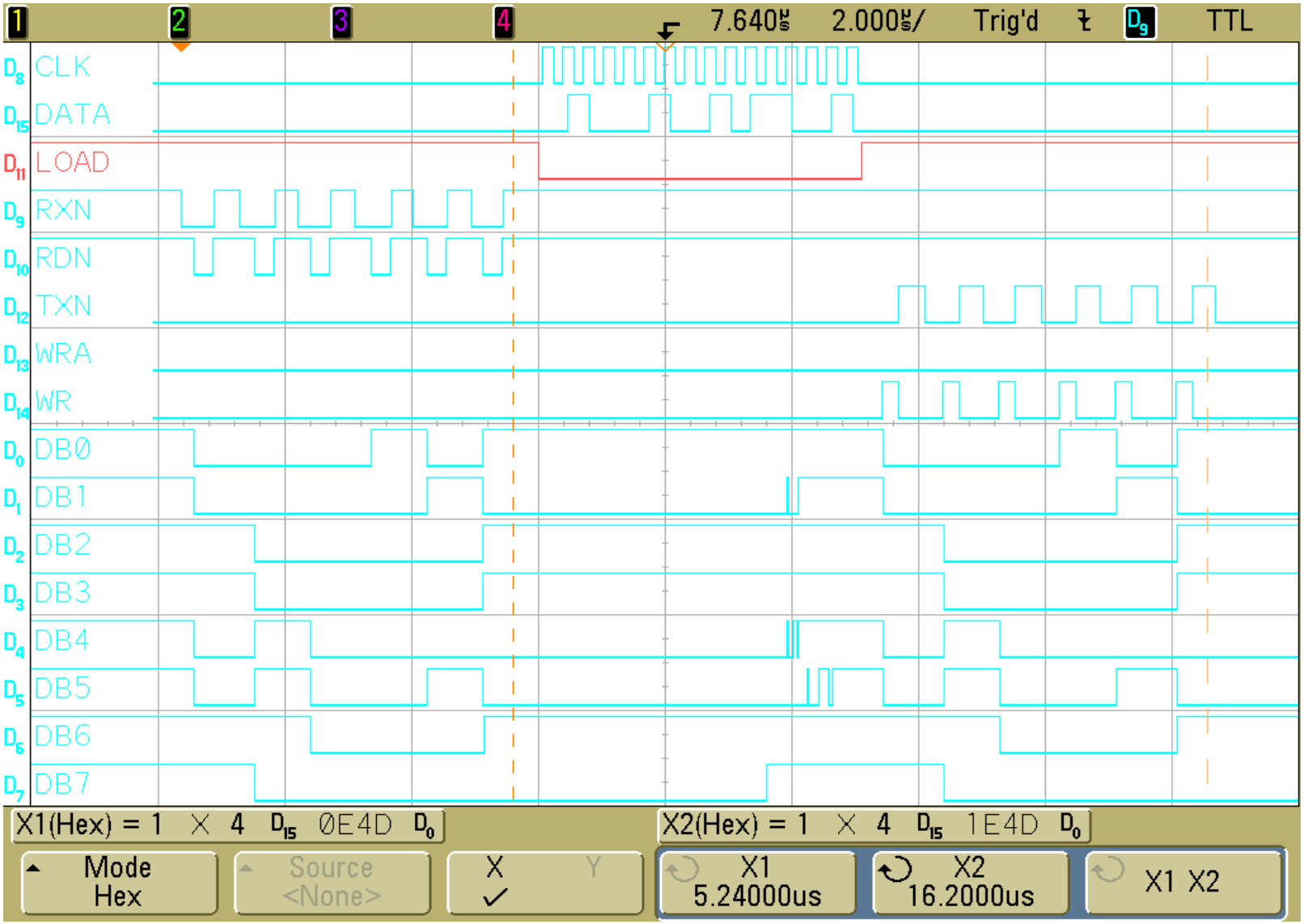
SPI Commands - LabView



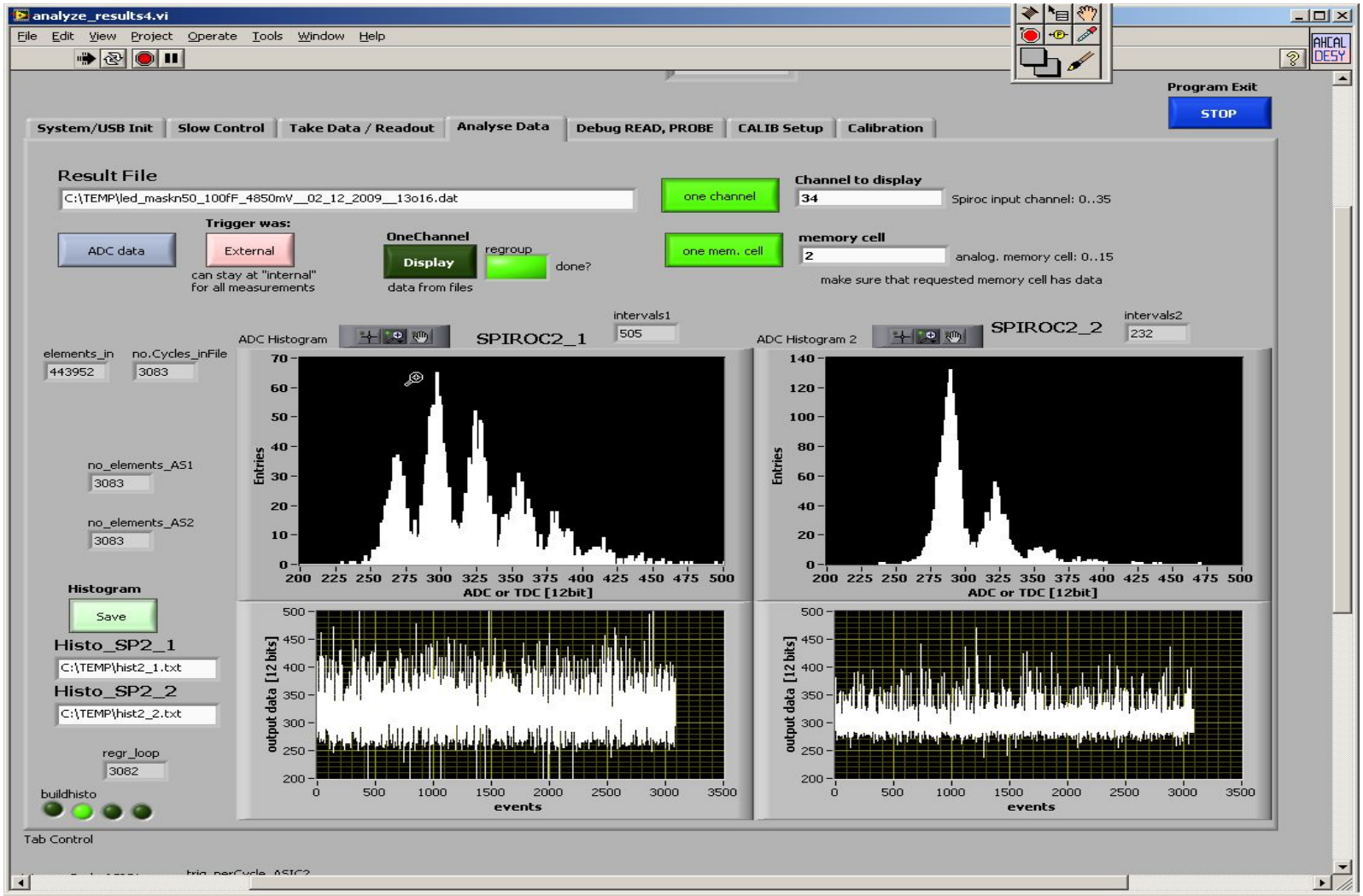
SPI Commands Table (Part)

SPI Commands for CALIB Board from DIF Board					
Command:	**Hex**	**Data**		**Return Value**	
Group 1:		**System informationen**			
Read Silicon Serial Number	0x11	--	--	6 Byte	SiliconNumber
Read Software data	0x12	--	--	4 Byte	Datum: DD MM JJJJ
Read Software version	0x13	--	--	1 Byte	0.0 - 15.15 (0xFF)
Read Board version	0x14	--	--	1 Byte	0 - 31
Group 2:		**Set Delay Line**			
Set DelayLine 1	0x21	1 Byte	0-255	--	--
Set DelayLine 2	0x22	1 Byte	0-255	--	--
Set DelayLine 3	0x23	1 Byte	0-255	--	--
Group 3:		**Enable Transmitter and Power**			
Enable LVDS Repeat en_1	0x31	1 Byte	0 or 1	--	--
Enable LVDSTransm. en_2	0x32	1 Byte	0 or 1	--	--
Enable LVDSTransm. en_3	0x33	1 Byte	0 or 1	--	--

SPI Command Example



Conclusion I.



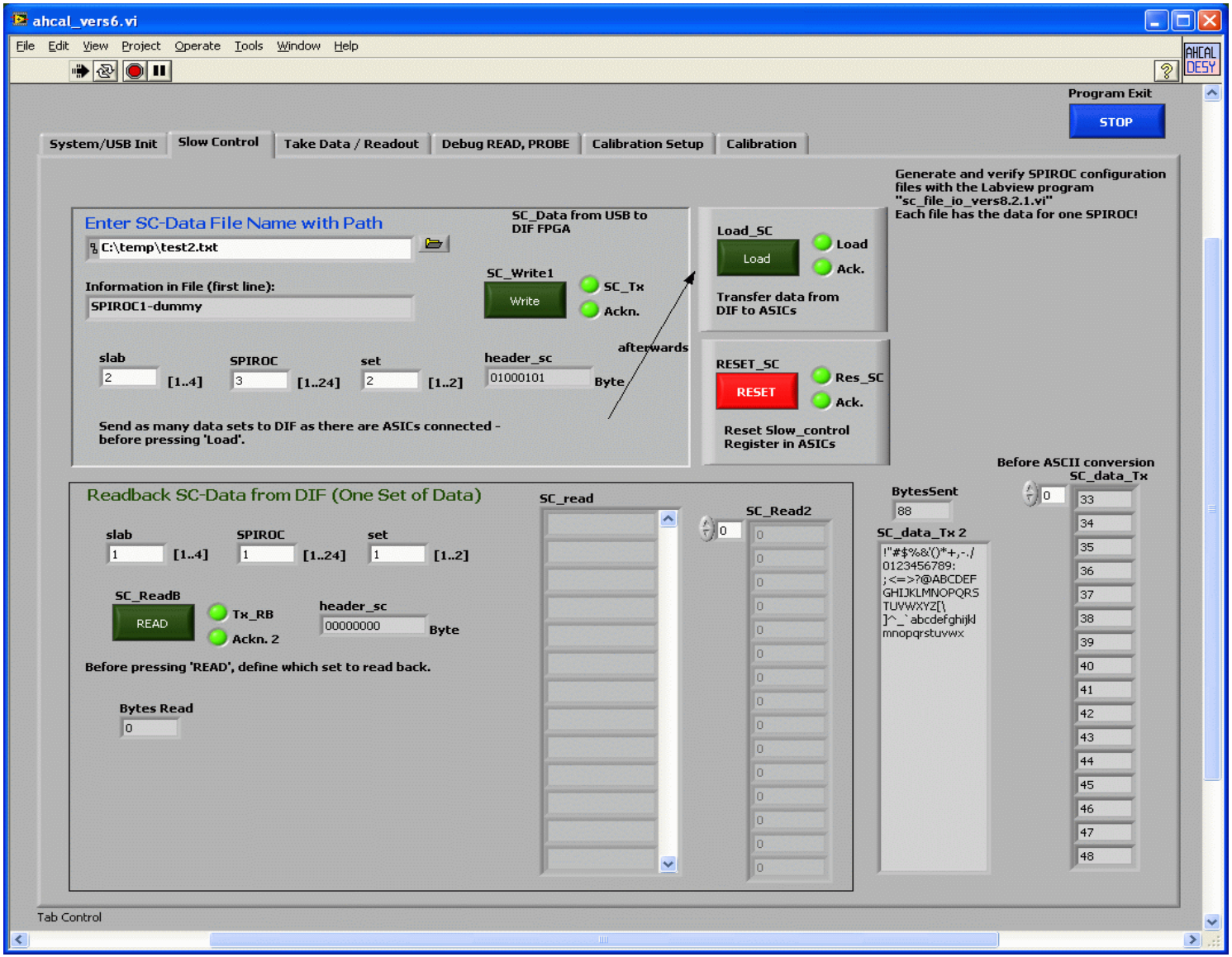
- It works !

Conclusions II.

Need to be done :

- **Beam test modification**
- **DIF communication with LDA and C&C**
- **Readout modification (circular buffer, dual port memory)**

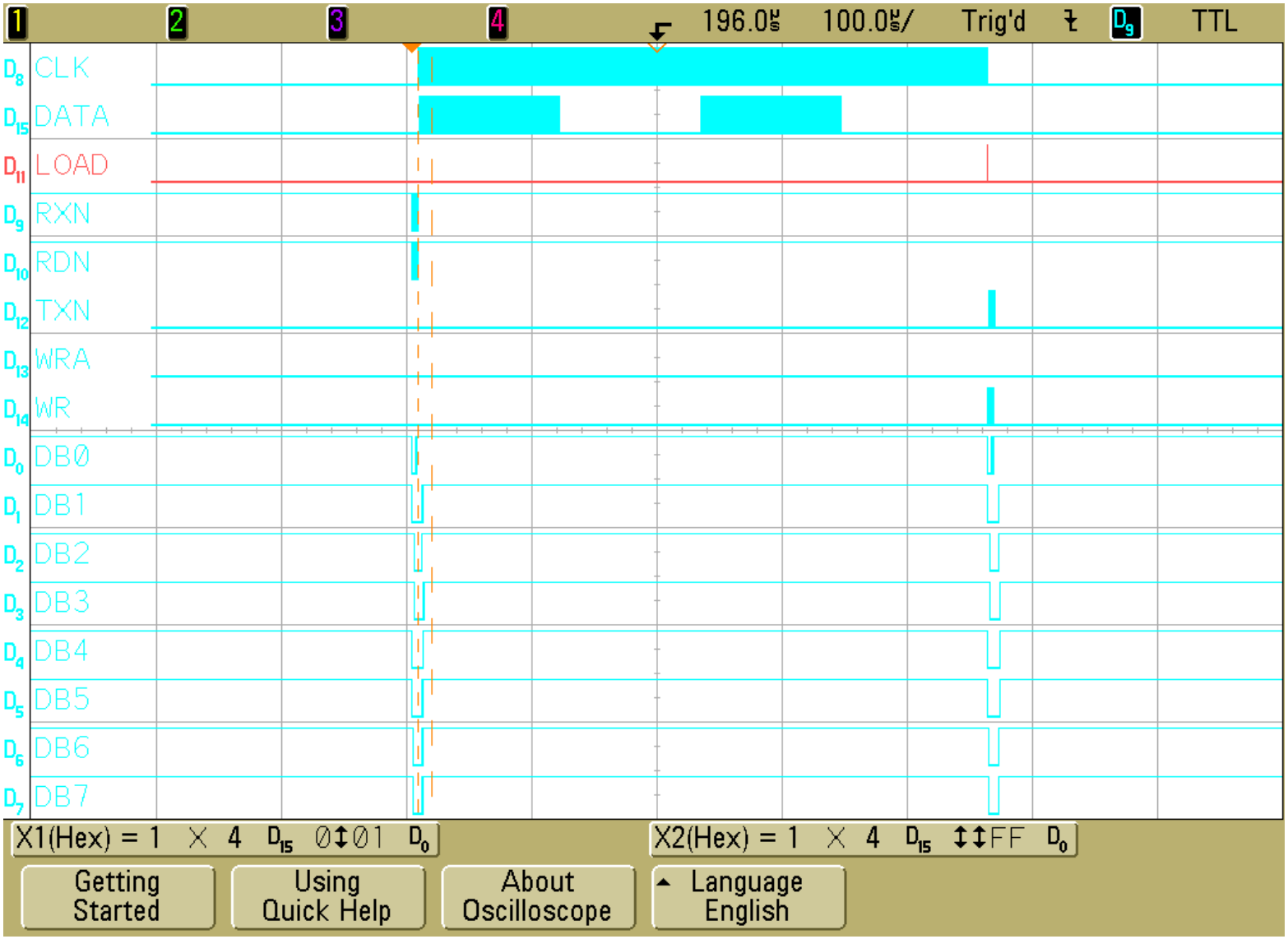
SC LabView


ahcal_vers6.vi
File Edit View Project Operate Tools Window Help
Program Exit
STOP
System/USB Init
Slow Control
Take Data / Readout
Debug READ, PROBE
Calibration Setup
Calibration
Generate and verify SPIROC configuration files with the Labview program "sc_file_io_vers8.2.1.vi" Each file has the data for one SPIROC!
Enter SC-Data File Name with Path
C:\temp\test2.txt
SC_Data from USB to DIF FPGA
Information in File (first line):
SPIROC1-dummy
SC_Write1
Write
SC_Tx
Ackn.
Load_SC
Load
Load
Ack.
Transfer data from DIF to ASICs
afterwards
slab
2
[1..4]
SPIROC
3
[1..24]
set
2
[1..2]
header_sc
01000101
Byte
RESET_SC
RESET
Res_SC
Ack.
Reset Slow_control Register in ASICs
Send as many data sets to DIF as there are ASICs connected - before pressing 'Load'.
Before ASCII conversion
SC_data_Tx
Readback SC-Data from DIF (One Set of Data)
SC_read
SC_Read2
BytesSent
88
SC_data_Tx 2
slab
1
[1..4]
SPIROC
1
[1..24]
set
1
[1..2]
SC_ReadB
READ
Tx_RB
Ackn. 2
header_sc
00000000
Byte
Before pressing 'READ', define which set to read back.
Bytes Read
0
Tab Control

SC Memory Mapping

- Parameters Size
  - Chain 1 – 4
  - ASIC 1 – 24
  - Set 1 -2
- Alternate versus Continual Mapping
  - Alternate Set 1/2
  - Alternate Chain 1/2/3/4
- Block size 128 bytes – 88 used / 40 free
- 88 bytes – 704 bits
  – we skip 1 bit from 1 byte

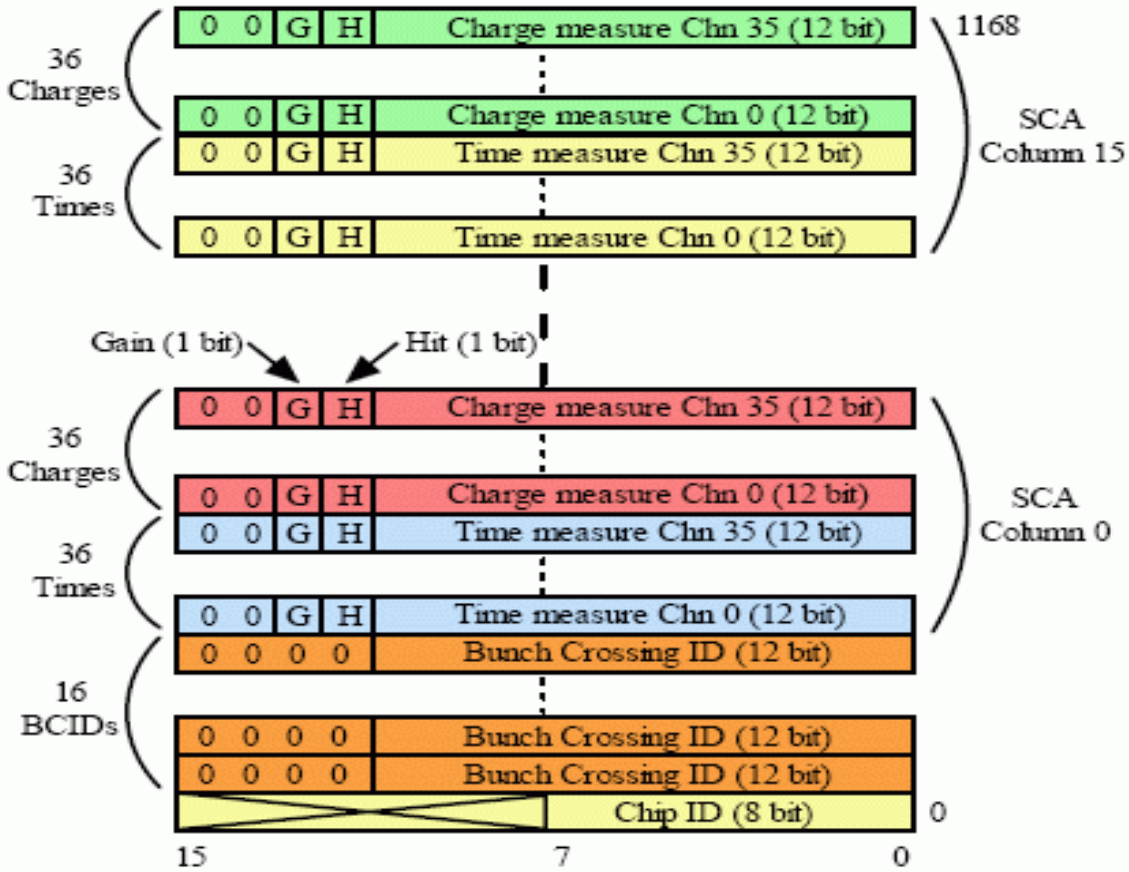
SC Load DIF to ASIC's



SPIROC RAM MAPPING

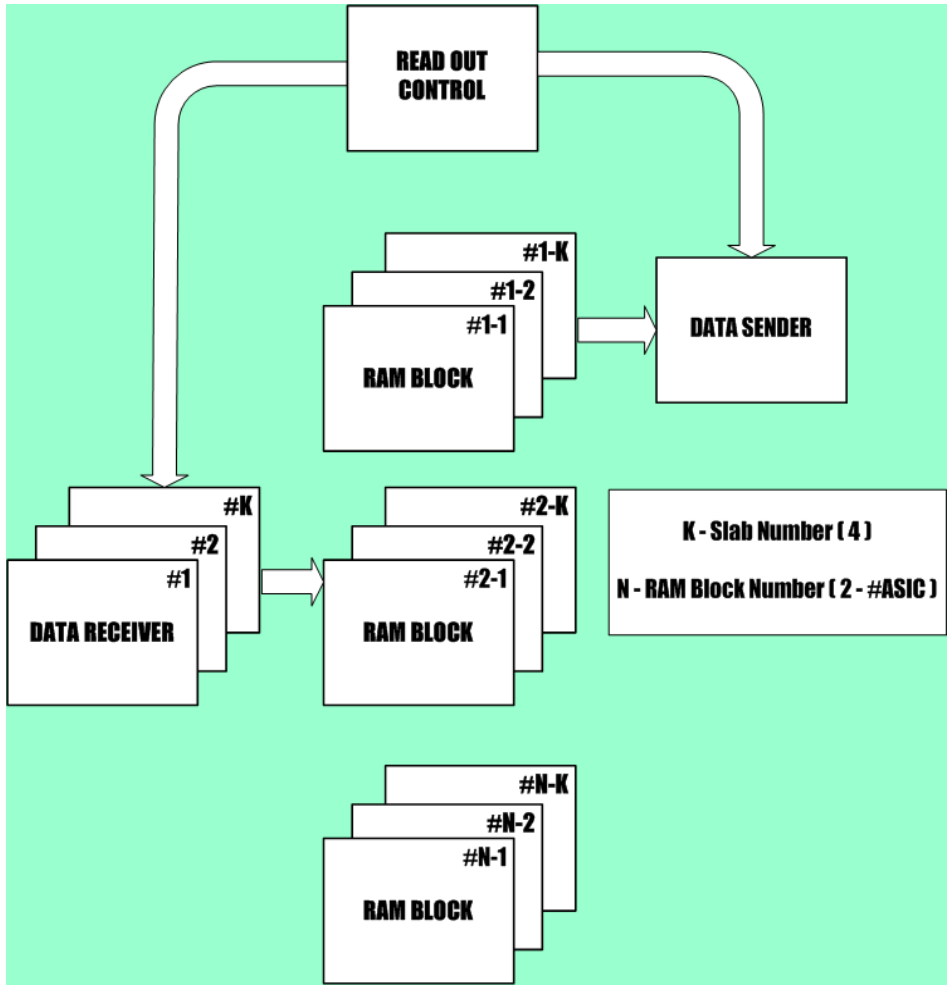
DATASHEET

12 Spiroc RAM mapping



Readout II.

- Dual Port Memory
  - More effective using of the memory space
- RAM Block FIFO
  - Data reordering
  - Data reduction (global cut, local cut, area cut)



Control Signals RO / Power

- Counter solution
  - Counter step definition (100us – 12bits, 1us – 18bits)
  - Synchronisation
  - Register definition (1 ON, 1 OFF, 1 default value)
  - Common counter for RO / Power Signals
- LUT solution
  - After table loading no more setup needed