Forward Calorimetry readout and DAQ status

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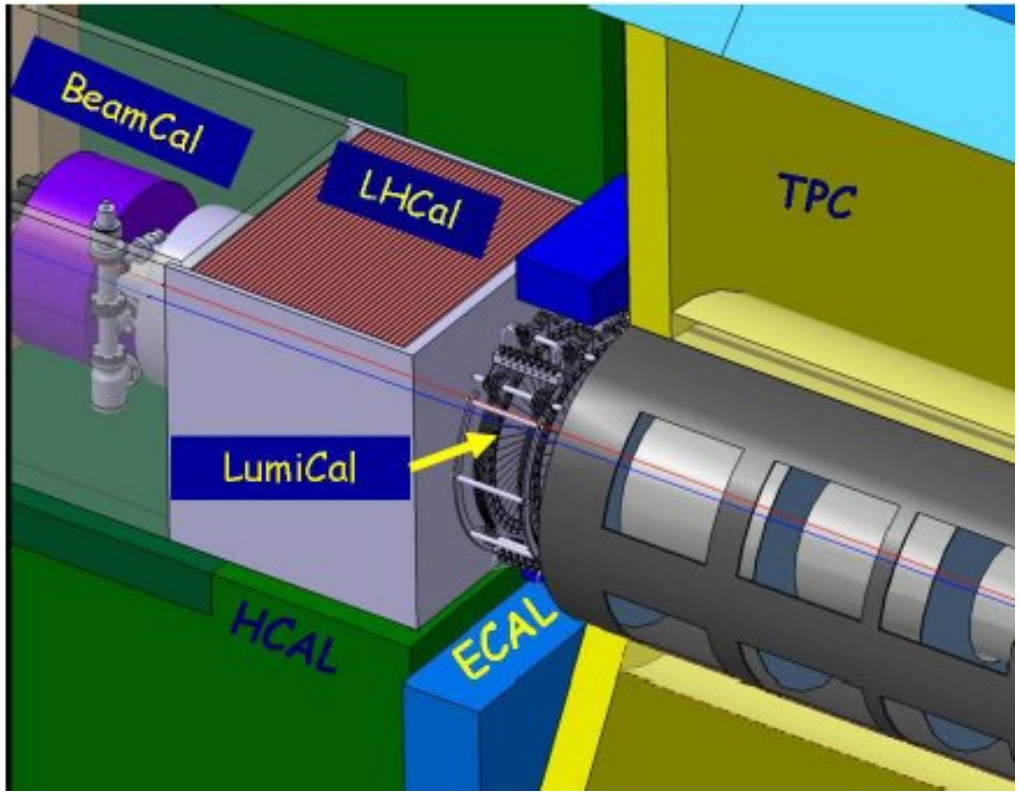
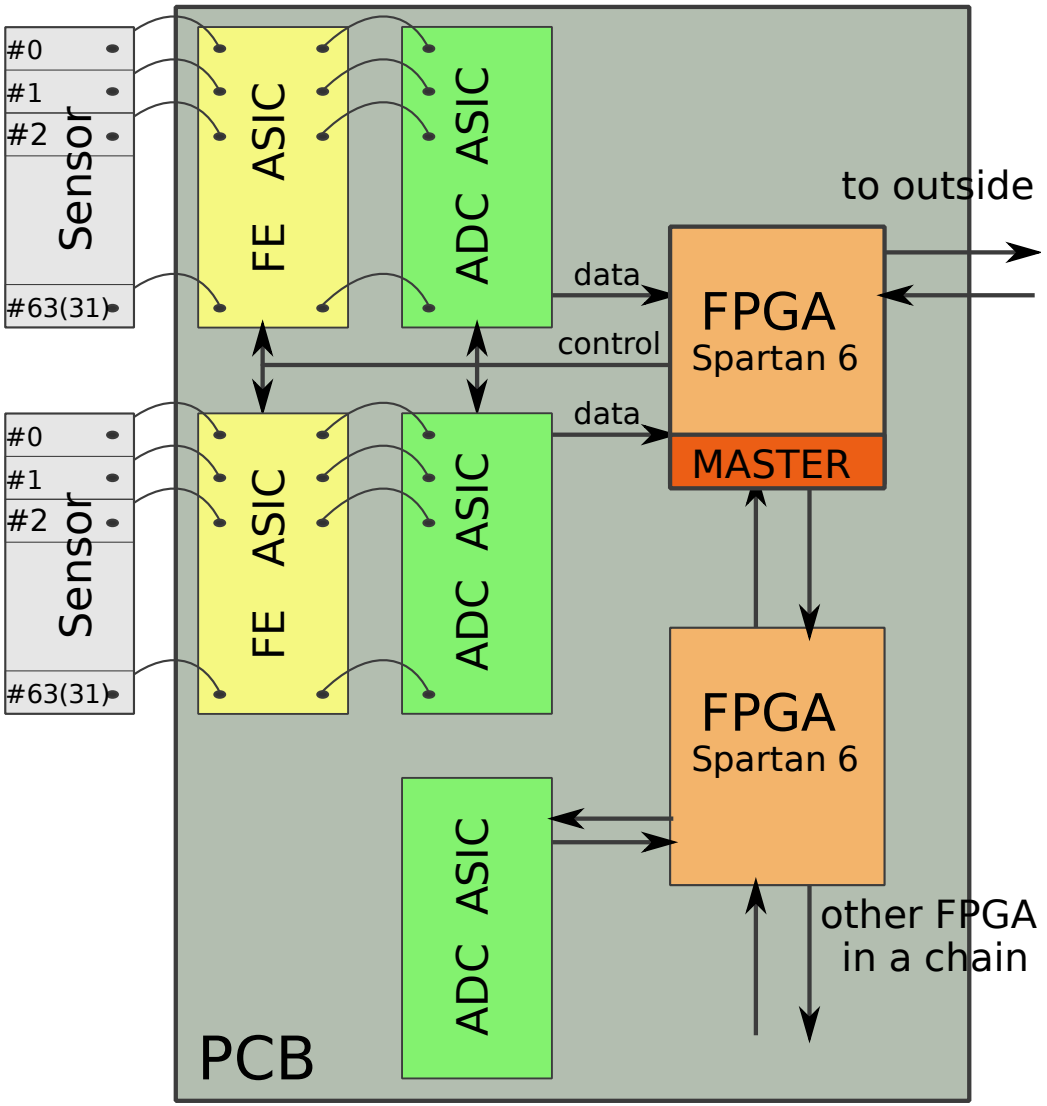
Outline

1. LumiCal
2. Other forward sub-detectors
   - BeamCal
   - Pair-Monitor in front of BeamCal
   - LHCal
3. Summary

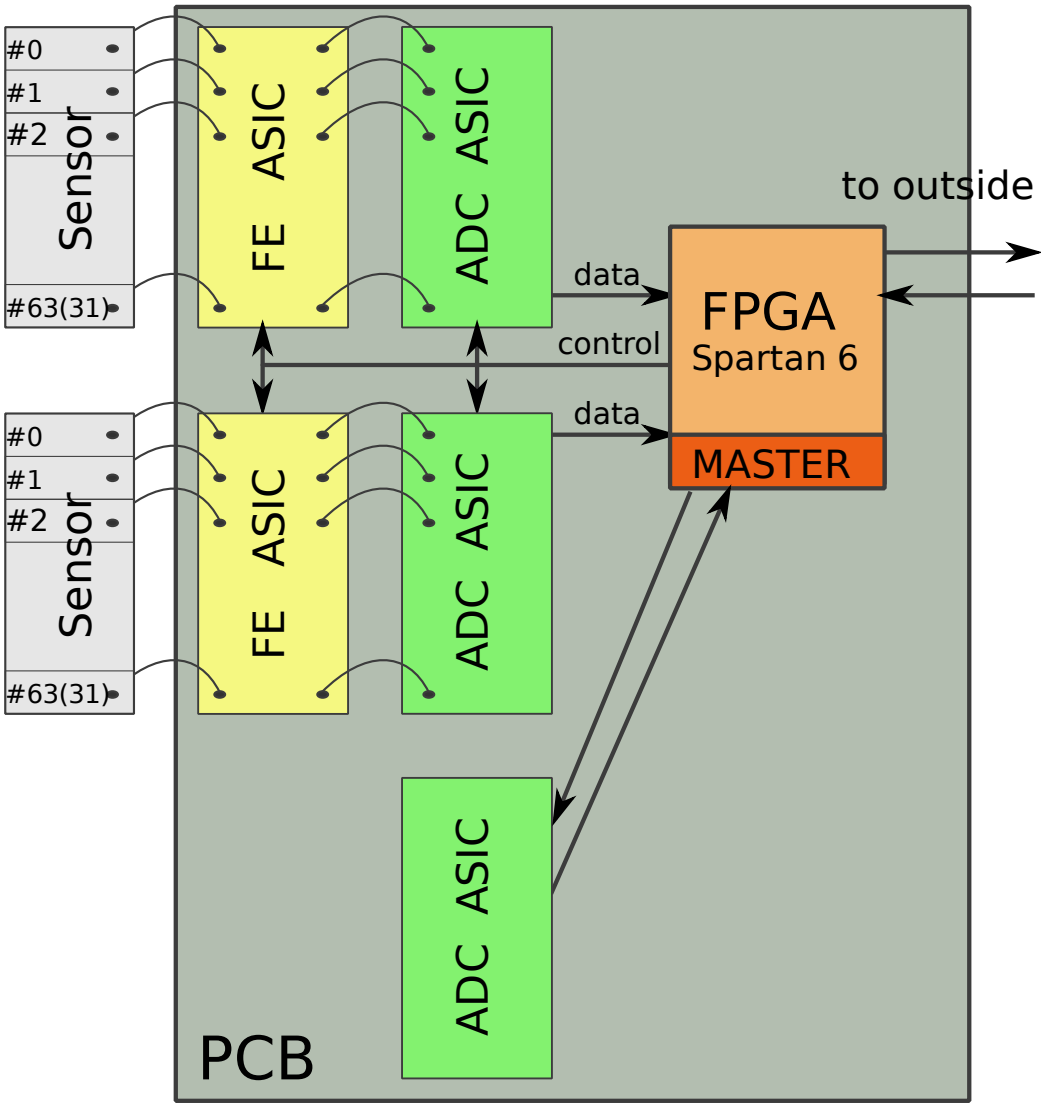


LumiCal Readout (**option 1**) (AGH & IFJ Cracow)



- one ADC for each FE channel
- one FE & ADC ASICs per 32 (or 64) channels
- 4 or 8 ADC ASICs per 1 FPGA
- one master FPGA per half-layer (or 2 for redundancy)
- FPGA serves as data concentrator and memory

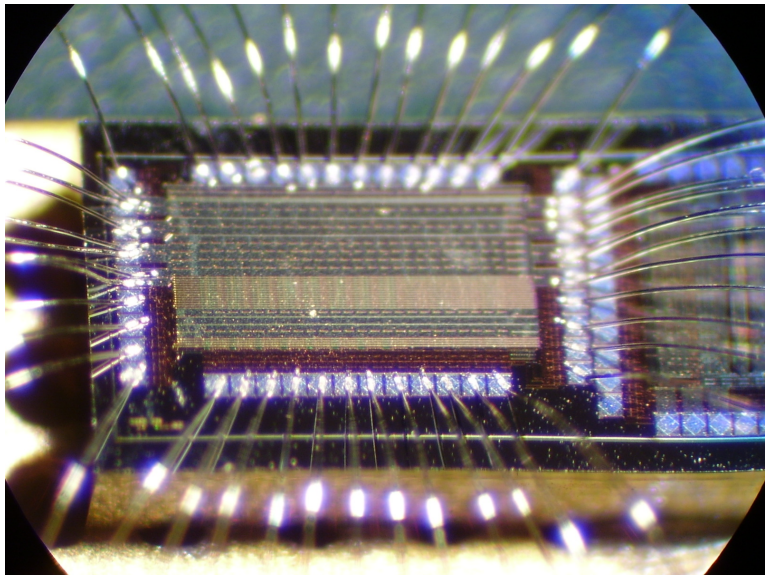
LumiCal Readout (**option 2**)



- ADC ASIC with zero suppression and small memory
- one FE & ADC ASICs per 32 (or 64) channels
- one FPGAs per half-layer (or 2 for redundancy)
- FPGA serves as data concentrator and 2nd level memory

Front-end electronics status

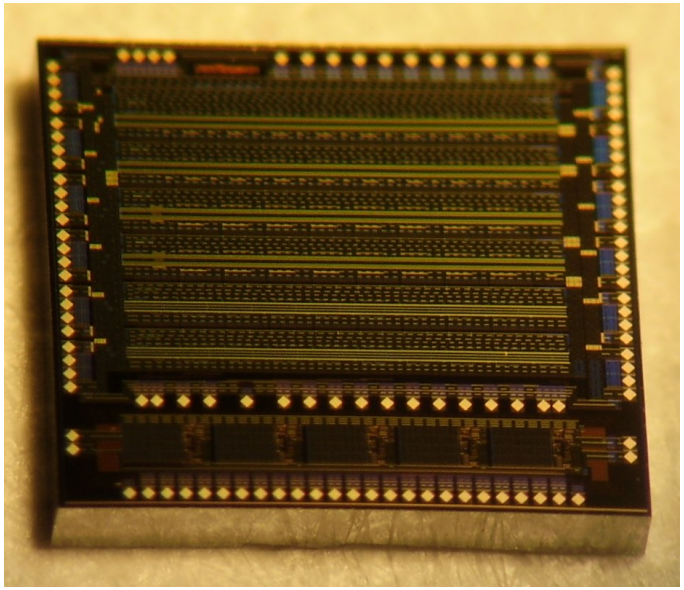
- architecture: charge amplifier with 1st order shaper
- prototypes fabricated, tested and ready for beam-test
- present technology AMS 0.35 μm
- Power: 8.9 mW/channel

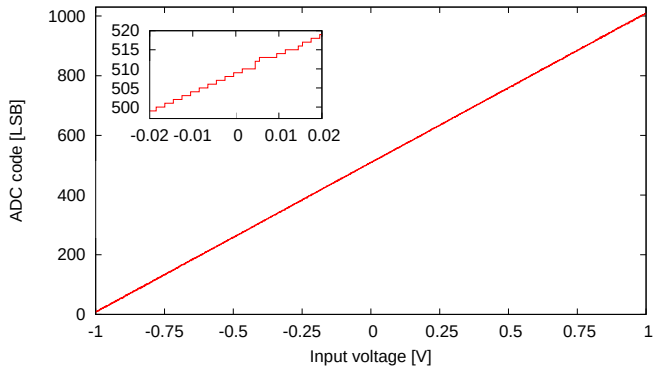


Mode	Gain [mV/fC]	Noise@50pF [fC]	Linearity [pC]	Rate [MHz]	Crosstalk [%]
Physics	0.107	0.62	10	3	$\approx$1
Calibration	$\approx$20	0.28	0.035	3	$\approx$0.1

ADC – prototypes and measurements

- architecture: 10 bit pipeline
- 1st prototype: only 8 stages
- 2nd prototype (photo): 9 stages + S/H + digital correction + clock and power switching
- No reference voltages yet - applied externally
- Both prototypes tested and fully functional
- 3rd prototype – multichannel (8) ADC with serial output will be submitted next week

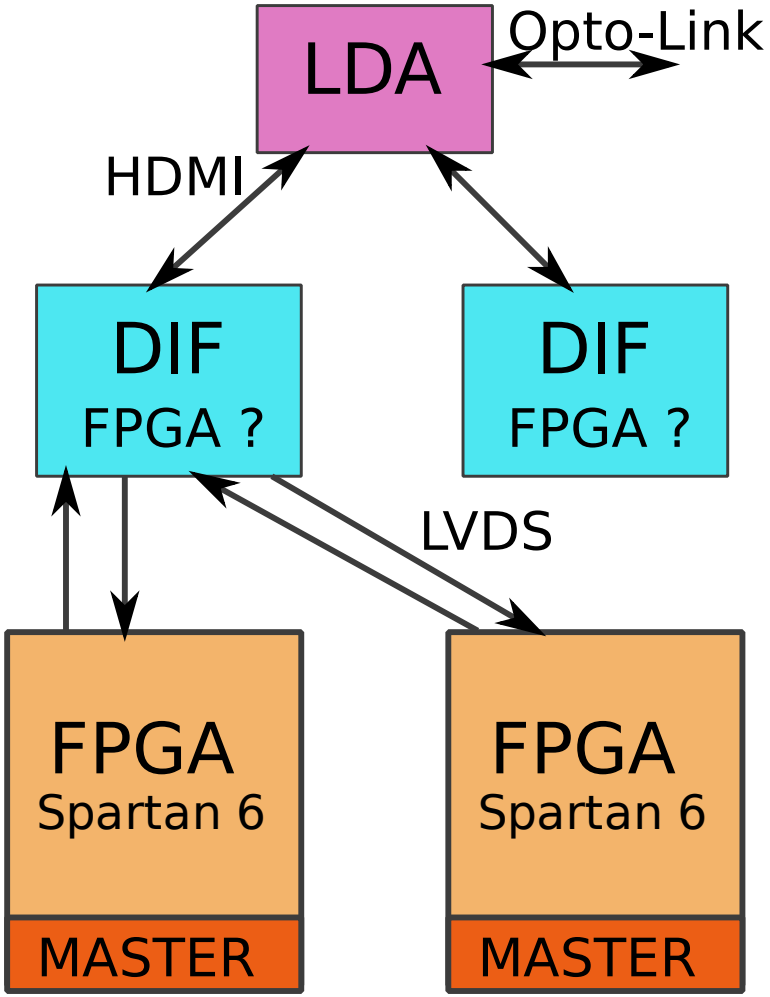




FPGA possible candidate

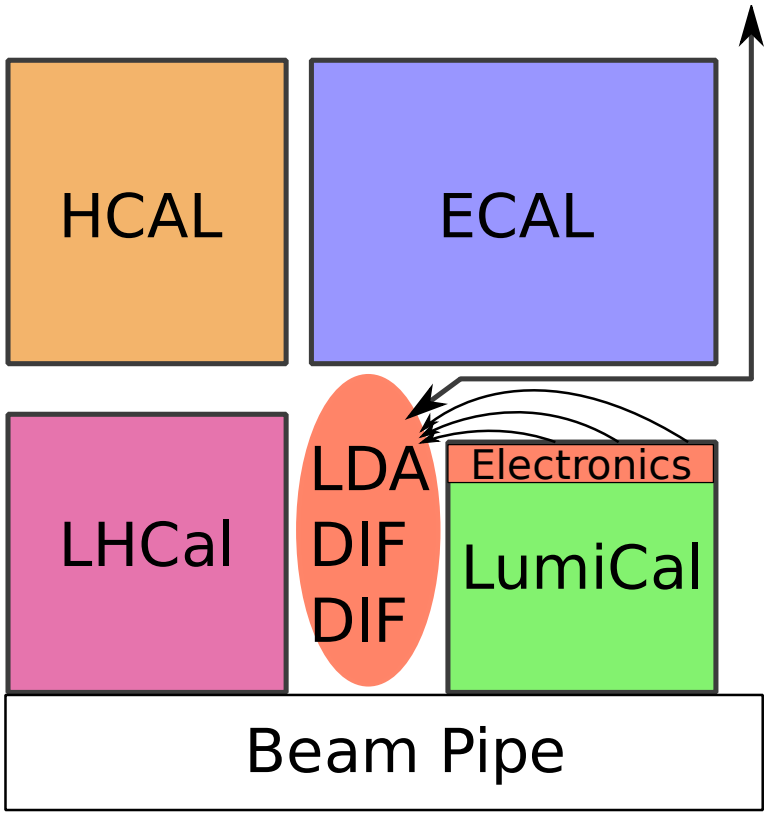
- Spartan-6 FPGA
- technology 45 nm should be partially radiation hard
- for example XC6SLX45T
  - size: 15×15 or 19×19 mm
  - memory 2MB
  - user I/O up to 296
  - 4 high speed transceivers from 614 Mbit/s to 3.125 Gbit/s

Second Level of LumiCal Readout



- data are sent out in the gap between or during the train (**to be decided**)
- master FPGAs are connected via LVDS link to DIF
- one master FPGAs for one half-layer results in 60 LVDS links (or 120 with redundancy)
- one LDA is enough in slow scenario (readout in the gap) or $\sim$5 for fast readout

Where to place the DAQ components?



- DAQ components may be placed between LumiCal and LHCal. Is there enough space?
- what about radiation resistance of DIF and LDA? Can they tolerate radiation loads in this location?

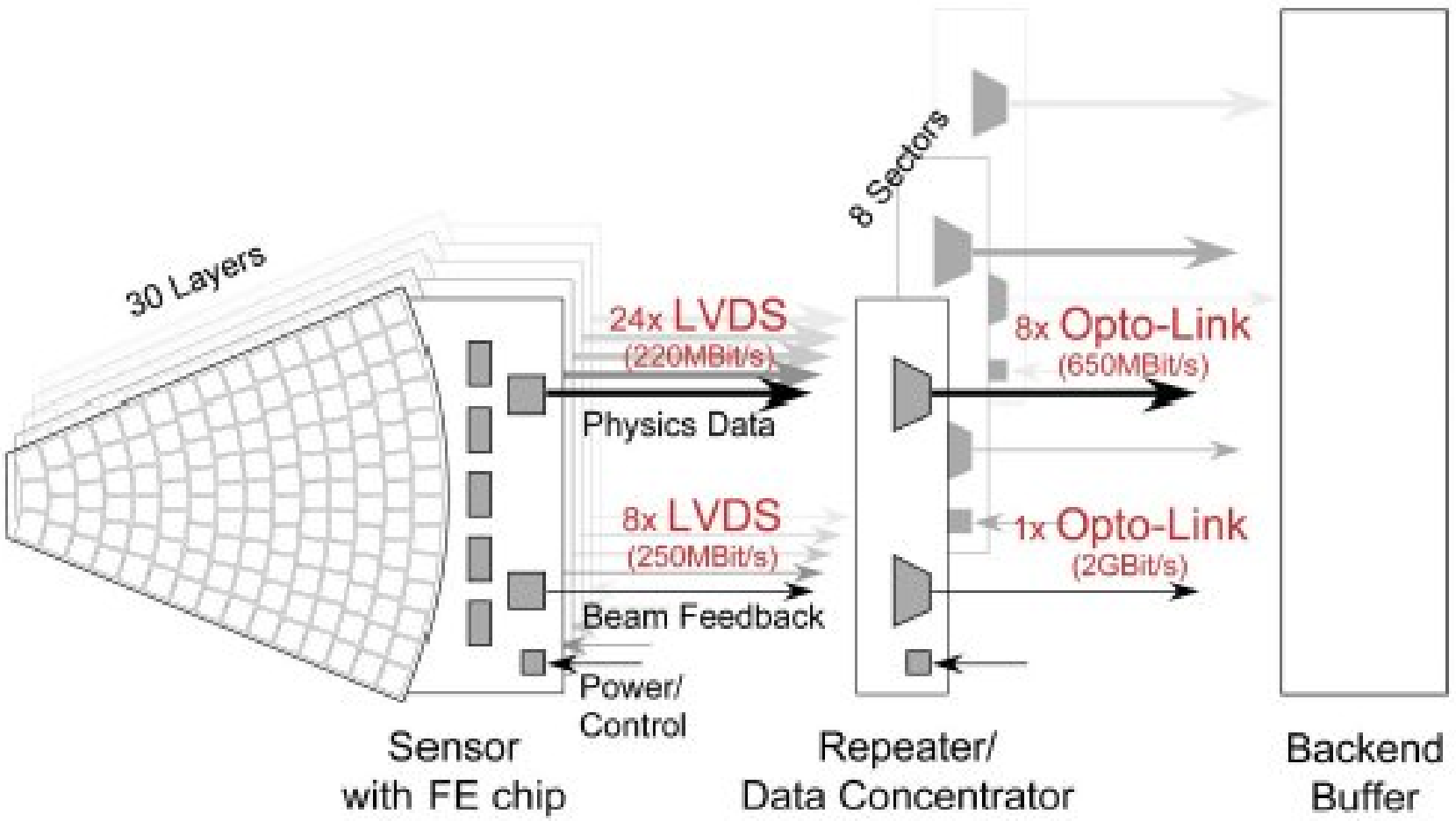
Data volume and rate

- average data volume
  - average number of hits in a single channel is around 10 per train but the standard deviation is also 10 (to be checked)
  - 10 hit/train * (10^5 channels) $\approx$ 1 M hit/train
  - 1 M * (10 ADC bits + 20 address bits) $\approx$ 4 MB/train
  - occupancy per train: 10^5 channels/1 M hit $\approx$ 1% (70% in LOI)
- data readout scenarios
  - data are sent in the gap between trains: 4 MB/200 ms = 160 Mbit/s
  - data are sent during train: 4 MB/1 ms = 16 Gbit/s

Clock

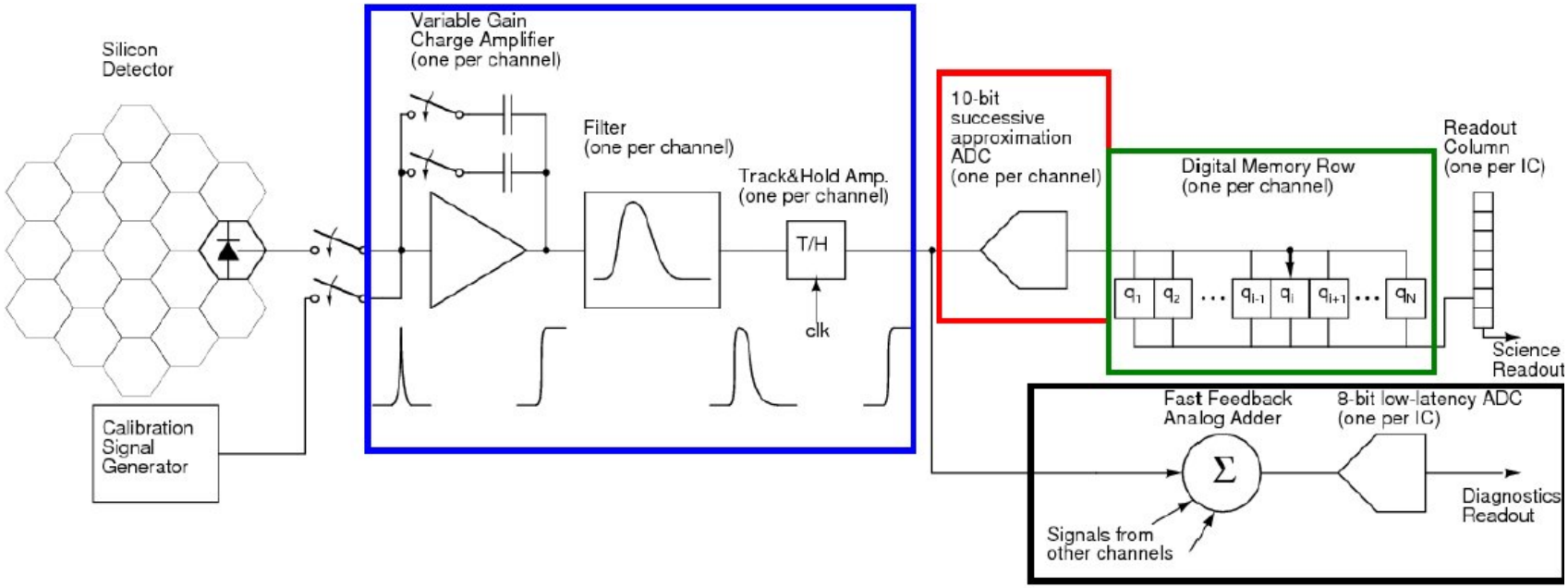
- machine clock (2.7 MHz) is needed for ADC sampling with precision (jitter) of about 1 ns
- will other (multiple) clocks be available or need to be generated locally?

BeamCal readout (DESY Zeuthen)



- similar to LumiCal concept
- no DIFs & LDAs in the moment

BeamCal readout ASIC (SLAC)



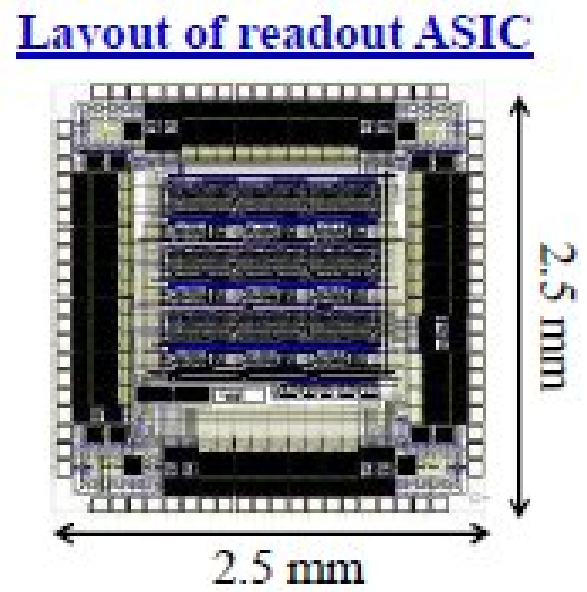
- technology TSMC 0.18 μm
- 32 channels
- memory: 2820 words (10 bits + parity) per channel
- analog addition of 32 channels for fast feedback
- design completed last year (tests in progress)

BeamCal data volume and rate

- data volume
  - 8 sectors/layer and 30 layers
  - total 38400 channels with occupancy $\sim$100%
  - 38400 * 10 bit * 2820 bx = 130 MB per train
- data readout
  - data are sent in the gap between trains: 130 MB/200 ms = 5 Gbit/s
  - so we need at least 2 LDAs (2*3Gbit/s) + 1 (redundancy)
- fast feedback – data are read out after each bx
  - 2 layers only * 1280 channels/32 * 8 bit/bx = 80 B/bx
  - the data rate is 1.6 Gbit/s

Pair Monitor (Tohoku Univ.)

- placed at the front of BeamCal
- 1st prototype was done in TSMC 0.18 μm
- 2nd prototype fabricated in FD-SOI CMOS 0.2 μm
- radiation tests are running
- 200 000 pixels * 8 bits * 16 = 3.2 MB per train
- data are sent in the gap between trains: $\sim$ 128 Mbit/s



LHCal

- necessary for hermeticity of hadronic events. It will cover the square hole in HCAL.
- Calorimeter in Si/W technology with 40 tungsten layers (10 mm thick), at $\sim$4 interaction lengths
- in comparison to BeamCal and LumiCal it gives a relatively small amount of additional data
- but in the moment no one is working on it!

Summary

- forward detectors electronics status
  - LumiCal: front-end ASIC ready, multichannel ADC will be submitted in the next week
  - BeamCal: readout chip is being tested
  - Pair Monitor: readout chip is during radiation tests
- data volumes and rates are known
  - in LumiCal: 4 MB/train and 160 Mbit/s or 16 Gbit/s
  - in BeamCal: 130 MB/train and 5 Gbit/s
  - BeamCal fast feedback: 80 B/bx and 1.6 Gbit/s
  - in Pair Monitor: 3.2 MB/train and 128 Mbit/s
- data readout and DAQ are in the conception phase
- common DAQ scheme with DIFs and LDAs can be use
- important questions concerning available space and radiation tolerance of DIF & LDA
- how to build DIF?