SDHCAL Power pulsing tests status in lyon

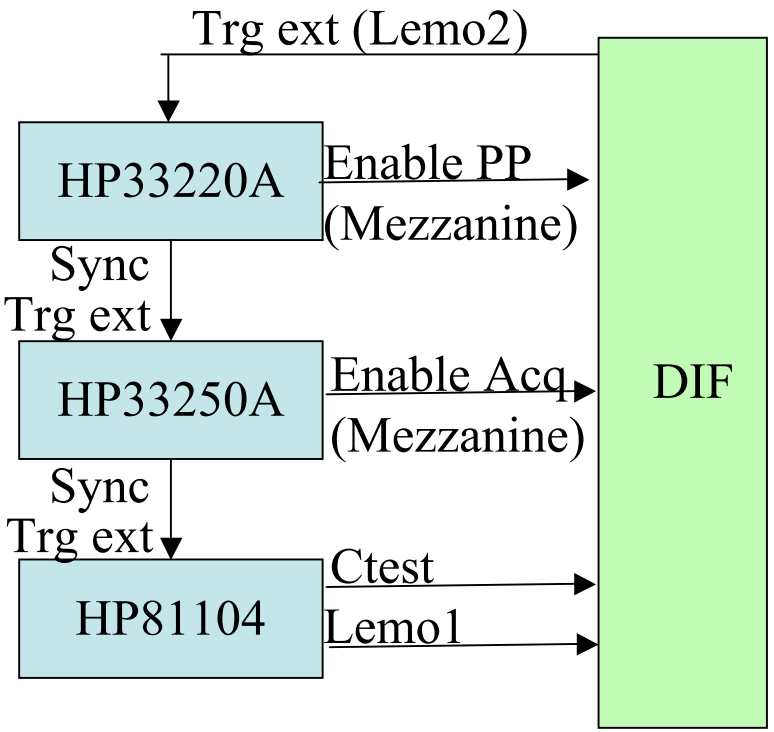
C. Combaret, for the IPNL team

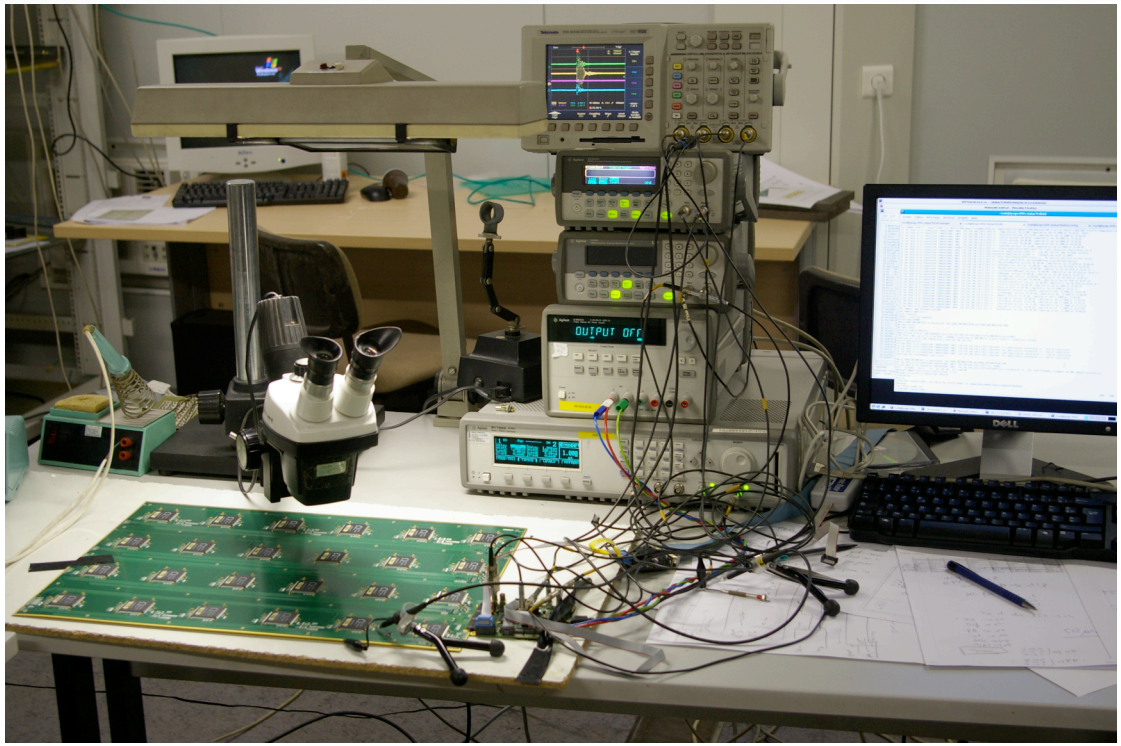
Power pulsing on Hardroc 2 ASU : method

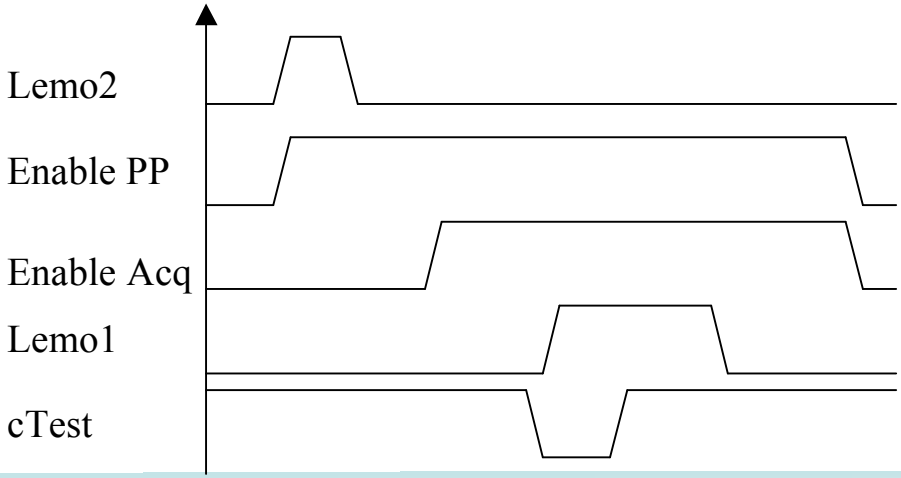
As discussed with HR2 designers :

1. Record (reference) Scurves and Bias levels with no capacitor removed
2. Enable PP hardware on DIF (use of Mezzanine pin 1)
3. Enable PP in DIF firmware : PowerOn_x = register OR Mezzanine_1
4. Try PP with no capacitor removed
5. Record analog bias signal
6. Remove Capacitors on biases of 1 HR2 step by step and check
7. Record analog bias signal
8. Record Scurves
9. Remove Capacitors on biases of all asics and check again
10. Record analog bias signal
11. Record Scurves

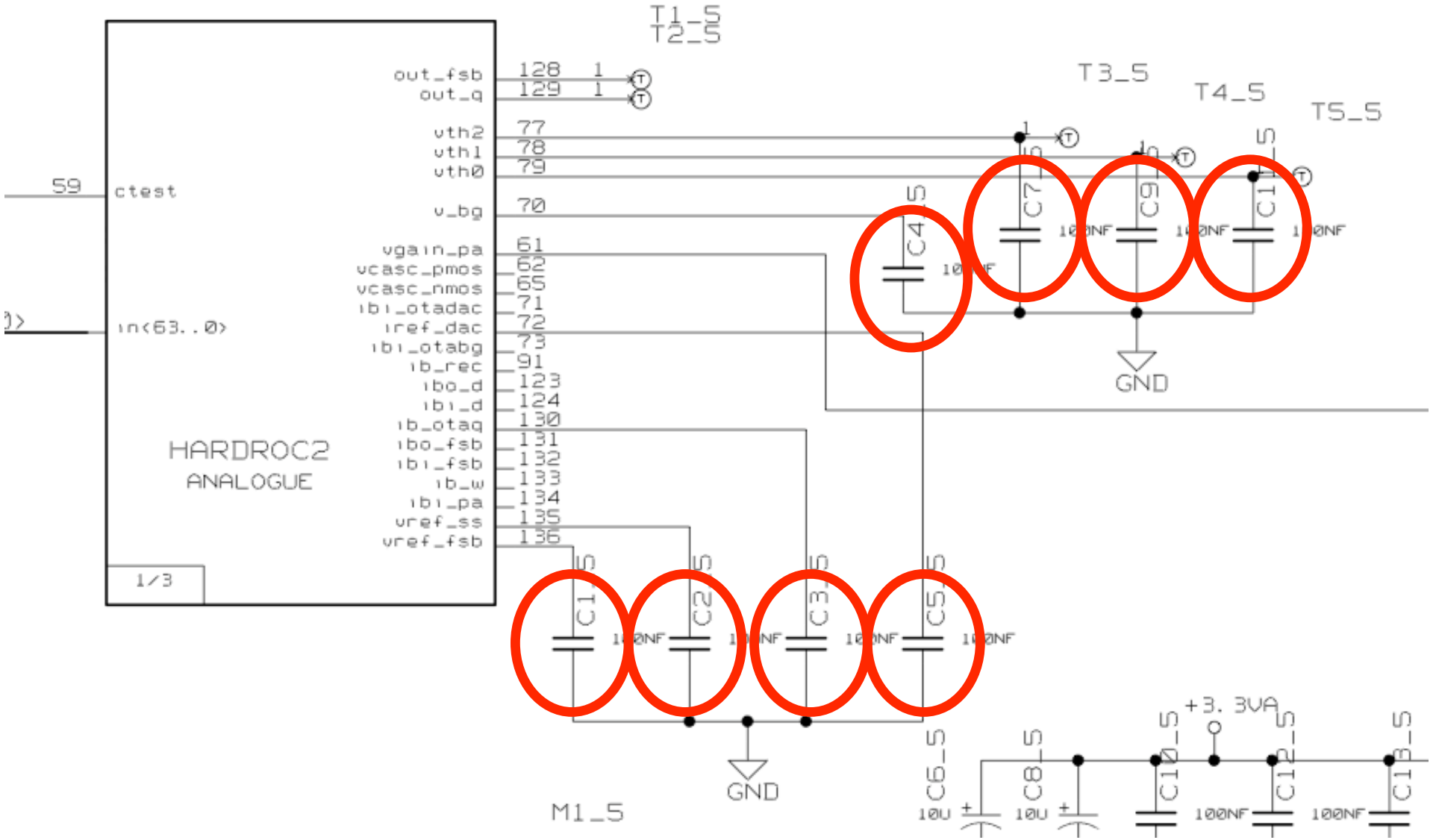
Hardware setup



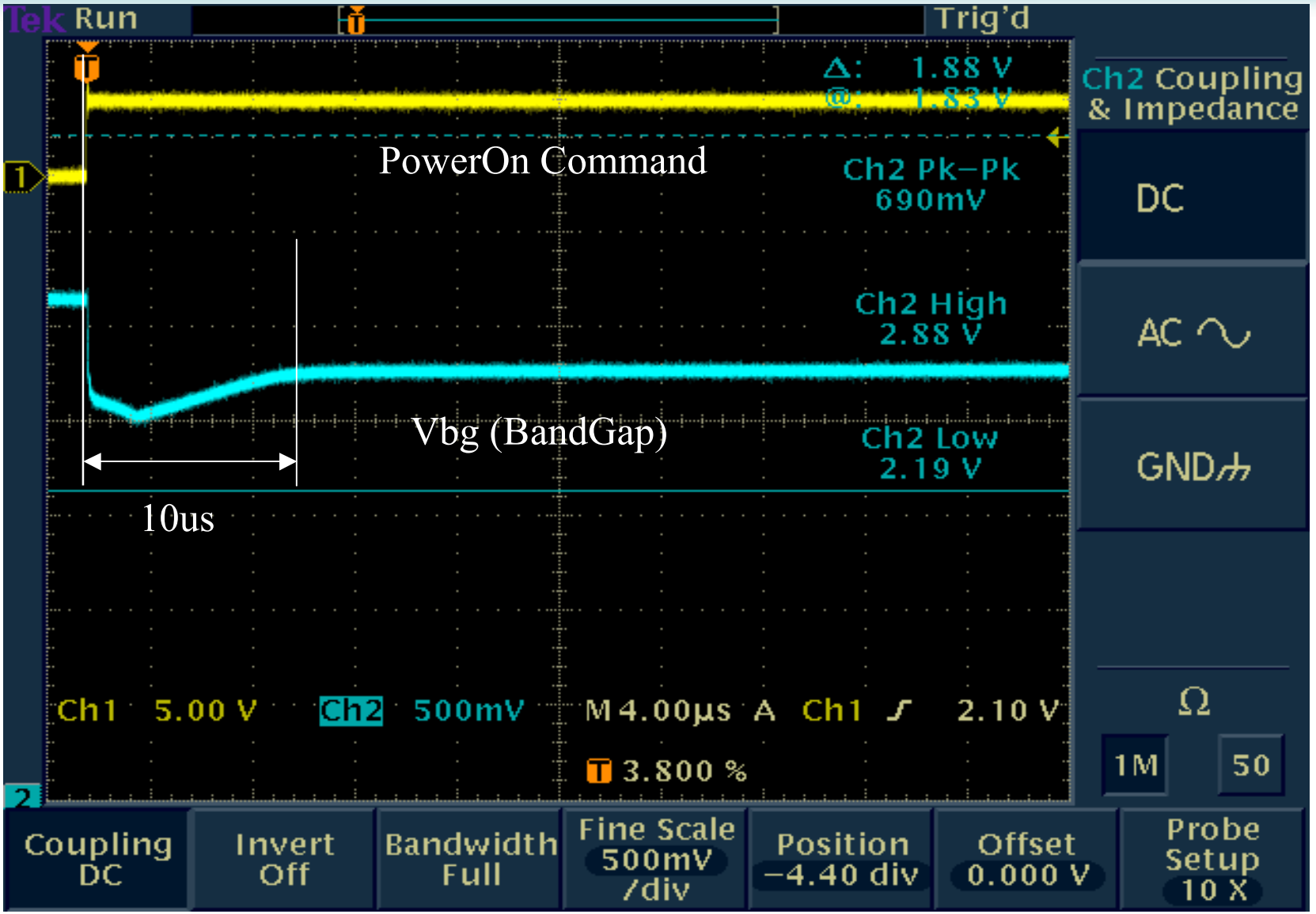




Power pulsing on Hardroc 2 ASU : method

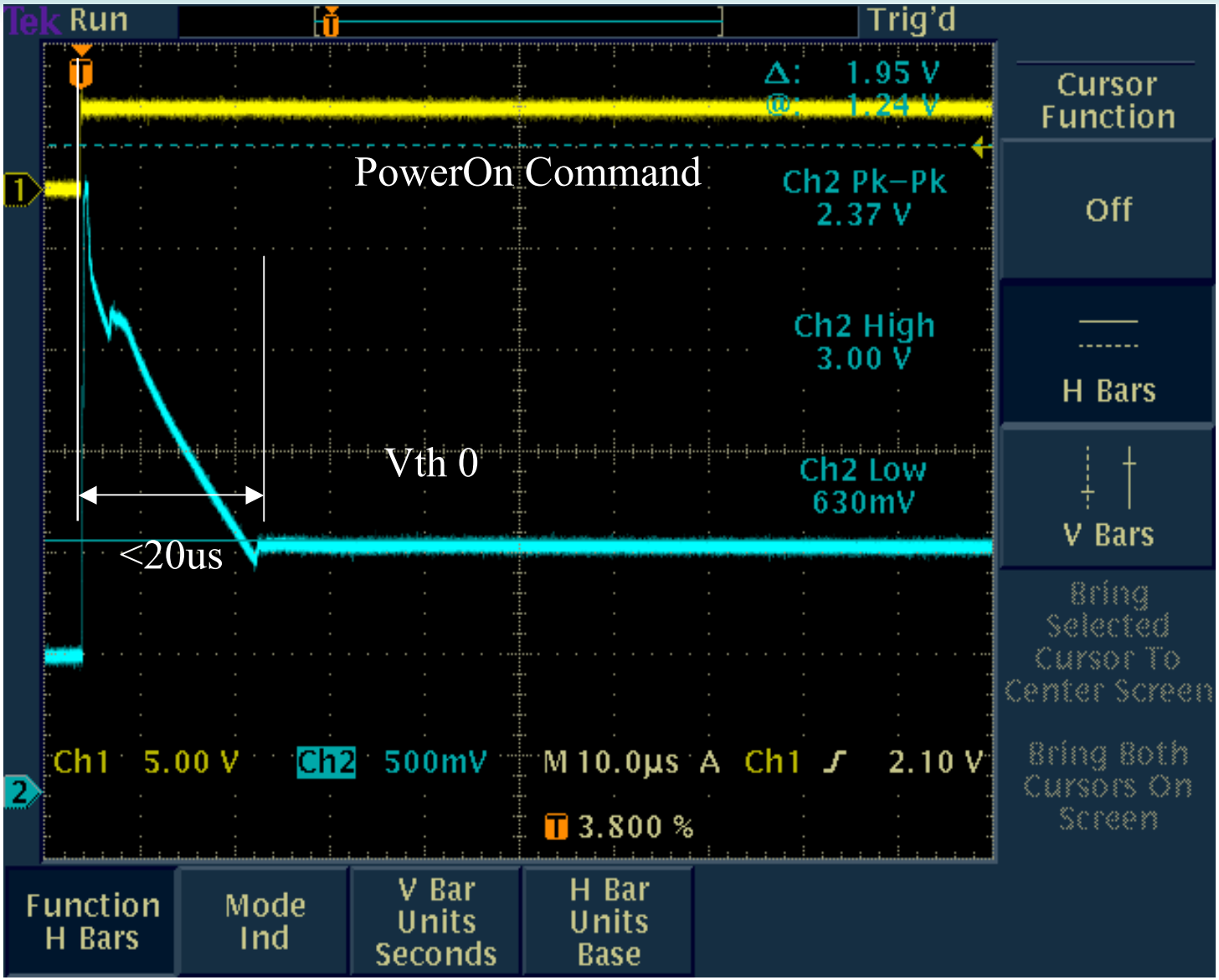


Power pulsing on Hardroc 2 ASU : preliminary results



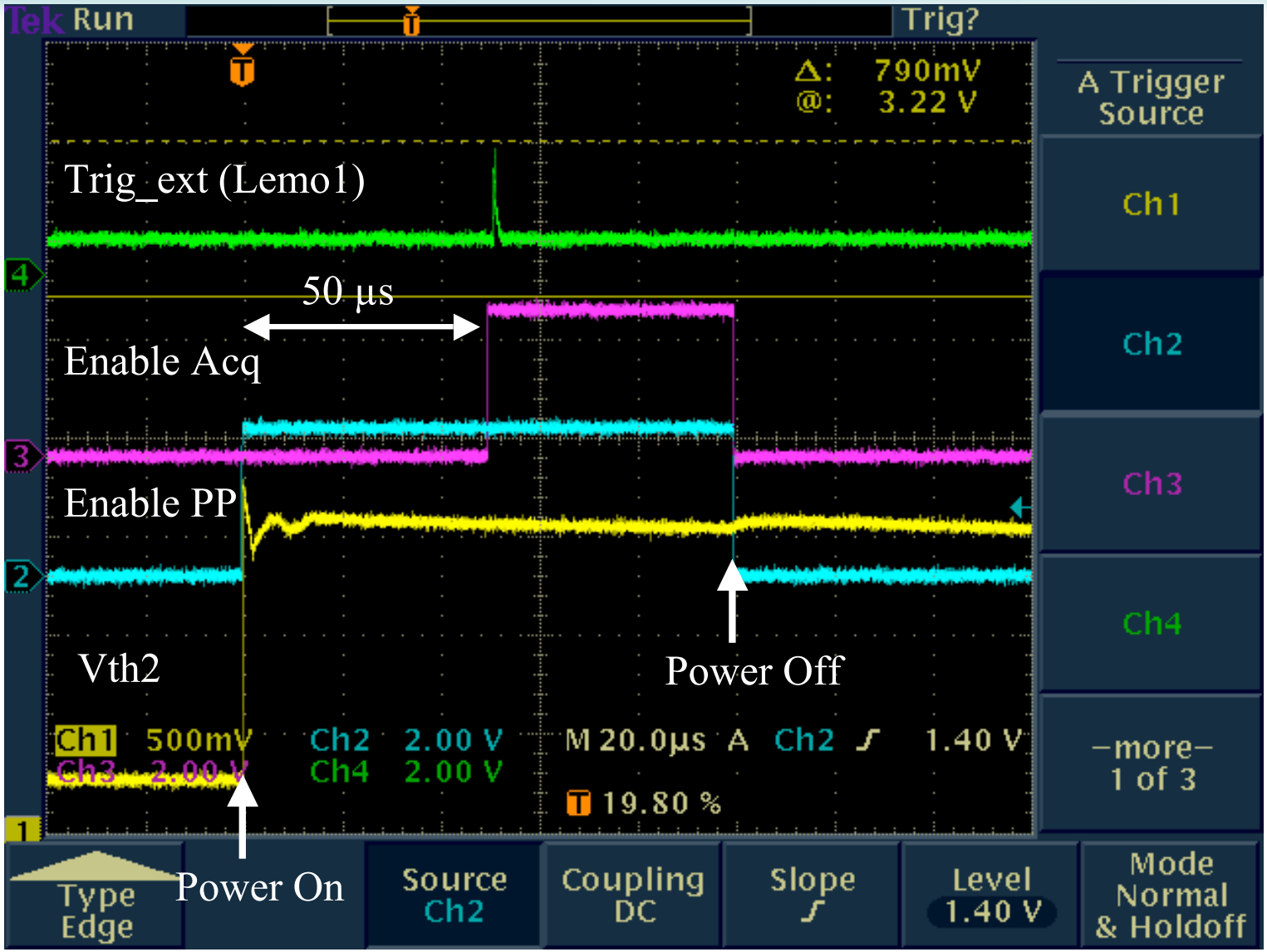
Capacitors removed on one asic (first of the ASU)

Power pulsing on Hardroc 2 ASU : preliminary results



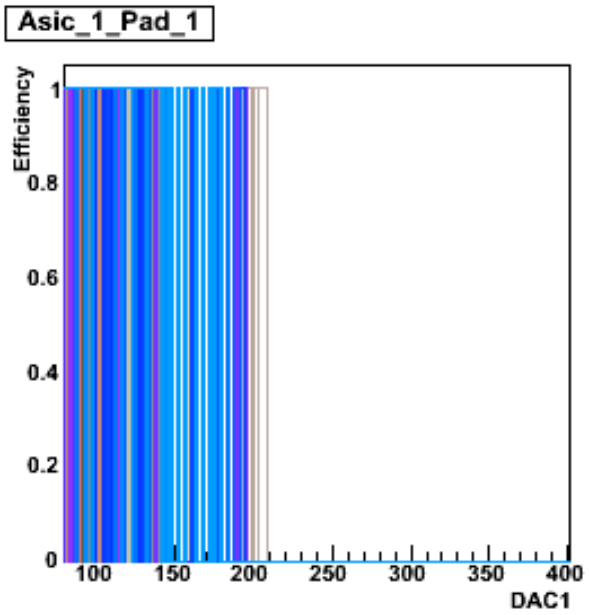
Capacitors removed on one asic (first of the ASU)

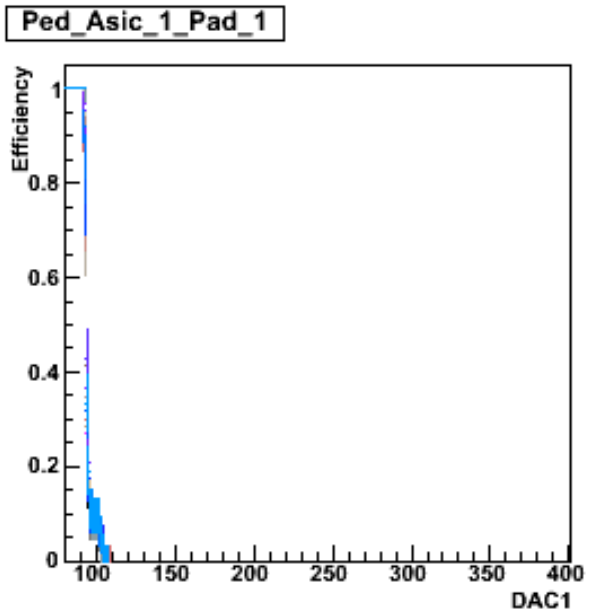
Power pulsing on Hardroc 2 ASU : preliminary results

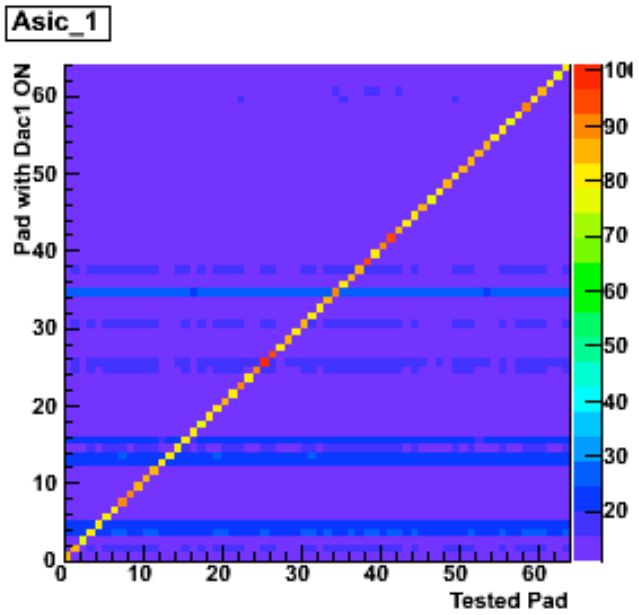


Capacitors removed on all asics

Power pulsing on Hardroc 2 ASU : preliminary results





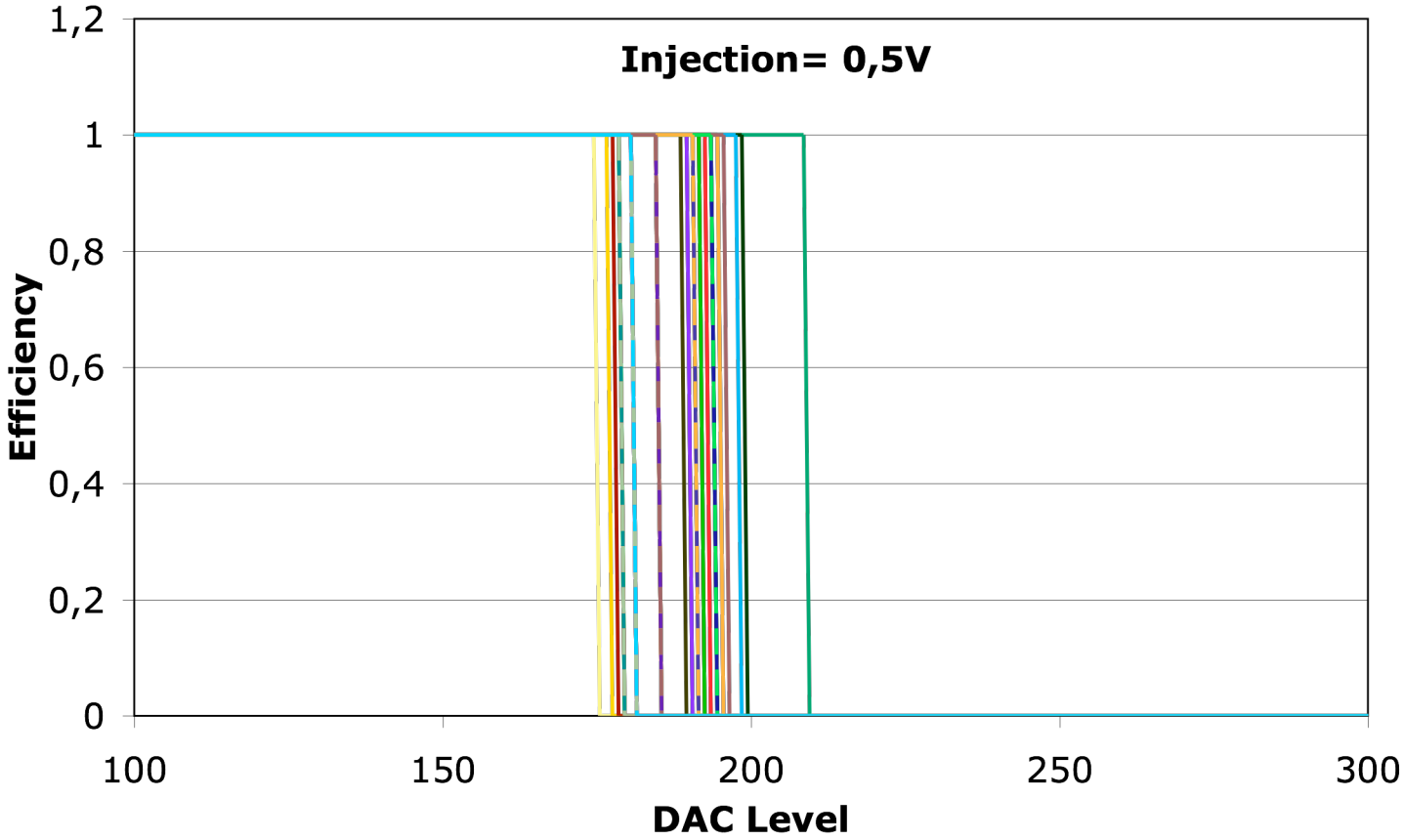


DAC1Min = 80
DAC1Max =400
DAC1Step=1
GainMin = 128
GainMax = 128
GainStep=1
Injection=0.5V

Pedestal looks roughly OK
Injected channel seems rougly OK
BUT strange behaviour for injected pads.

→ Because of slow control bug in HR2, some (many) SLC configurations can not be used

Power pulsing on Hardroc 2 ASU : preliminary results

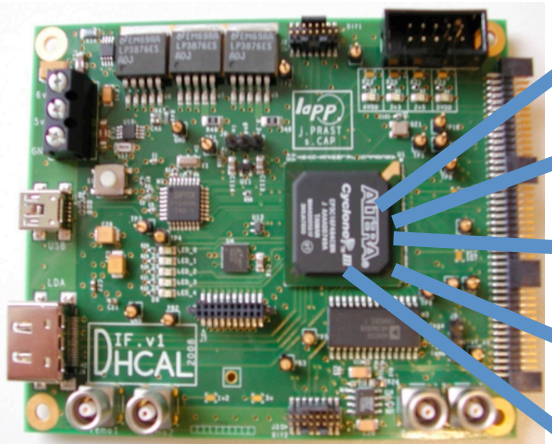


Asic 1
DAC1Min = 80
DAC1Max =400
DAC1Step=1
GainMin = 128
GainMax = 128
GainStep=1
Injection=0.5V

After correction, data seem more correct…

But this Scurve is very preliminary, comparisons must be made with results obtained before power pulsing.

DIF (For J. Prast, LAPP)



VHDL firmware1 for Hardroc1 Micromegas

VHDL firmware2 for Hardroc1 RPC

VHDL firmware3 for Dirac2 Micromegas

VHDL firmware4 for Hardroc2 Micromegas

VHDL firmware5 for Calice DAQ Test

DHCAL DIF Production (For J. Prast, LAPP)

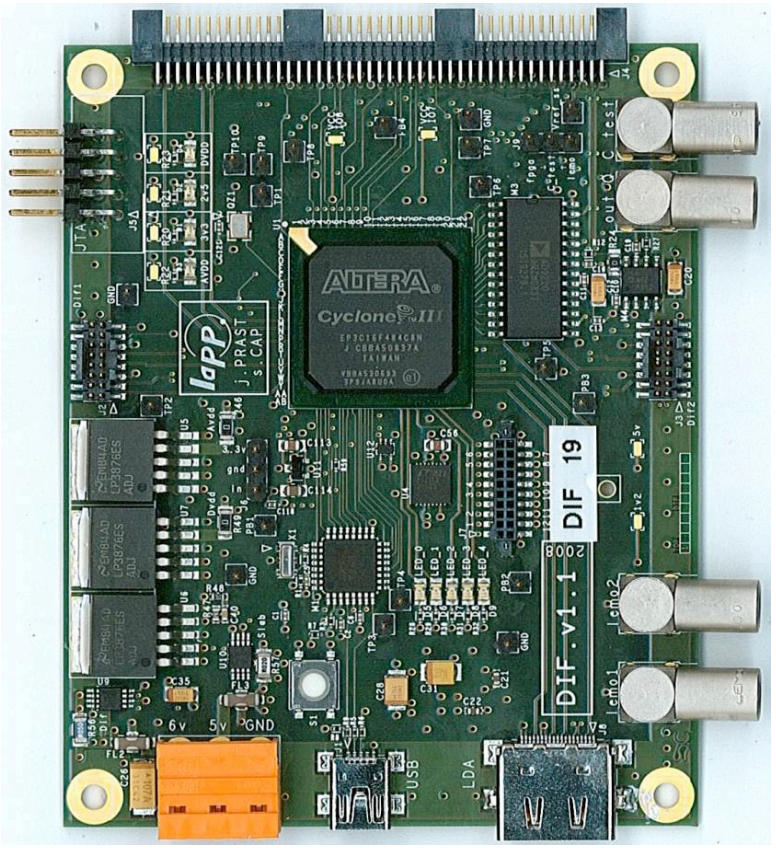
120 DIF have to be produced for the m^3 (+ spares ie 140 ?).

The DIF will be produced as they are currently.

- The board works quite well.
- We do not have time to make a new prototype (schedule + manpower).

Boards will be produced and tested for beginning of fall 2010.

- Some boards can be available before if required (> end of spring)



Thank you for your attention