TPC DAQ: status and plans

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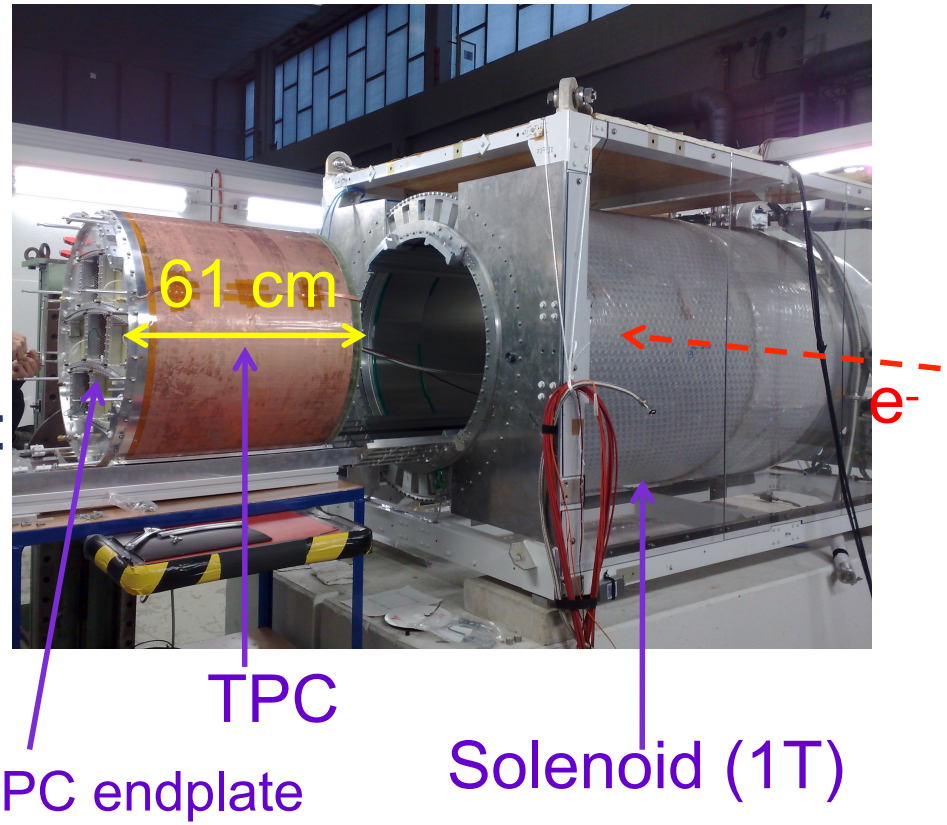
On behalf of the LCTPC Collaboration

Overview

- Current status
- AFTER DAQ
- ALTRO DAQ
- Future developments

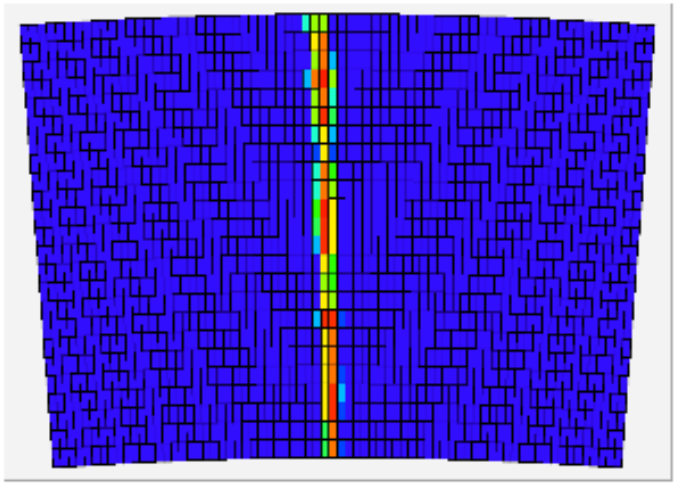
Current status

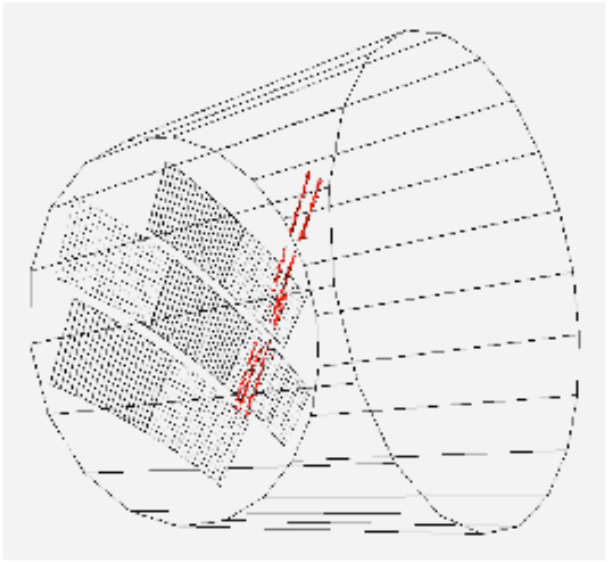
- Since end of 2008, LCTPC collaboration is testing a large TPC prototype (LPTPC) with 6 GeV e^- beam in DESY
- TPC endplate allows to easily accommodate different Micro Pattern Gas Detector (MPGD)
- 3 MPGD technologies are tested:
  - **MICROMEGAS + PADs**
  - **Double GEM + PADs**
  - **Triple GEM + CMOS Timepix chip**
- 3 ReadOut Electronics are tested:
  - **MICROMEGAS + T2K AFTER**
  - **Double GEM + ALTRO (ALICE)**
  - **Triple GEM + CMOS Timepix chip**



Current status II

- Since end of 2008, 12 weeks of test beam in DESY with LPTPC
  - **Both GEMs and MICROMEGAS are running nicely**
  - **As well as their DAQ**

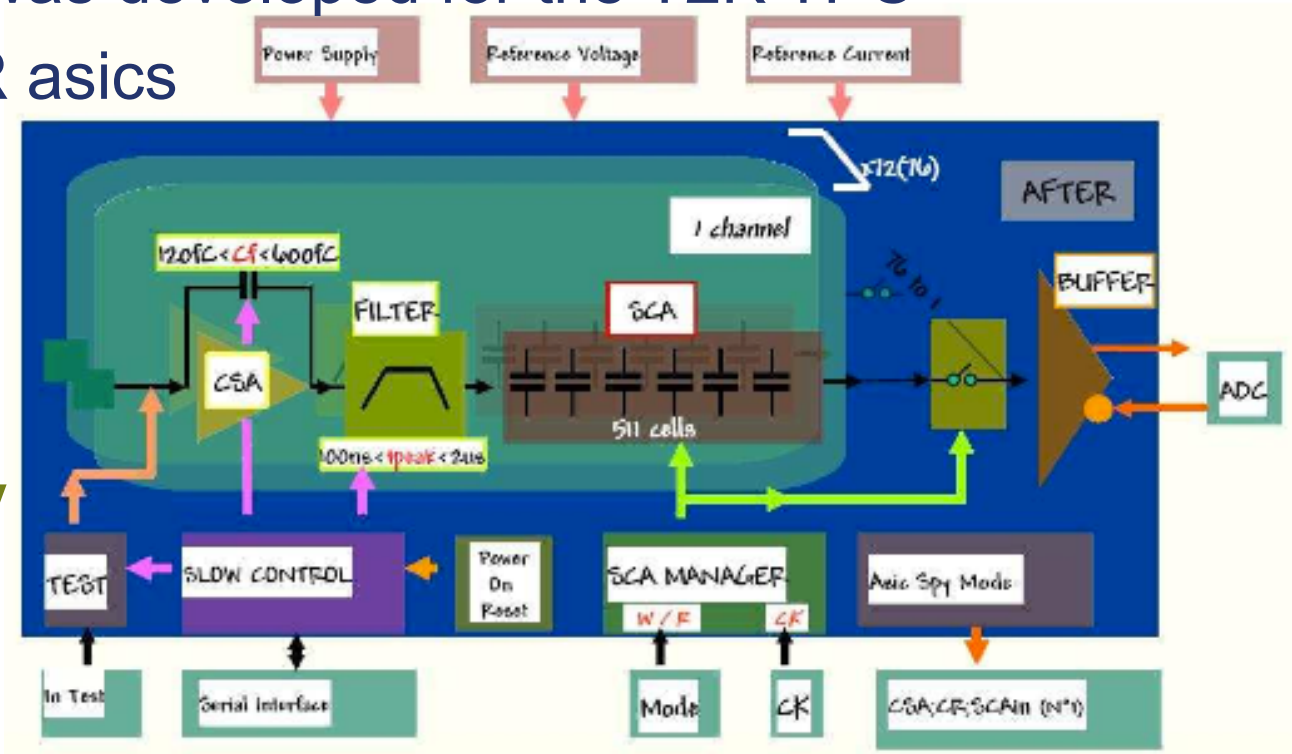




- However
  - **Different DAQ systems for the different detectors**
  - **In ILD, space will be limited for TPC electronics (10 cm)**
    - => need redesign of FE readout and DAQ interface

DAQ for MICROMEGAS+AFTER

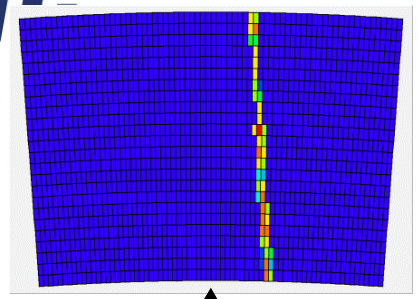
- AFTER electronics was developed for the T2K TPC
- 1 FEC has 4 AFTER asics
- 1 AFTER has 72 ch:
  - **4 gains**
  - **16 peaking times from 100 ns to 2 µs**
  - **511 analog memory cells/channel**



- 6 FECs are driven by a Front-End Mezzanine (FEM) card
- FEM is linked to Data Concentrator Card (DCC) via a duplex optical fiber
- DCC sends data to DAQ PC through Ethernet channel

DATA FLOW

DAQ:
- Maximum rate: 14 Hz (Zero Suppression mode)
- Triggered by beam (no TLU)
- Easy to use (GUI)



T2K electronics
1728 channels

Optical
fibre

Back-end
electronic
(ML405)

TCP/IP via ethenet

PC
T2K DAQ
on Linux

1-hour automatic
rsync backup

500 Go — ILC_DATA_01

500 Go — ILC_BCKP_01

500 Go — ILC_DATA_02

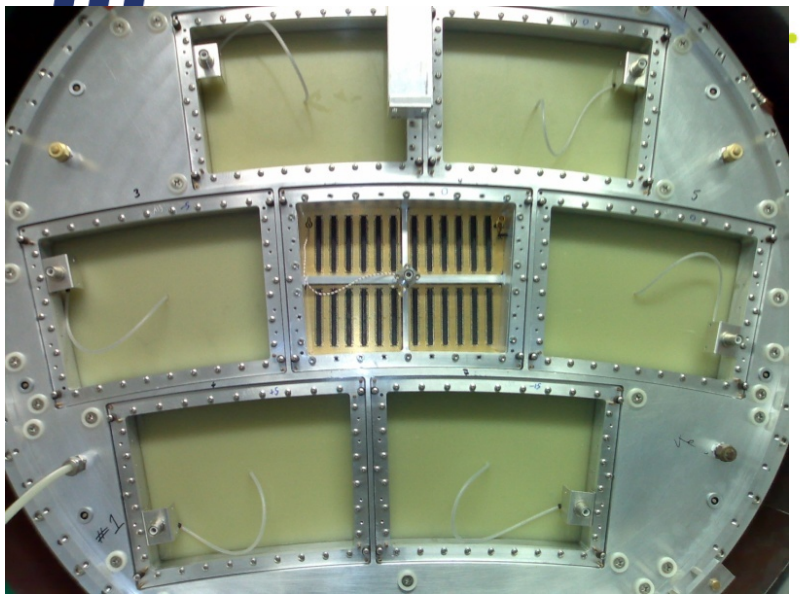
500 Go — ILC_BCKP_02

1 To — Saclay

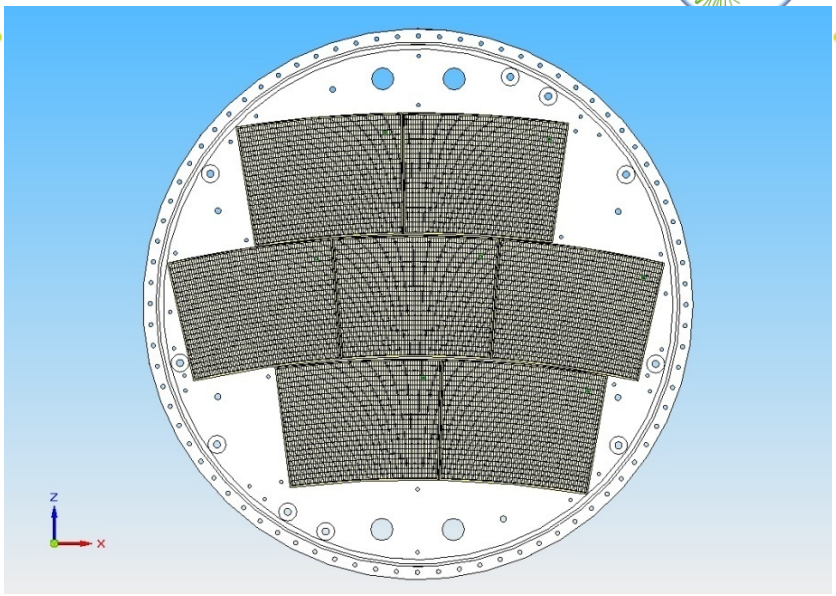
Grid

NativeToLCIO (Yun-Ha Shin)
Transfert done by K. Dehmelt

Future Plan

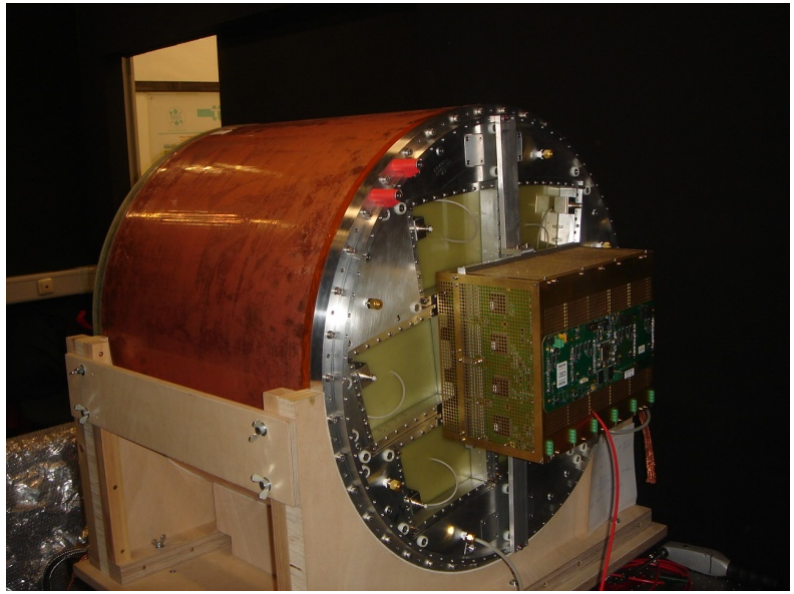


Resistive technology choice

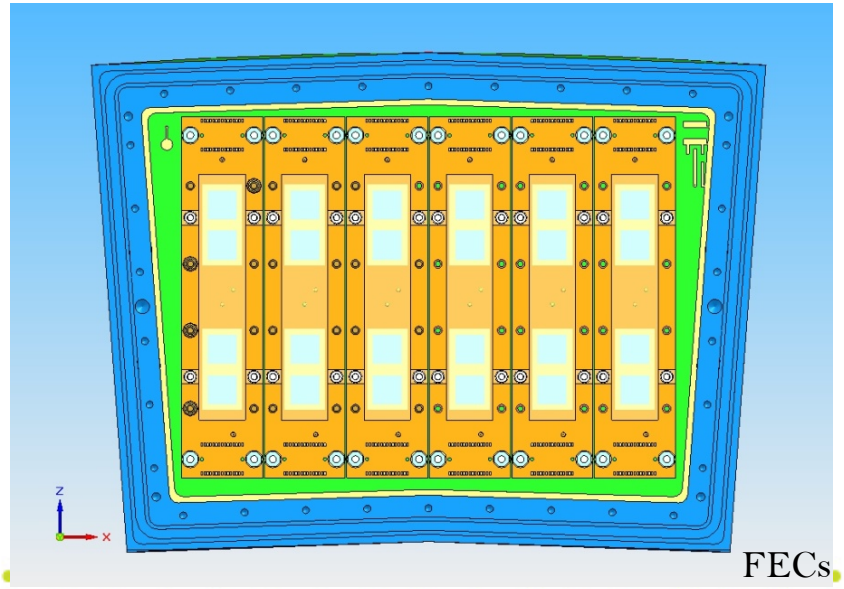


In 2008/2009 with one detector module (1728ch)

In 2010 with 7 detector modules.



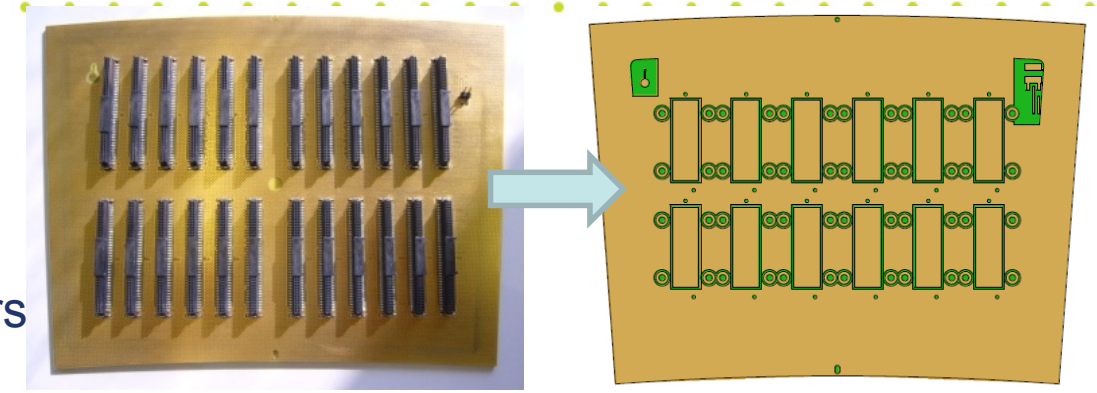
Reduce the electronics

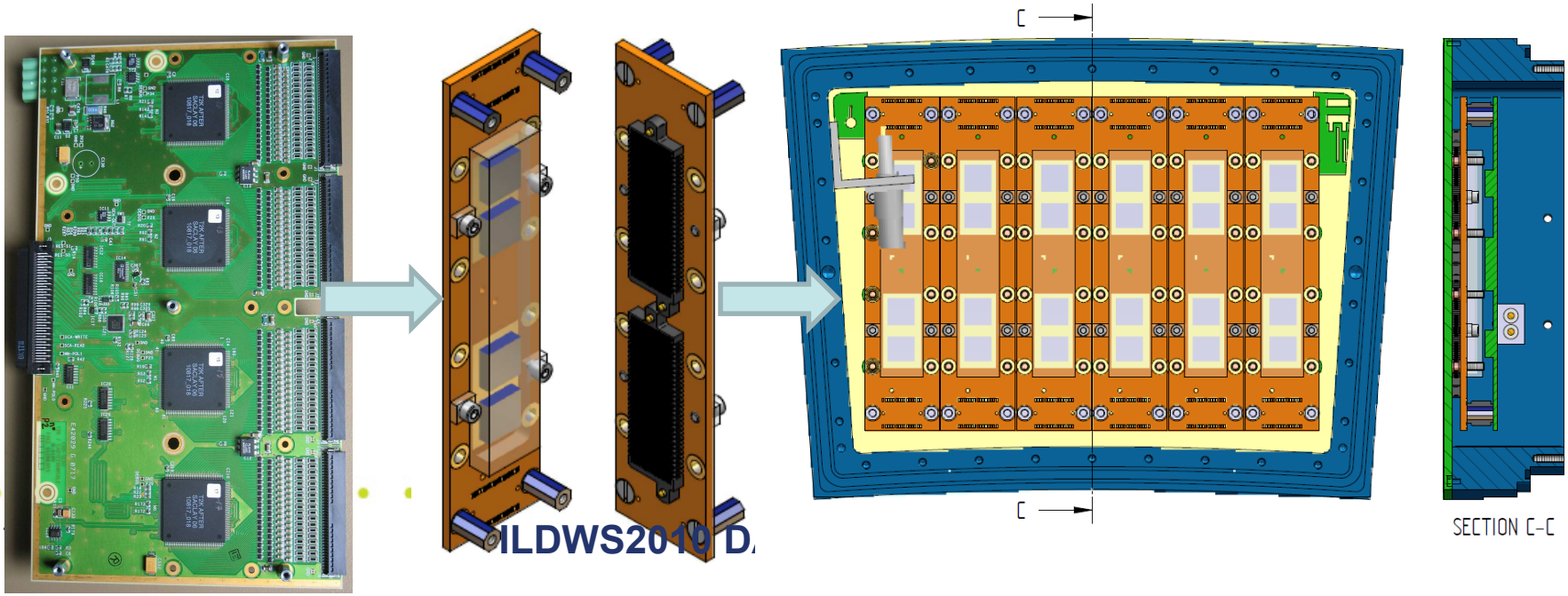


FECs

Future plans

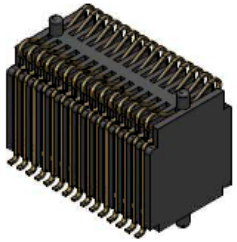
- This requires:
  - **New PCB routing**
    - keep pad layout
    - Use flat 300 point connectors
  - **New FEC**
    - Remove part of the protection (Resistive foil protects)
    - Remove packaging (silicon is 7x7mm instead of 20x20 for the packaging
    - transfer power regulation and ADC to the mezzanine module card.

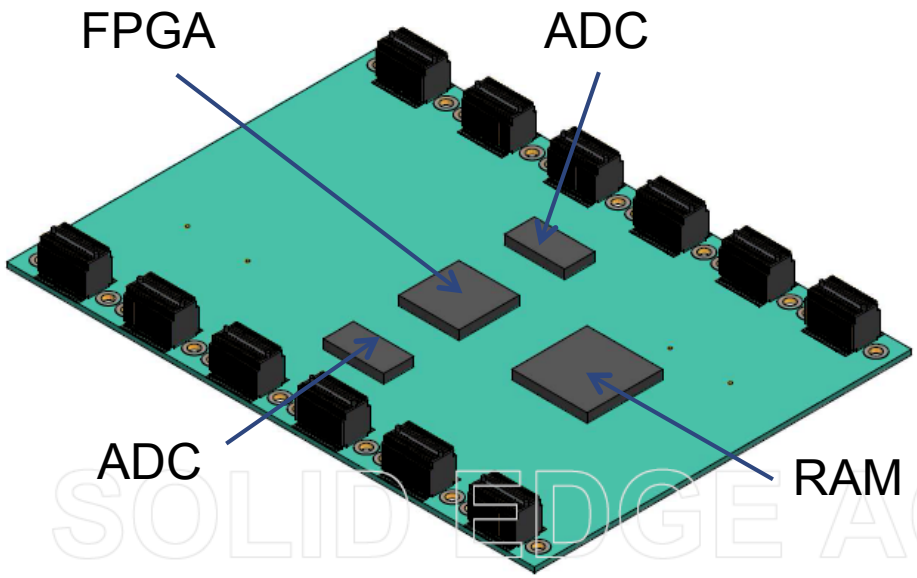




Future plans

- => requires new FEM and Back-end Module:
  - **FEM:**



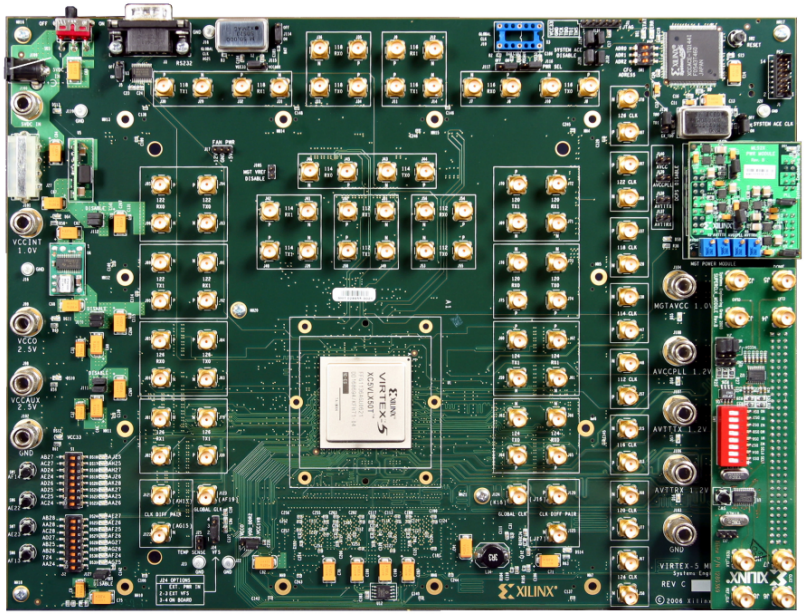


  - **Back-end:**
    - ML523 development kit from Xilinx

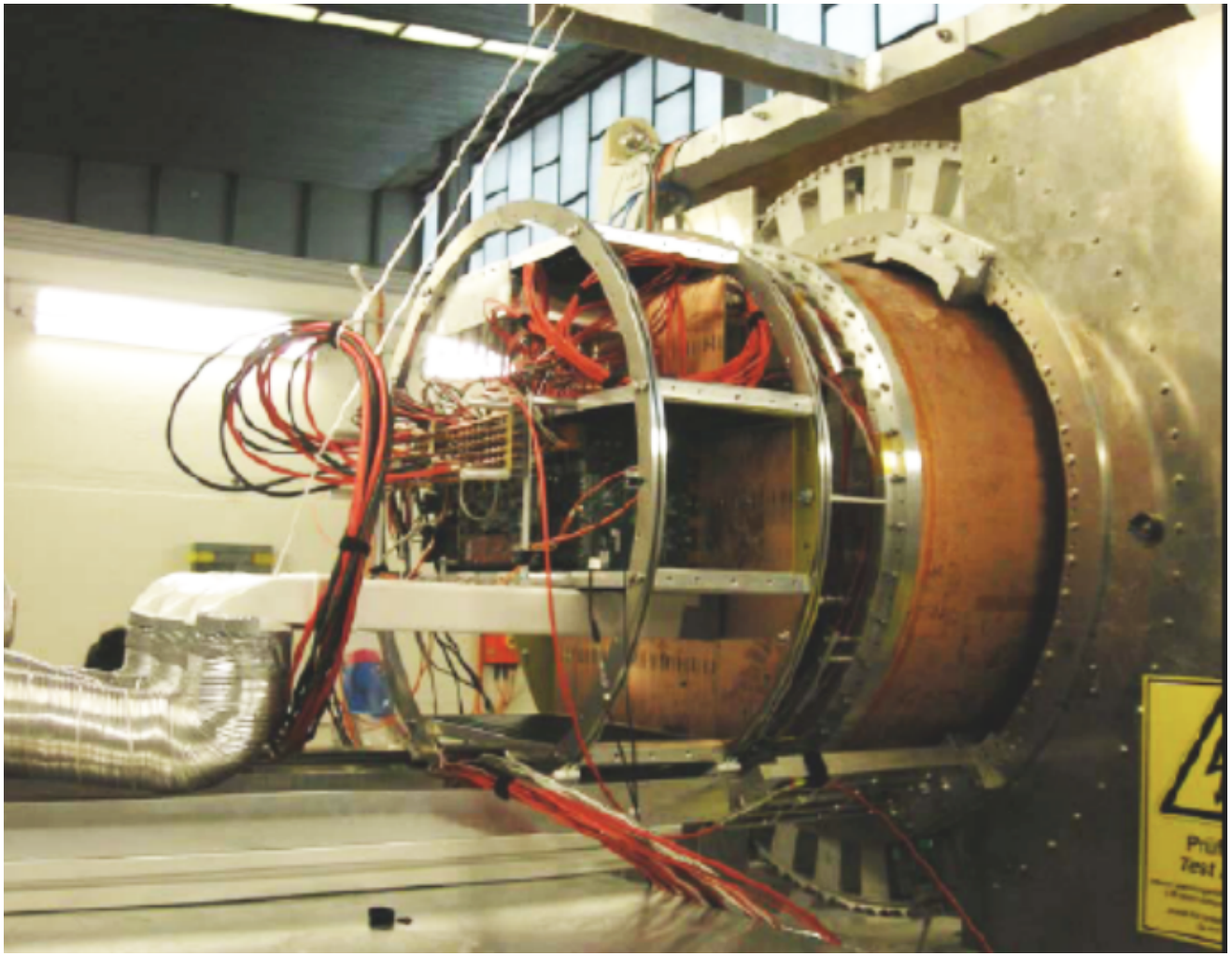
→ **vc5vfx100t FPGA from Virtex-5 device family**

- Embedded PowerPC
- 16 Multi Gigabit Transceivers
- Embedded Ethernet MAC

→ **128 Mbyte DDR2 memory**

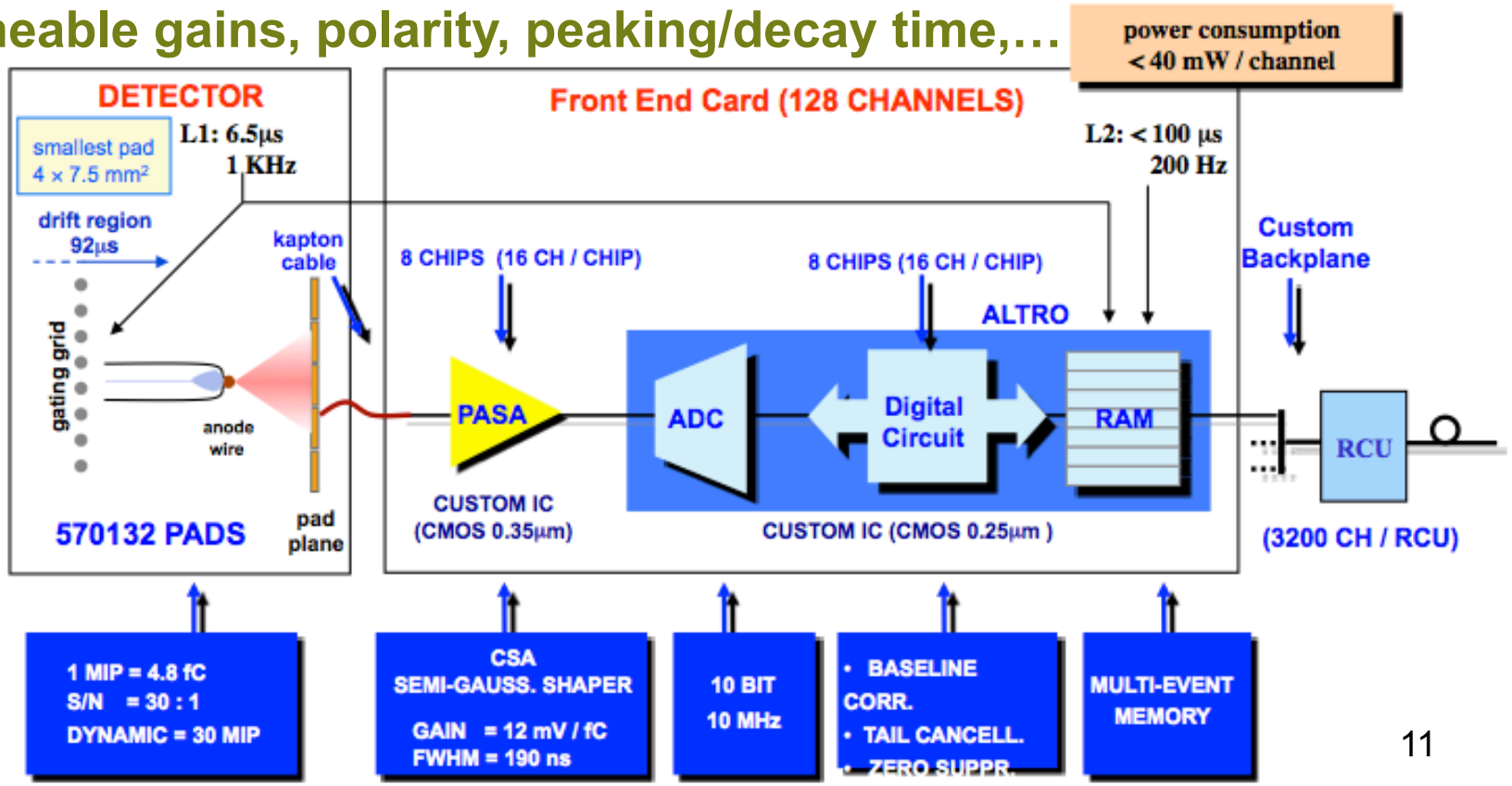


LPTPC equipped with Double GEM + ALTRO

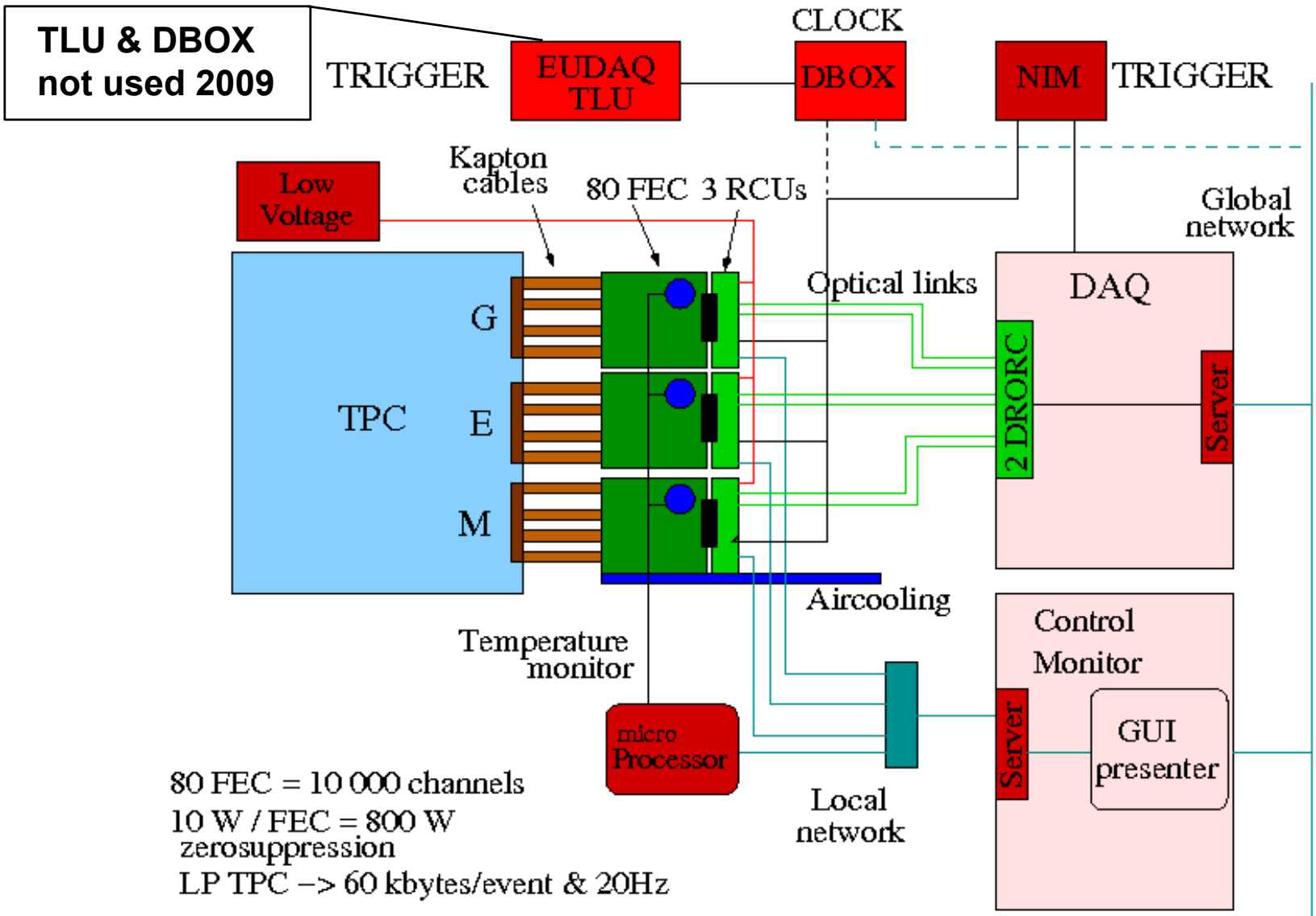


ALTRO RO

- ALTRO chip (ALICE TPC Read Out) has 16 channels
  - **Digitize and buffer the signal**
  - **Perform zero-suppression**
- 1 FEC has 8 ALTRO chips
- For LCTPC, CERN designed a new preamp: PCA16
  - **Tuneable gains, polarity, peaking/decay time,…**

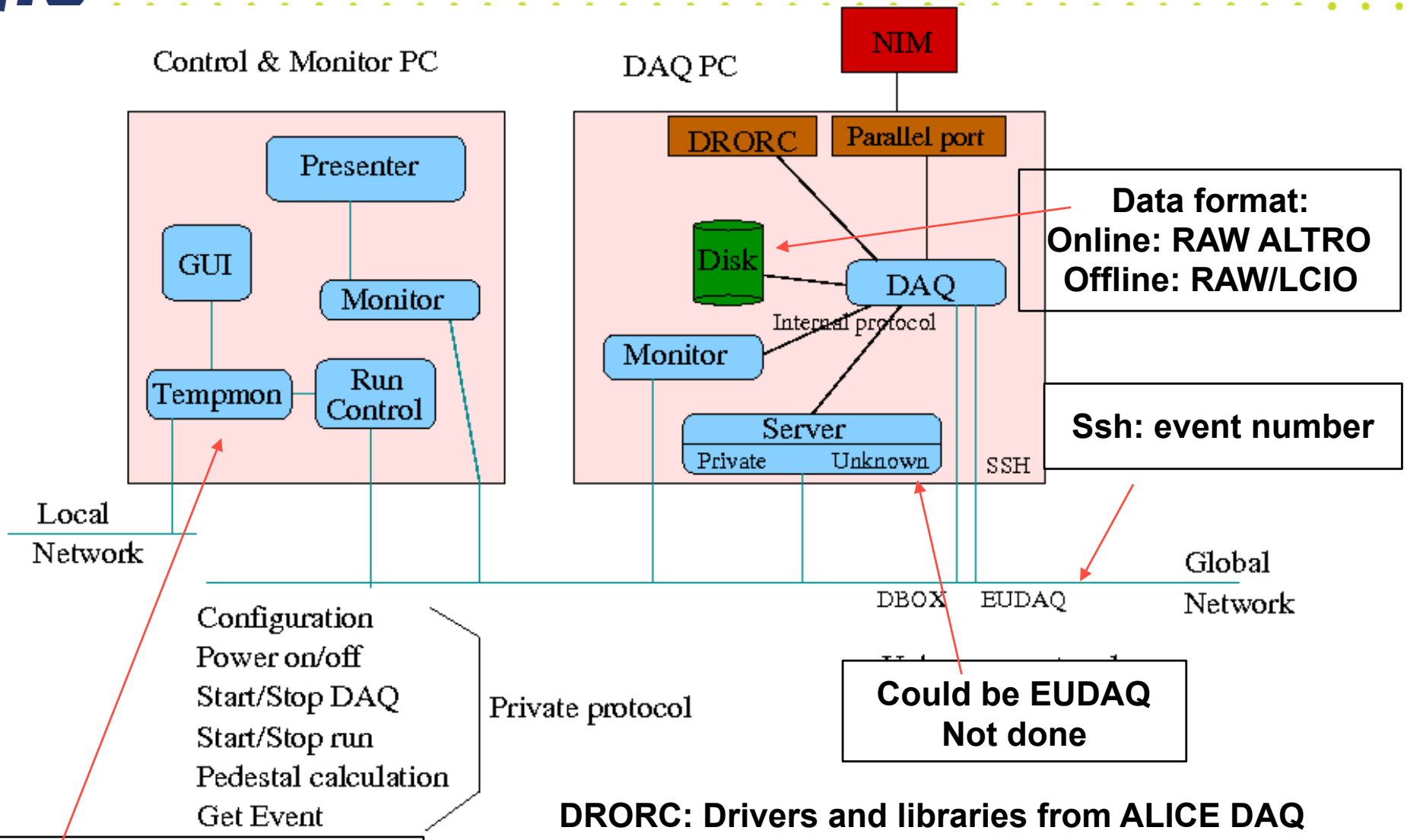


DAQ for GEM + ALTRO



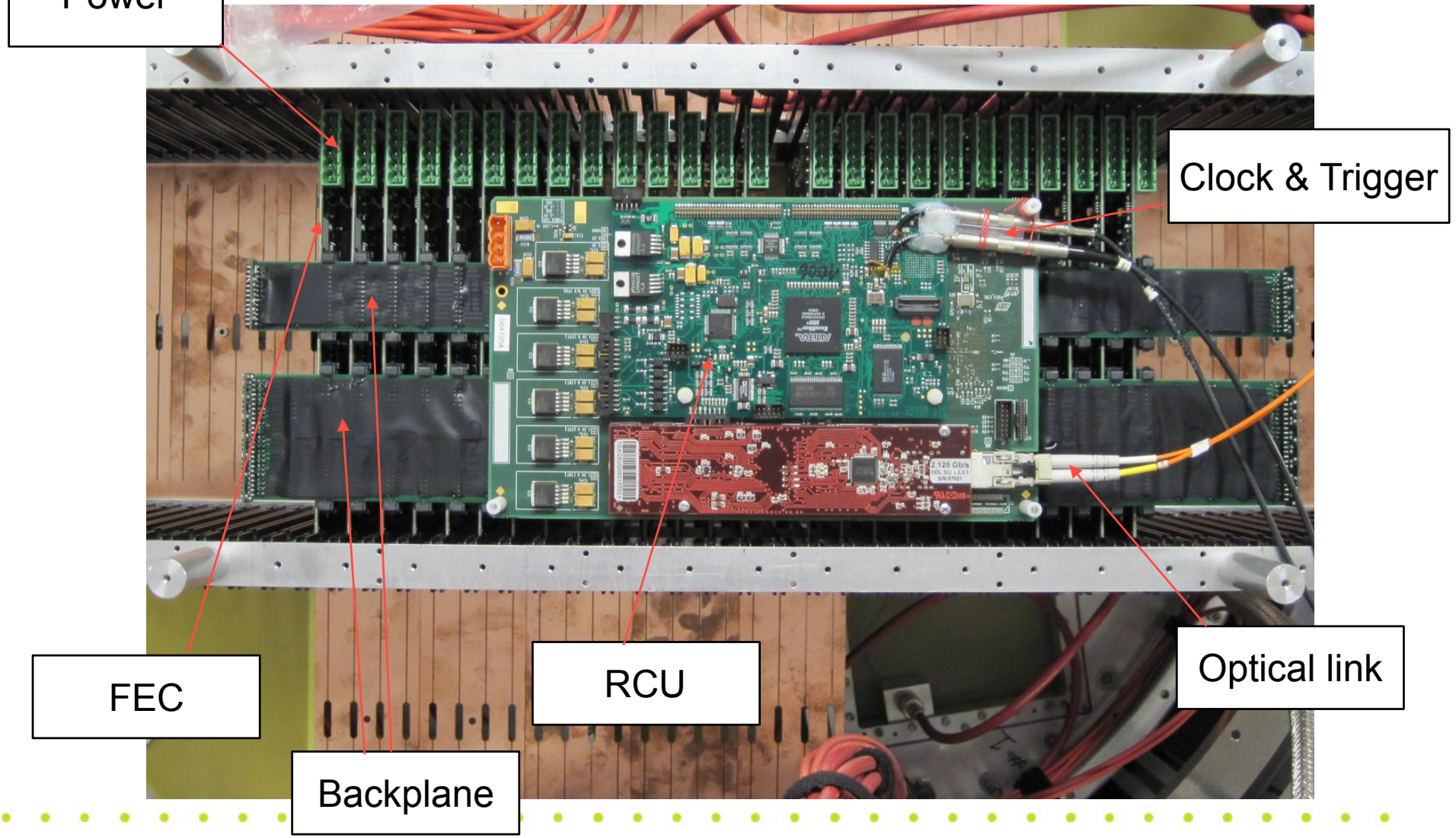
FEC = Front End Card (modified, programmable amplifier)
RCU= Readout Control Unit (modified trigger/clock inputs
DRORC = Data ReadOut Receiver Card

ALTRO standalone software



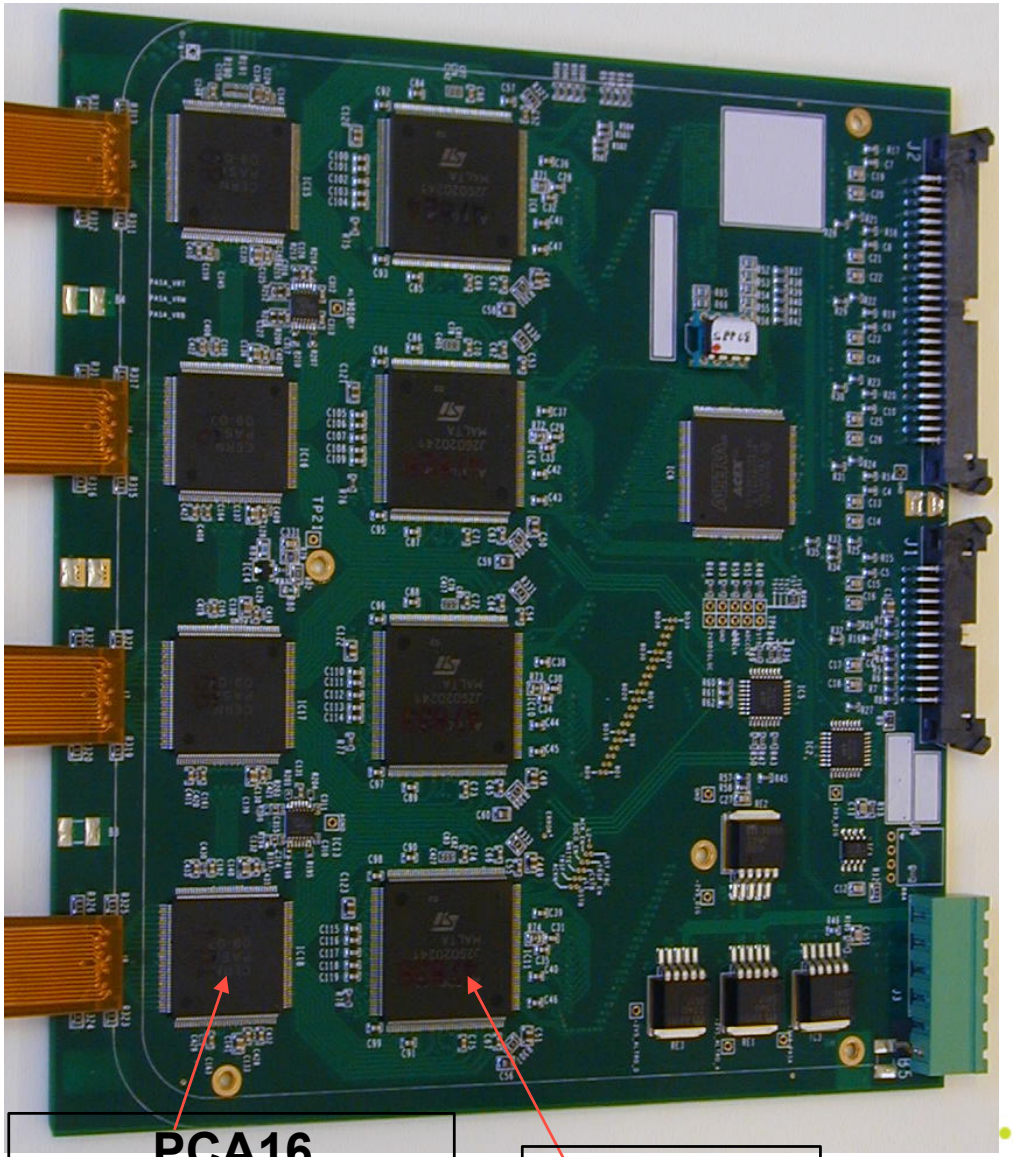
DRORC: Drivers and libraries from ALICE DAQ
DAQ: Plain C-code (ALICE code examples)
Control/Monitor: Java/C++/ROOT/C

CURRENT ALTRO READOUT

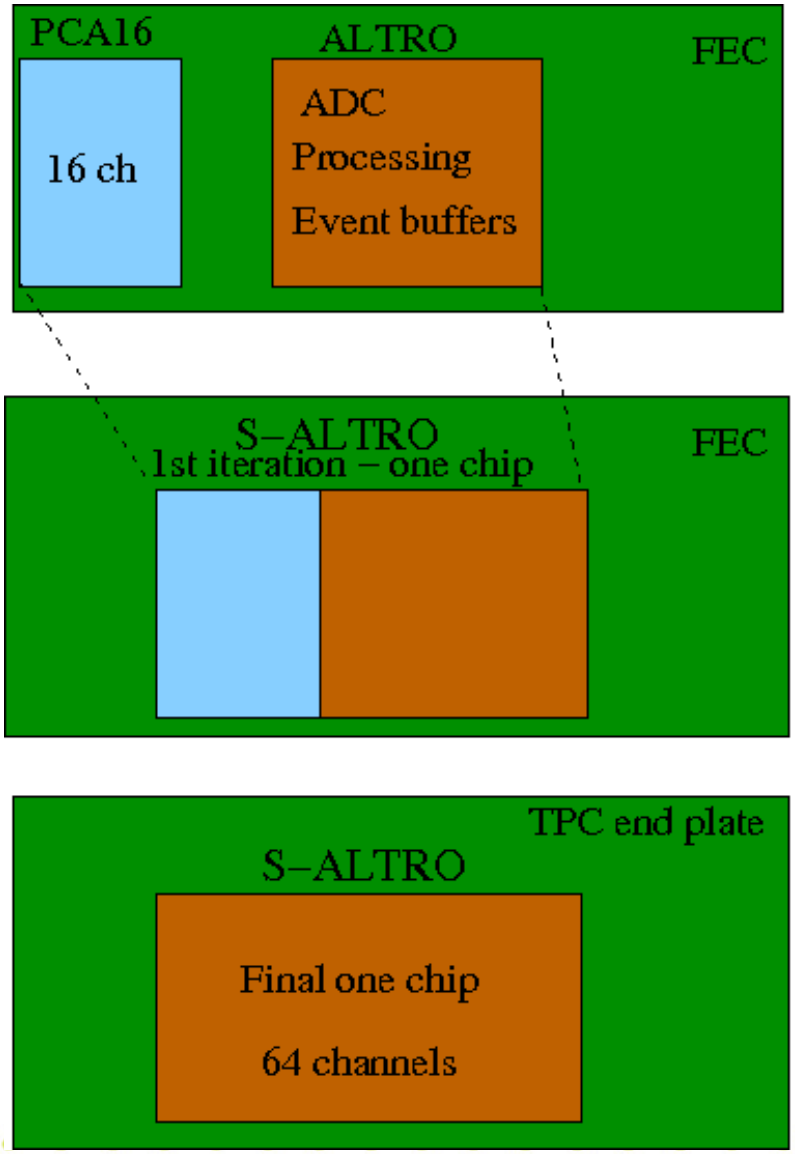


FEC Developments: S-ALTRO

Present :

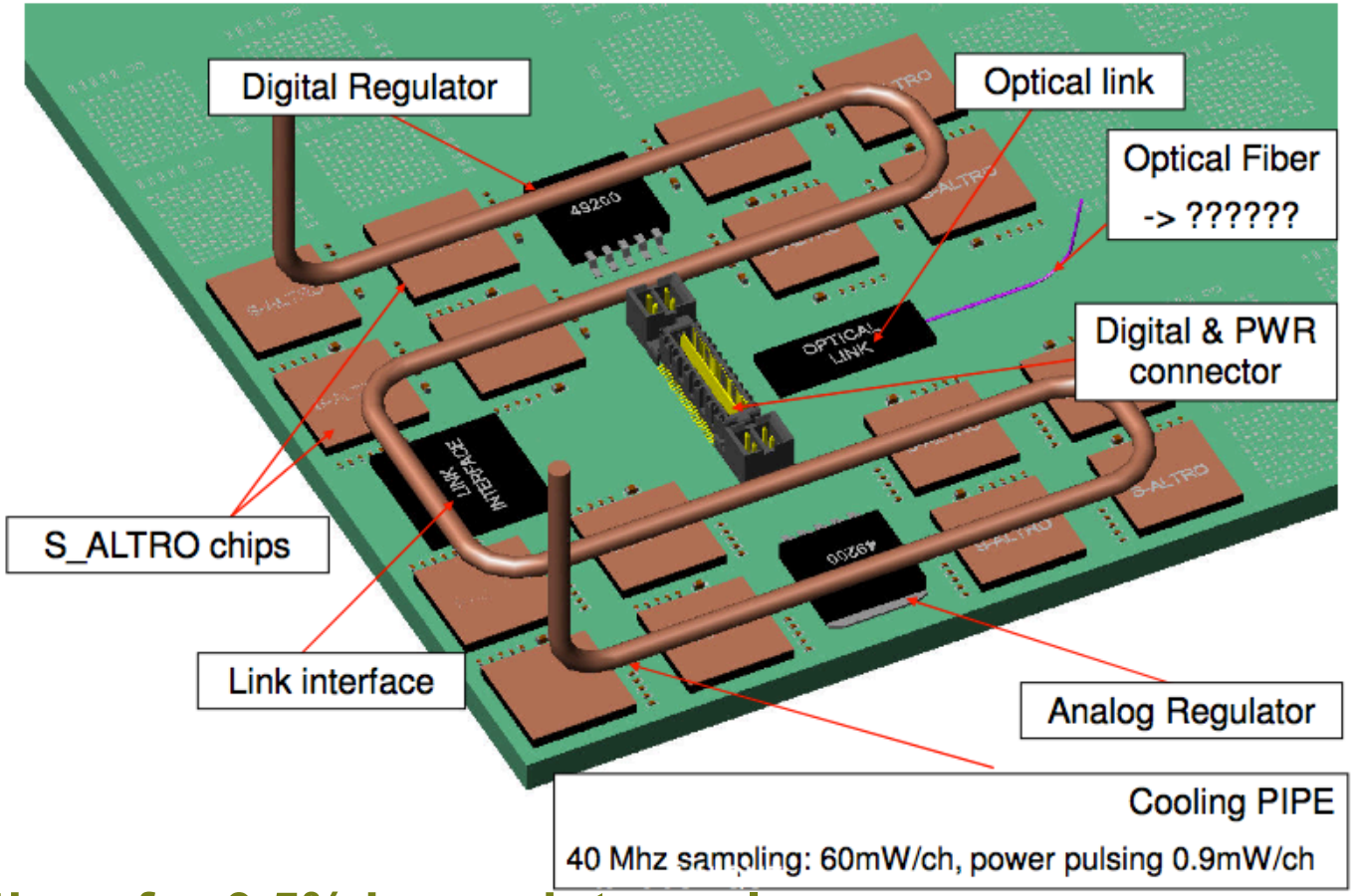


Future :



S-ALTRO mounted on TPC endplate

- S-ALTRO will be flip-chip mounted on PCB (! Cooling !)



Expectations for 0.5% beam duty cycle:

- average power / channel 0.5 mW / channel (at 10 MSPS)
- average power / m^2 100 W (at 10MSPS)

Other issues and developments

- For the short term:
  - **Try to use EUDAQ and TLU for the different readout electronics**
  - **This should help for future combined test beams**

- At much longer term:
  - **Investigate the possibility to use micro-TCA standard**

Conclusions and plans

- The Large TPC Prototype is working well, with GEMs and MICROMEGAS
- AFTER and ALTRO DAQ working fine as well
- For both, a lot of developments ongoing to reduce the size of the FE readout

+ Need to use EUDAQ and TLU for future combined test beams

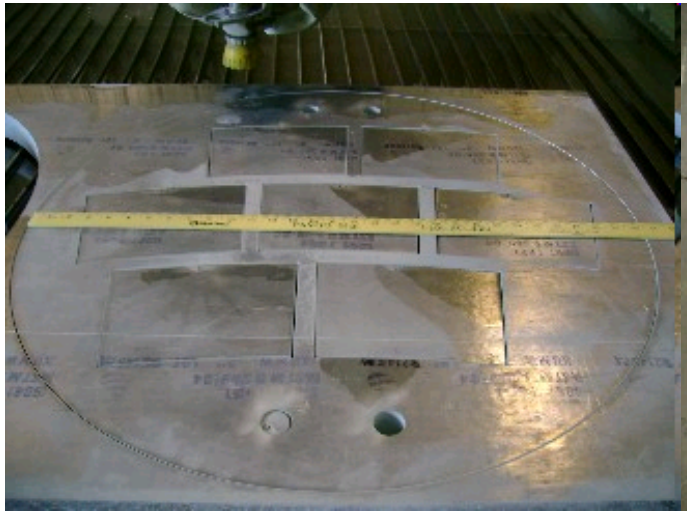
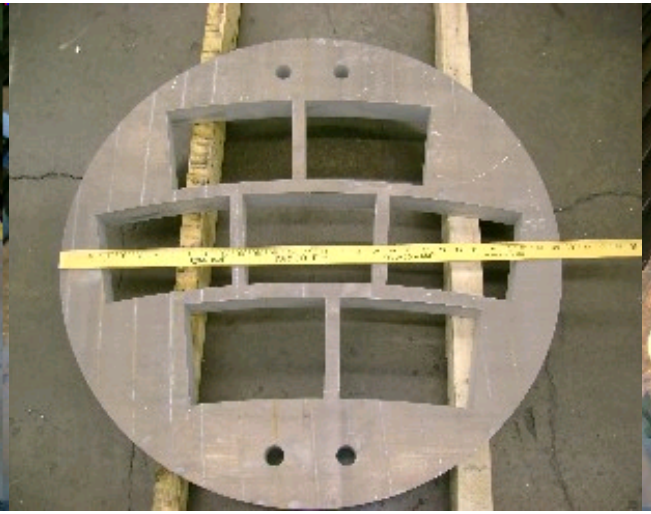
+ Interests to try microTCA standard

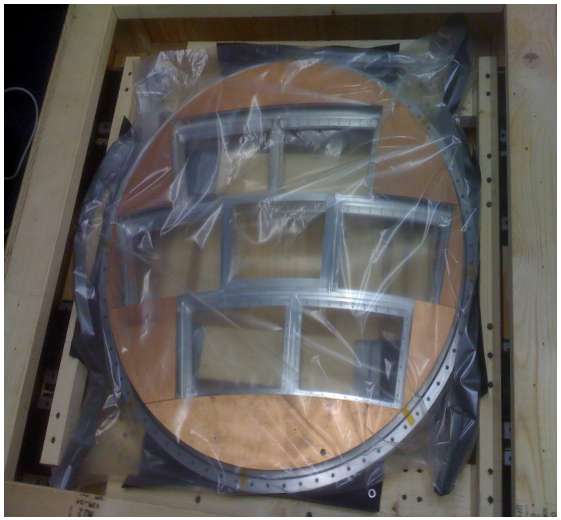
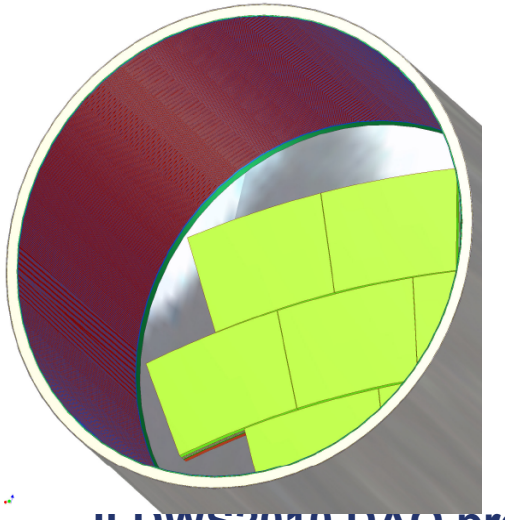
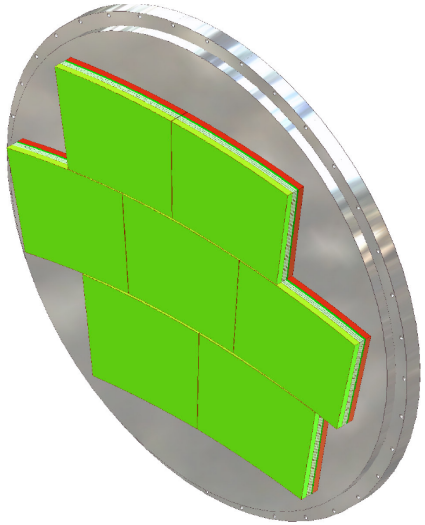
Back-up slides

TPC Performance

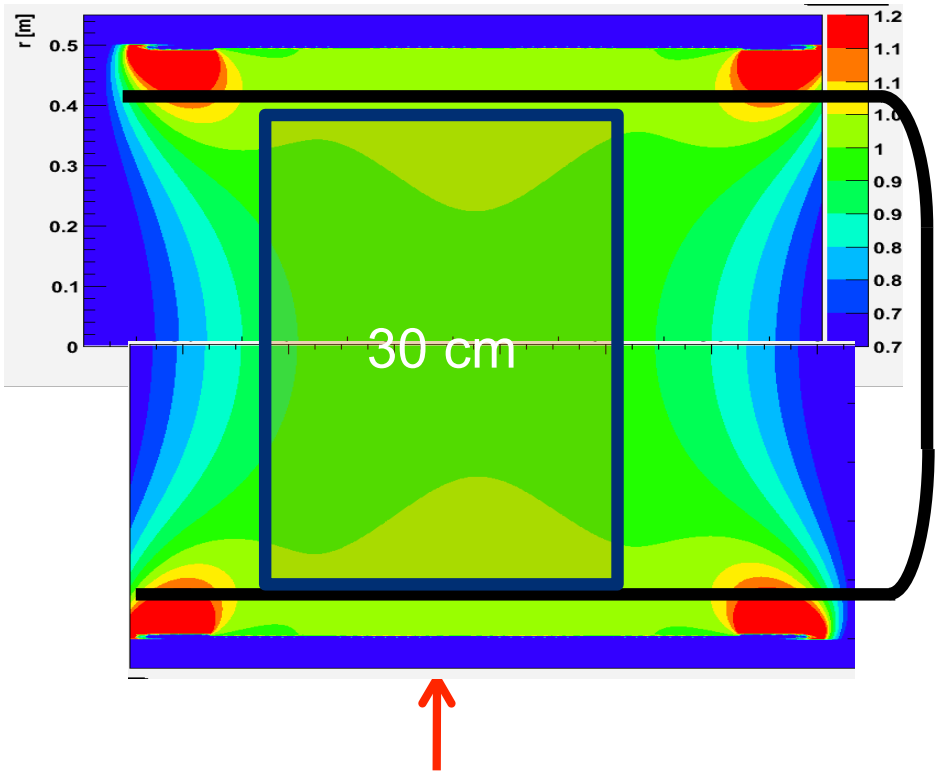
Size	$\phi = 3.6$m, L = 4.3m outside dimensions
Momentum resolution (3.5T)	$\delta(1/p_t) \sim 9 \times 10^{-5}$/GeV/c TPC only ($\times$ 0.4 if IP incl.)
Momentum resolution (3.5T)	$\delta(1/p_t) \sim 2 \times 10^{-5}$/GeV/c (SET+TPC+SIT+VTX)
Solid angle coverage	Up to $\cos\theta \simeq 0.98$ (10 pad rows)
TPC material budget	$\sim 0.04X_0$ to outer fieldcage in r
	$\sim 0.15X_0$ for readout endcaps in z
Number of pads/timebuckets	$\sim 1{\times}10^6$/1000 per endcap
Pad size/no.padrows	$\sim$ 1mm$\times$4–6mm/$\sim$200 (standard readout)
σ_{point} in $r\phi$	$< 100\mu$m (average over $L_{sensitive}$, modulo track ϕ angle)
σ_{point} in rz	$\sim$ 0.5 mm (modulo track θ angle)
2-hit resolution in $r\phi$	$\sim$ 2 mm (modulo track angles)
2-hit resolution in rz	$\sim$ 6 mm (modulo track angles)
dE/dx resolution	$\sim$ 5 %
Performance	$> 97\%$ efficiency for TPC only ($p_t > 1$GeV/c), and
	$> 99\%$ all tracking ($p_t > 1$GeV/c) [82]
Background robustness	Full efficiency with 1% occupancy,
	simulated for example in Fig. 4.3-4(right)
Background safety factor	Chamber will be prepared for 10 $\times$ worse backgrounds
	at the linear collider start-up

LP-TPC Endplate

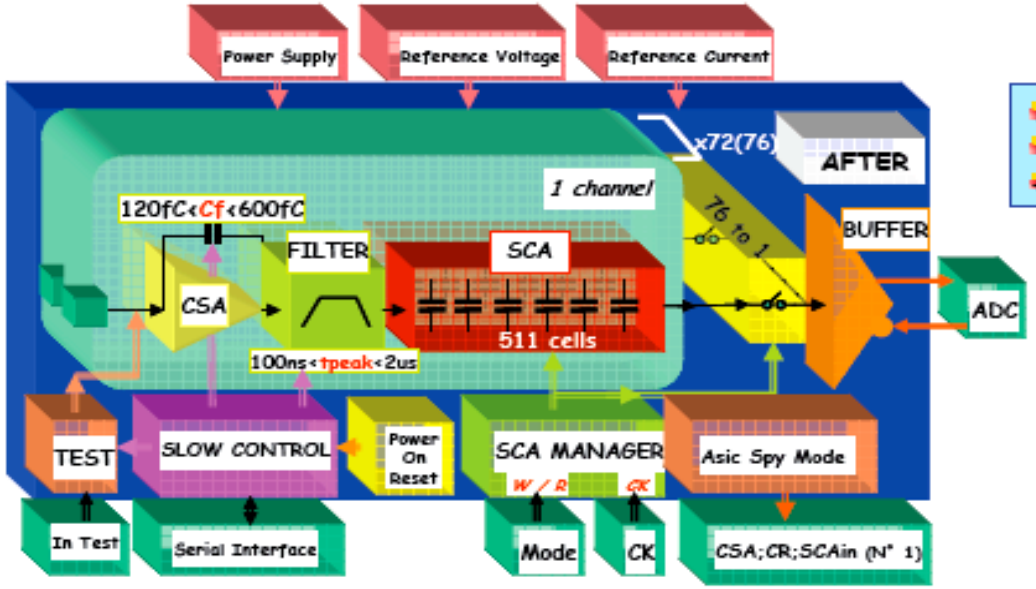
B field



Readout Electronics: AFTER

AFTER Main Features

dapnia saclay



- No zero suppress.
- No auto triggering.
- No selective readout.

Main features:

- **Input Current Polarity:** positive or negative
- **72** Analog Channels
- **4** Gains: 120fC, 240fC, 360fC & 600fC
- **16** Peaking Time values: (100ns to 2µs)
- **511 analog memory cells / Channel:**
  Fwrite: 1MHz-50MHz; Fread: 20MHz

- **Slow Control**
- **Power on reset**
- **Test mode:**
  calibration or test **[channel/channel]**
  functional **[72 channels in one step]**
- **Spy mode on channel 1:**
  CSA, CR or filter out

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