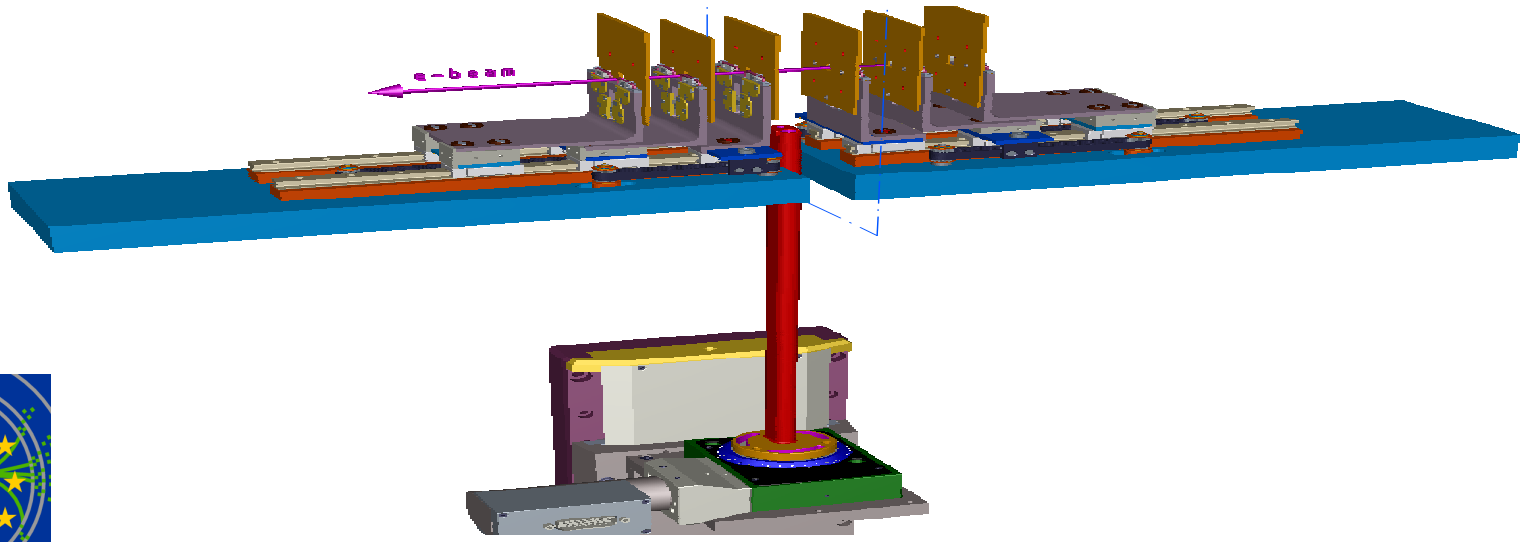
EU/AIDAQ for the pixel telescope

Emlyn Corrin & Daniel Haas
DPNC Genève (CH)
ILD DAQ Workshop
Paris, Jan 2010

- EUDAQ Status
  - Telescope
  - Sensors
  - Readout
  - Software
- AIDA
  - Sensors
  - Readout
  - Rates
  - Data format

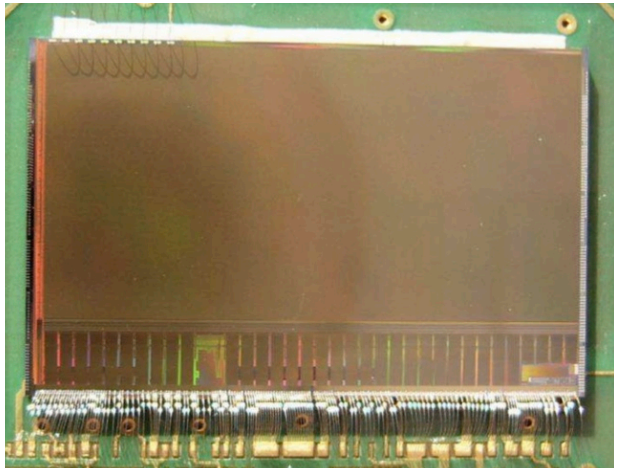
EUDET: Telescope

- Six sensor planes on two arms
- Space for DUT in between



EUDET: Sensors

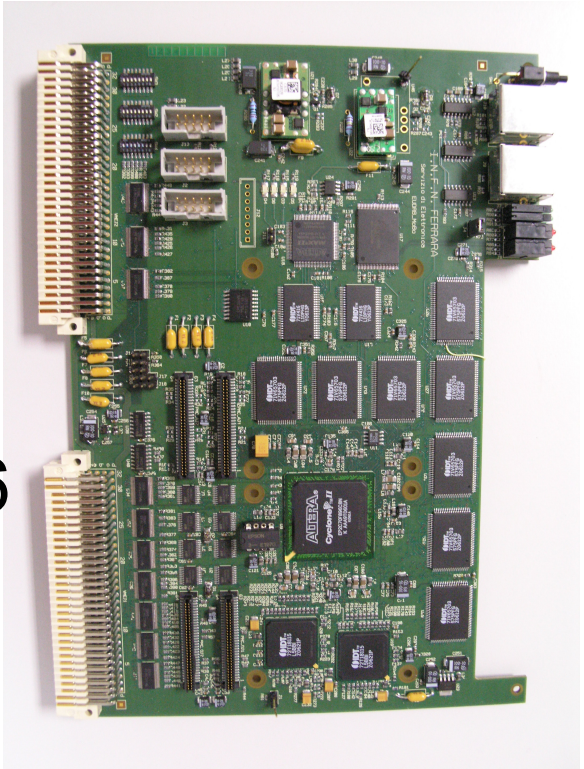
- Mimosa 26 (MAPS)
- 10.6 × 21.2 mm
  with 18.4 µm pitch
  (576 × 1152 pixels)
- 115 µs integration time
- Integrated discriminator
  and zero-suppression



- Two serial links at 80 MHz, up to 9216 bits / frame
- Mean data rate: ~100 Mbit/s per sensor

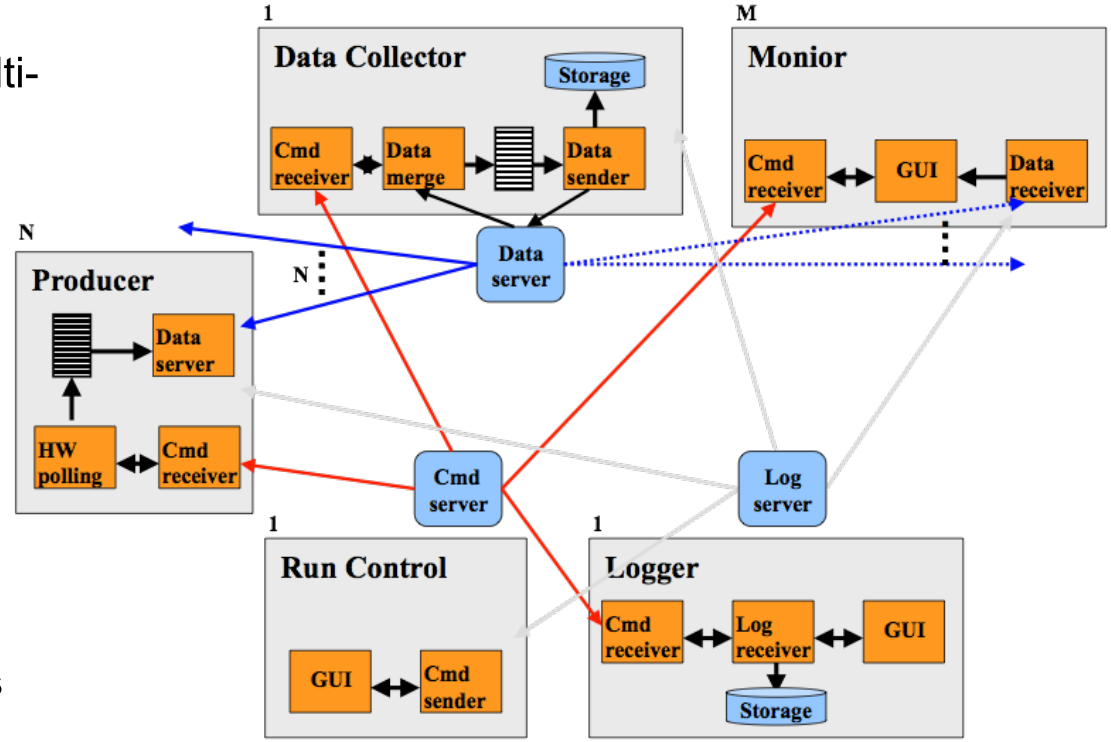
EUDET: Readout

- EUDRB: VME board with Altera FPGA
- Pluggable daughter cards
- Designed for analogue MAPS chips, and adapted to Mimosa 26
- One board per sensor
- Read out over VME by MVME6100
- Data then sent over Gigabit Ethernet to DAQ



EUDAQ: Software

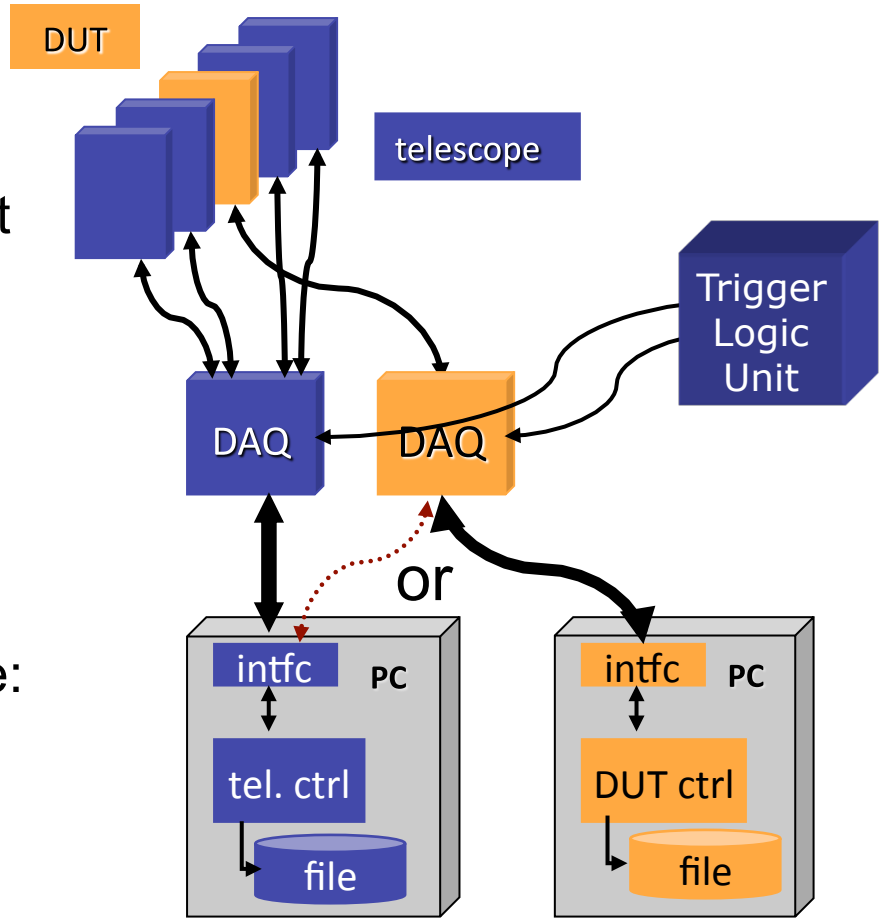
- Platform independent (MacOSX, Linux, Windows)
- Object oriented, distributed and multi-threaded
- Highly modular, but light-weight
- DAQ Software is divided into many parallel tasks:
  - RunControl to steer the task
  - several Producer tasks read the hardware
  - one DataCollector task bundles events, writes to file and sends subsets for monitoring
  - Several Online - Monitoring tasks
  - Logger task allows to see what is going on

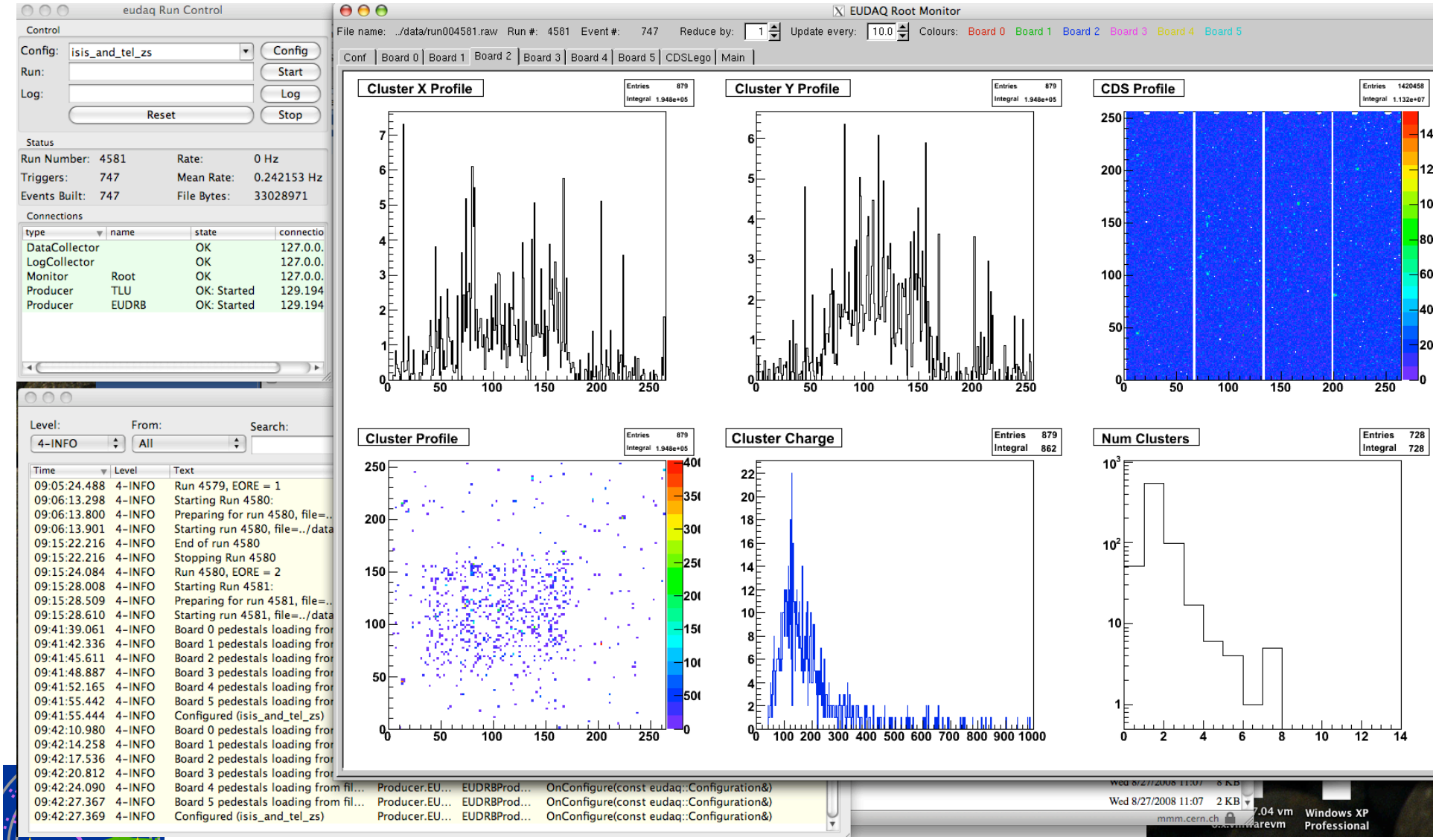


http://projects.hepforge.org/eudaq/

EUDAQ: Integration Concept

- How to integrate the DUT hardware with the EUDET beam telescope?
  - different groups with different detector technologies and different, pre-existing DAQ systems
- Use completely different hardware and DAQ for the DUT and the telescope
- Two levels of integration possible:
  - "easy" solution: at trigger level
  - full integration on DAQ software level

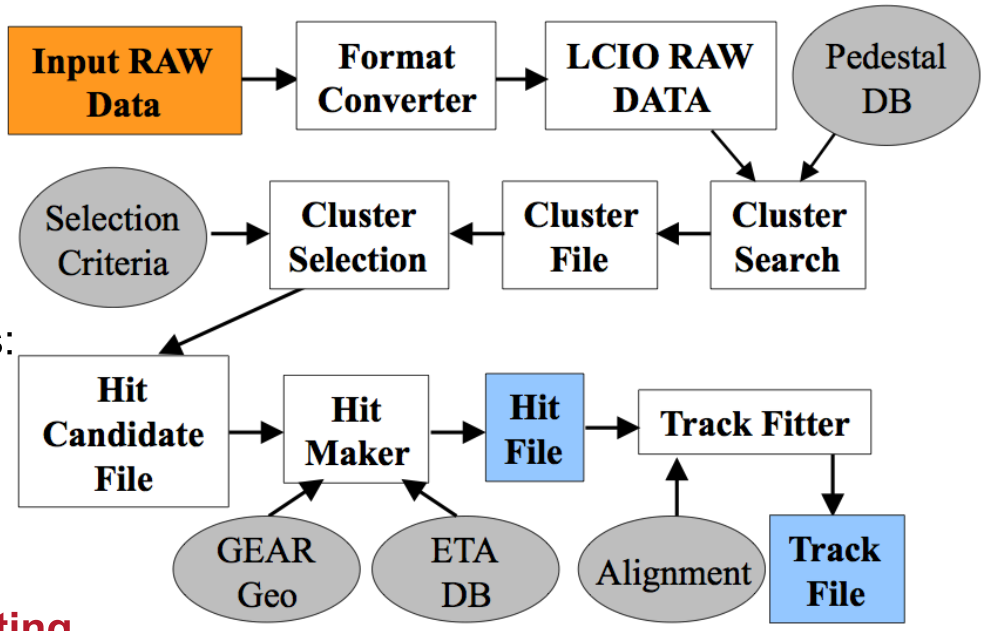



eudaq Run Control
Control
Config: isis_and_tel_zs
Run:
Log:
Reset
Config
Start
Log
Stop
Status
Run Number: 4581
Rate: 0 Hz
Triggers: 747
Mean Rate: 0.242153 Hz
Events Built: 747
File Bytes: 33028971
Connections
type name state connectio
DataCollector OK 127.0.0.
LogCollector OK 127.0.0.
Monitor Root OK 127.0.0.
Producer TLU OK: Started 129.194
Producer EUDRB OK: Started 129.194
Level: From: Search:
4-INFO All
Time Level Text
09:05:24.488 4-INFO Run 4579, EORE = 1
09:06:13.298 4-INFO Starting Run 4580:
09:06:13.800 4-INFO Preparing for run 4580, file=..
09:06:13.901 4-INFO Starting run 4580, file=../data
09:15:22.216 4-INFO End of run 4580
09:15:22.216 4-INFO Stopping Run 4580
09:15:24.084 4-INFO Run 4580, EORE = 2
09:15:28.008 4-INFO Starting Run 4581:
09:15:28.509 4-INFO Preparing for run 4581, file=..
09:15:28.610 4-INFO Starting run 4581, file=../data
09:41:39.061 4-INFO Board 0 pedestals loading fro
09:41:42.336 4-INFO Board 1 pedestals loading fro
09:41:45.611 4-INFO Board 2 pedestals loading fro
09:41:48.887 4-INFO Board 3 pedestals loading fro
09:41:52.165 4-INFO Board 4 pedestals loading fro
09:41:55.442 4-INFO Board 5 pedestals loading fro
09:41:55.444 4-INFO Configured (isis_and_tel_zs)
09:42:10.980 4-INFO Board 0 pedestals loading fro
09:42:14.258 4-INFO Board 1 pedestals loading fro
09:42:17.536 4-INFO Board 2 pedestals loading fro
09:42:20.812 4-INFO Board 3 pedestals loading fro
09:42:24.090 4-INFO Board 4 pedestals loading from fil... Producer.EU... EUDRBProd... OnConfigure(const eudaq::Configuration&)
09:42:27.367 4-INFO Board 5 pedestals loading from fil... Producer.EU... EUDRBProd... OnConfigure(const eudaq::Configuration&)
09:42:27.369 4-INFO Configured (isis_and_tel_zs) Producer.EU... EUDRBProd... OnConfigure(const eudaq::Configuration&)
EUDAQ Root Monitor
File name: ../data/run004581.raw Run #: 4581 Event #: 747 Reduce by: 1 Update every: 10.0 Colours: Board 0 Board 1 Board 2 Board 3 Board 4 Board 5
Conf Board 0 Board 1 Board 2 Board 3 Board 4 Board 5 CDSLego Main
Cluster X Profile
Cluster Y Profile
CDS Profile
Cluster Profile
Cluster Charge
Num Clusters
Entries 879
Integral 1.948e+05
Entries 879
Integral 862
Entries 728
Integral 728
Wed 8/27/2008 11:07 2 KB
Windows XP Professional

Analysis & Reconstruction Software

EUTelescope:

- Set of relevant high level objects (like tracks or space points) to characterize the DUT
- Histograms of important figures of merit.
- Based on available/tested software tools:
  - Single sensor analysis → **sucimaPix** (INFN)
  - Eta function correction → **MAF** (IPHC)
  - Track fitting → **Analytical track fitting** and straight line fitting
  - Alignment → **Millepede II**
  - Framework → ILC Core software = **Marlin + LCIO + GEAR + (R)AIDA + CED**



- Sticking to the ILC de-facto standard offers the possibility to easily use the GRID
- Each module is implemented in a Marlin processor
  execute all of them together, or stop after every single step

AIDA: Sensors

- Mimosa 26 to be replaced with Ultimate chip, currently in development
- Double the active area (~2 × 2 cm)
- Possibly use ADC instead of discriminators, enhanced resolution even with larger pitch

AIDA: Readout

- EUDRB to be replaced with new digital readout system
- NI Flex RIO currently being evaluated, work in progress at IPHC Strasbourg
- Tagging of events & clock distribution: TLU will support this this year (may need a ‘better’ TLU for AIDA and interface to Calice clock distribution)

NI FlexRIO – Custom I/O for LabVIEW FPGA and PXI

NI PXI-795xR *NEW!*

- Virtex-5 FPGA programmable with the LabVIEW FPGA Module
- Up to 128 MB onboard DDR2 DRAM
- Access to 132 single-ended I/O lines configurable as 66 differential pairs
- Custom cable I/O with the NI FlexRIO Adapter Module Development Kit (MDK)
- 100 MHz digital I/O with the NI 6551 adapter module
- 8 DMA channels for high-speed data streaming

Operating Systems
- Windows Vista/XP/2000
- LabVIEW Real-Time

Required Software
- LabVIEW
- LabVIEW FPGA Module
  - LabVIEW code compiler for FPGAs
  - Emulated debugging mode

Recommended Software
- LabVIEW Real-Time Module

Driver Software (included)
- NI-IO

Model	Bus/Form Factor	FPGA	FPGA I/O	Onboard Memory (DRAM)
[illegible]	PXI	Virtex-5 LX30	96 differential or 192 single-ended	0 MB
[illegible]	PXI	Virtex-5 LX30	96 differential or 192 single-ended	128 MB
[illegible]	PXI	Virtex-5 LX85	96 differential or 192 single-ended	128 MB
[illegible]	PXI	Virtex-5 LX110	96 differential or 192 single-ended	128 MB

Table 1. NI FlexRIO FPGA Modules

Current Status

- 66 Differential inputs
- User defined Adaptator Module
- User defined on-board fw (deserialisation)
- PXI bus → Average ~ 60 MB/s

- 1 Mi26 plane @ 10 kframe/s → ~ 25 MB/s
  - 4 Planes ~ 100 MB/s → 60 % of full speed
  - 6 Planes ~ 150 MB/s → 40 % of full speed

Cost ?

- PXI-7951R (No RAM) ~ 2,8 K€
- PXI-7952R (128 MB RAM) ~ 3,7 K €
- Adaptator module SE 100 MHz ~ 1 K€
  - LVDS foreseen for end of summer
- PXIe Crate + CPU ~ 8 K €
- Adaptater Module Development Kit ~ 4,6 K€
  - Overhead of 4,6 K € (CAD files etc …)
  - ~ 60 € / enclosure

Future ?

- PXIe ? 250 MB/s / lane … X 1, 2, 4, 8, 12, 16, 32 → 6 GB/s …
  - Can't be handled by software …
  - Writing to disk + % of monitoring by software
- Fast serial links Gb/s
  - Direct handling on FPGA ?
  - User HW on Adaptater Module

AIDA: Data rates

- Performance: Still need to do the precise math, but:
- Software framework will achieve 'normal' network performance (Bandwidth/2) (status quo for EUDET)
- 1 "Ultimate Chip" can achieve up to 200 Mbits/second, assuming ~20 sensors in total (telescope + test-box): ~400 MB/s
- Current Flex RIO can achieve up to 80 MB/s per card
- Need 10 Gbit hardware for the DAQ system

AIDA: Data format

- For test-beams:
  - custom binary raw format first,
  - hit conversion afterwards a good choice
- Currently, we also convert to LCIO in step 2, could be done immediately
- Users can just dump their raw data
- Then work on decoding in parallel to starting data taking
- Bugs in decoding do not affect already collected data

EUDAQ to AIDAQ

Missing steps

- Scalability: Currently, one central data-collector, could easily be decentralized, need still a central RunControl
- Slow Control System: nothing implemented
- Metadata: On file, should likely move to a DB
- Manpower: Emlyn Corrin, need him+more

Conclusions

- Have to finish EUDET successfully this year (lots of users/testbeam, heavy workload)
- AIDA proposal must go through, before real work
- Manpower in Geneva is reduced, only Emlyn remains
- Hardware/Software solutions for reading out pixels within AIDA are on the way, based on:
  - EUDAQ software framework
  - LCIO/Marlin based analysis framework
  - Commercial readout boards for the sensors