Available software & hardware DAQ systems at LPNHE for Silicon tracker studies

IXTH SILC MEETING
PARIS, FRANCE

Alexandre CHARPY & LPNHE team

Goal

Conducted by LPNHE:

- Research baseline: wafer 6”-8”, 200µm of thickness, pitch of 50 µm, transparency ~70%, active edge

Edgless with SOI technology

VTT- Juha Kalliopuska

Manufacturing achievement:

- edgeless & pixels sensors, 6” wafer, 50 µm pitch

HPK designed by Vienna w/wo surface treatment of silicon wafers(Santander)

→ 50µm pitch, 320µm of thickness
→ ~ 20% transmittance
→ Alignment System (IFCA) using an infra-red laser in labs & tests beam

3D technology (short strips)

FBK-irst-U. Trento/INFN - Gian Franco Dalla Betta

- 250 µm thick substrate, full 3D detectors and passing-through columns
- New double-sided process defined, no need for support structure, allow dual read-out

Edgeless planar strips

FBK-irst-U. Trento/INFN - Gian Franco Dalla Betta

- Prototyped sensors 2.5x5cm^2 (Trento & LPNHE)
- full characterization at Lab followed by beam test & HPK comparison

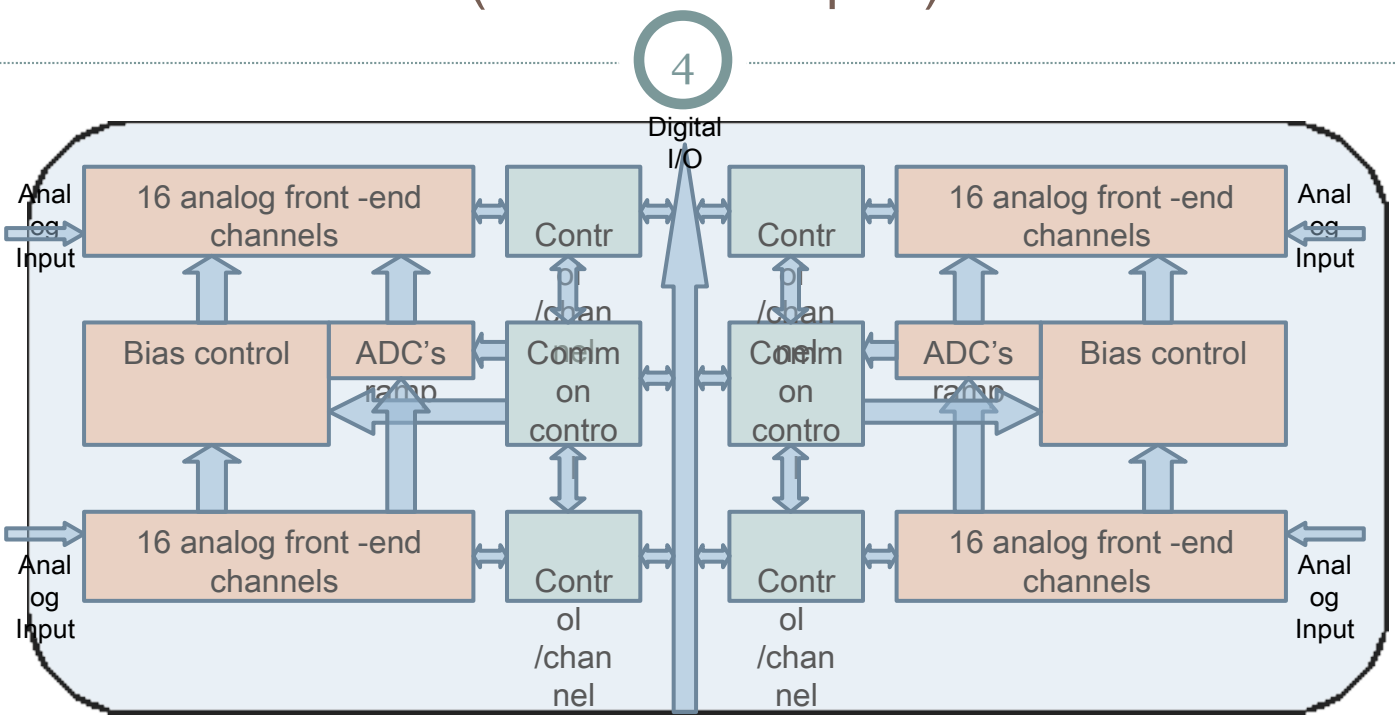
SiTr130_128 chips
(under developed)

2010 : Conception-achievement and test of the new version of the SiTr130-128 chip → IBM technology, 130nm

- 128 channels + JTAG
- 0.5*1 cm^2 of silicon, thin down
- Numerical output with pre-amplifier, shaper, reinitialisation, 8x8 analog pipeline for pulse reconstruction, zero suppression, single ramp ADC, integrated numerical control, robustness & flexibility, power cycling, serialization
- Goal: silicon surface optimisation, modular architecture
- Under Study : **direct connection chip/senseur**

LPNHE
Laboratoire de
Physique Nucléaire
et des Hautes Energies

SiTr130_128 chips
(under developed)

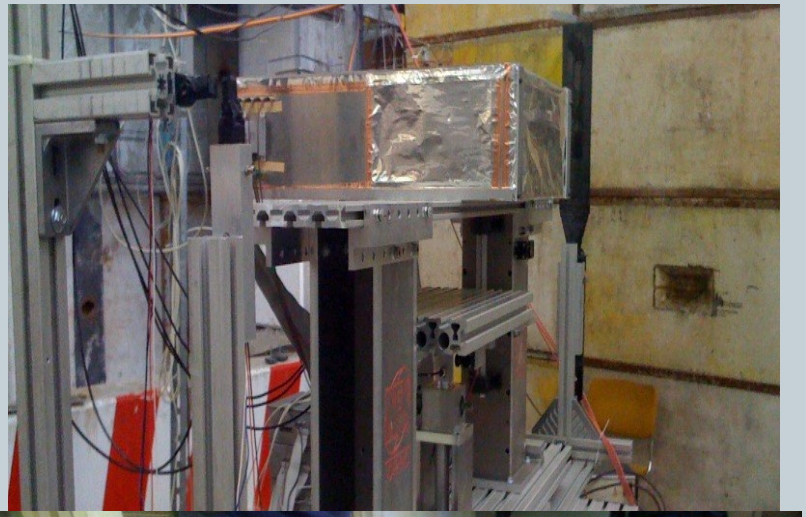


- Zero suppression
- 8x8 analog pipeline for pulse reconstruction
- Single ramp ADC → 10 bits
- Data tagging+timestamping+check >48 bits
- Chips serialization
- i/o @ 48 MHz (final-100MHz)

Comparison with VA1 chip coupled w ith 16 bits ADC used for Si sensor technology

2009 Setup

- Standalone telescope, with five silicon sensors layers: 512 active strips/modules
- Intented to be easily integrated to a test beam
  - High customization
  - All Electronic features In One “AlteraBox”
  - Main functionalities (Peaking Time, Laser Alignment etc…)
  - DAQ – read both FEE systems (new SiTr130-128 chips & VA1)



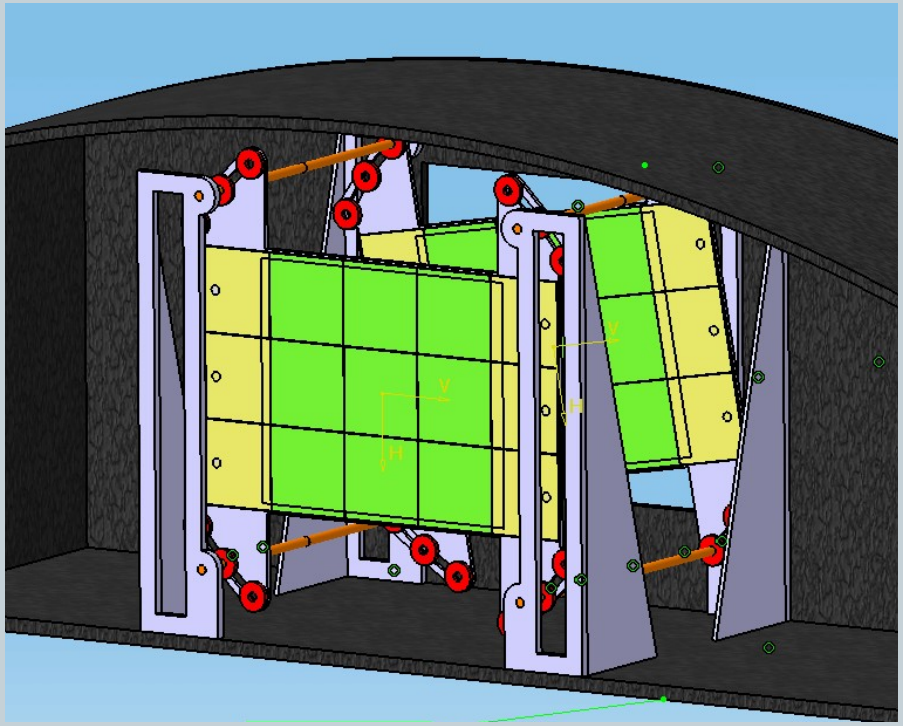
Prospect for 2010

<u>Increase of the number of channel to read:</u>

- Nowadays: 2560 channels
- EUDET and transnational tests (mi-2010) => 15000 to 20000 channels
- Update to VA1 to SiTr130-128

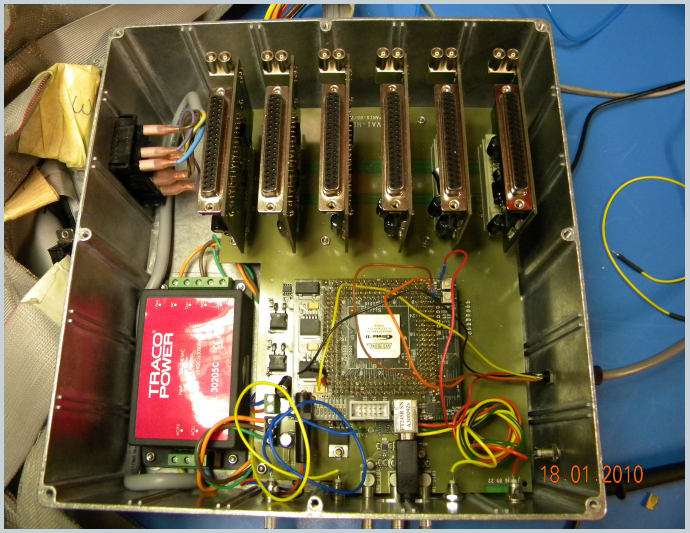
- 2011-2012 -> much more !!!

<u>Chip substitution:</u> VA1 → SiTR130-X (16bits → 64 bits per channel) (see H.PHAM)



DAQ Hardware

- Evolutive DAQ Hardware ToolKit (EUDET deliverable)
  - Adapted to both: VA1 (référence) prototypes SiTr-130 and next, mix mode (VA1+SiTr chips)
  - USB/FPGA interface with microtcontroler
  - TTL/NIM for triggering and laser alignement
  - AlteraBox chaining
  - Power supplied embedded
  - Need to integrate the TLU ?



Faster serial Interface:

- Ethernet & Light peak (optical link @ 10 Gb) → end of 2010-201

Development toward the final DAQ design for ILD → link with the mechanical constraint

Data Acquisition System software Narval

Acquisition requirement:

- Increasing of the data size management
- Addressing of the data
- On-line control
- High Flexibility

Narval is the main frame (ADA-oriented) https://forge.in2p3.fr/projects

→ module programming: ADA/C/C++

→ *Can be easily connected to any global DAQ software → what is needed ?*

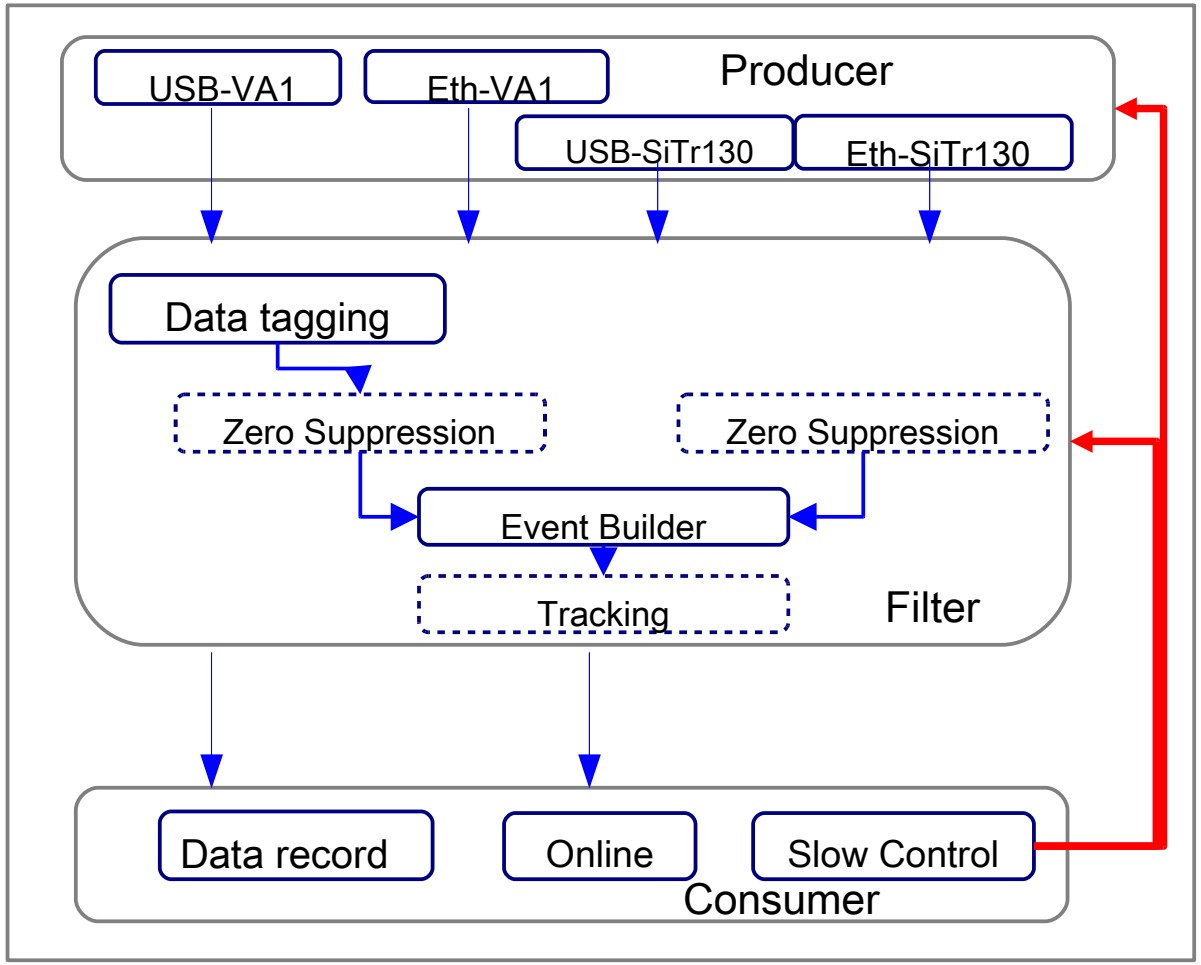
→ *Can easily include another DAQ system*

→ *ENX for the slow Control*

FPGA system is handled by a full VHDL software package

Data Acquisition System software
Narval

Master: Narval as a linux server



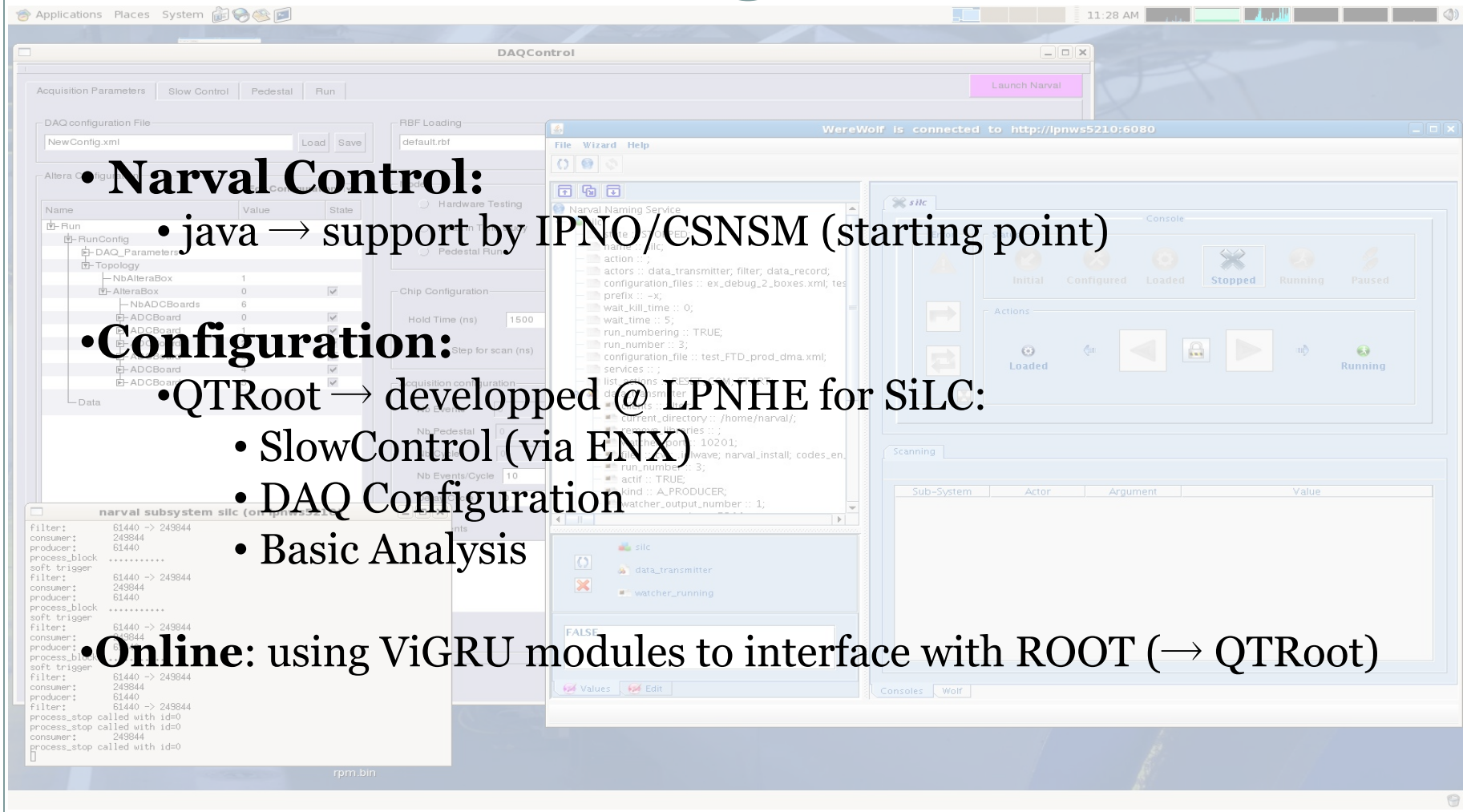
- Three basic actors:
  → Producers
  → Filters
  → Consumers
  (could be created)

- Dedicated libraries in C/C++/ADA95

- High flexibility with very simple scripts & xml files

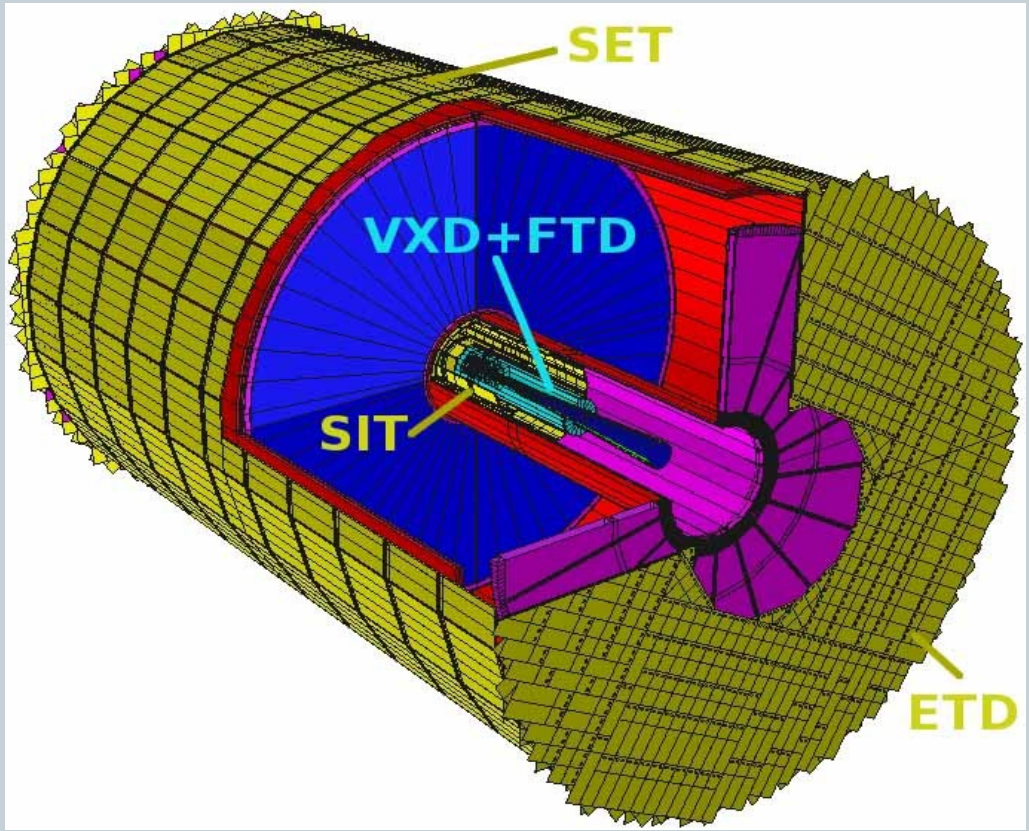
Raw Data format for combined test beam ?

Data Acquisition System
Software



- **Narval Control:**
  - java → support by IPNO/CSNSM (starting point)
- **Configuration:**
  - QTRoot → developped @ LPNHE for SiLC:
    - SlowControl (via ENX)
    - DAQ Configuration
    - Basic Analysis
- **Online**: using ViGRU modules to interface with ROOT (→ QTRoot)

Prospect for 2012
The Silicon Envelope of ILD



Detailed design
GEANT4 simulation both in MOKKA & ILCROOT
(here) & mechanical design (CATIA) in progress

Total number of modules:

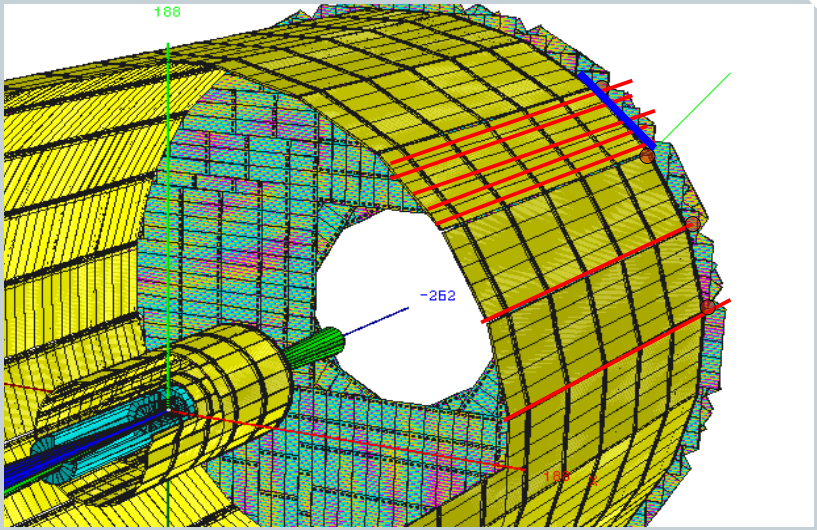
500 (SIT) + 2500 (SET) + 2000 (ETDs)
5000 modules of 1792 channels

Total number of channels:

10^6 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)
$10 x10^6$ channels
~5.12 Gbytes

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30

Prospect for 2012
The Silicon Envelope of ILD



- On the “module”:
Chaining of 14 SiTR130-128

- “Super Module”:
Chaining the adjacent ladders toward a level 1 concentrator

- Half cylinder (“Detector Element”):
Level 1 concentrator (toward level 2 ?)

- Toward the global Silicon DAQ system by Optical fibers

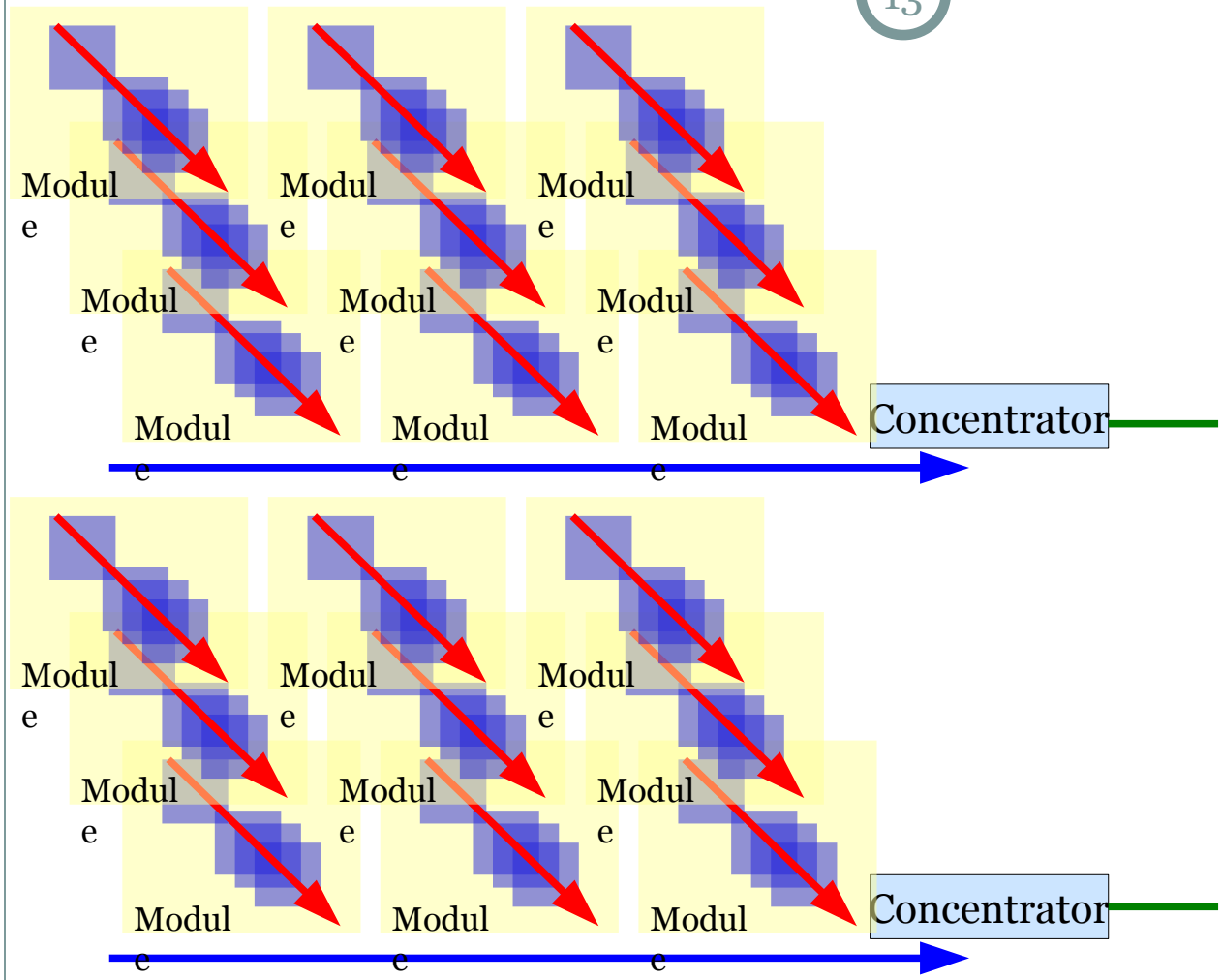
- Send to Global DAQ system

Depending on the final requirements

Topology is In progress

DAQ Silicon tracking architecture

A global schematic view of the Silicon DAQ architecture



3 “floors”:

F1: chip on sensor, full readout chain in a single chip (A/D, zero suppression, multiplex ...)

F2: on detector sides, daisy chains chips, data buffering, preprocessing ...

F3: processing, azimuthal sector, track reconstruction

Si Tracking DAQ – ILC workshop, Warsaw

Thanks for your intention