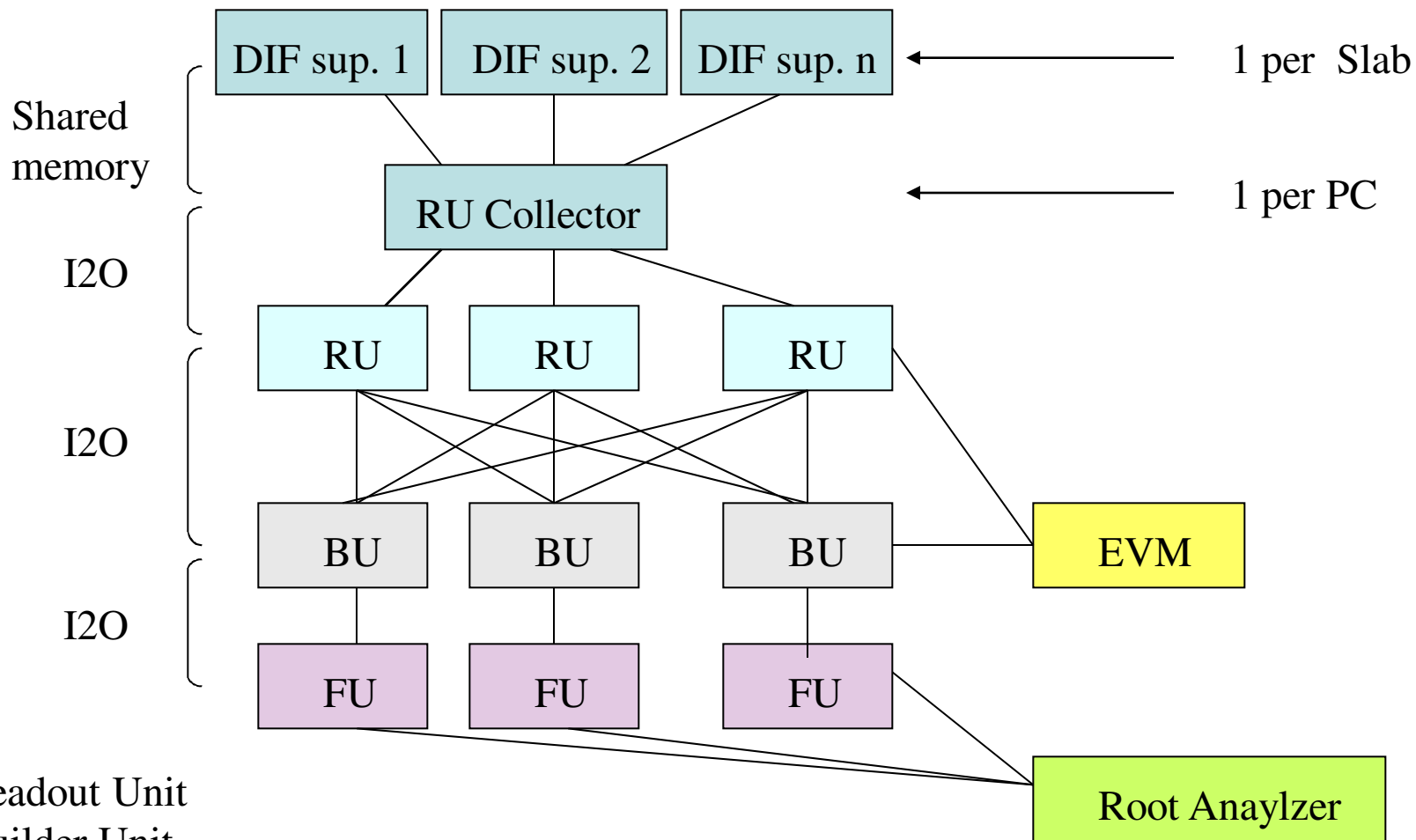


SDHCAL DAQ status in Lyon

C. Combaret, for the IPNL team

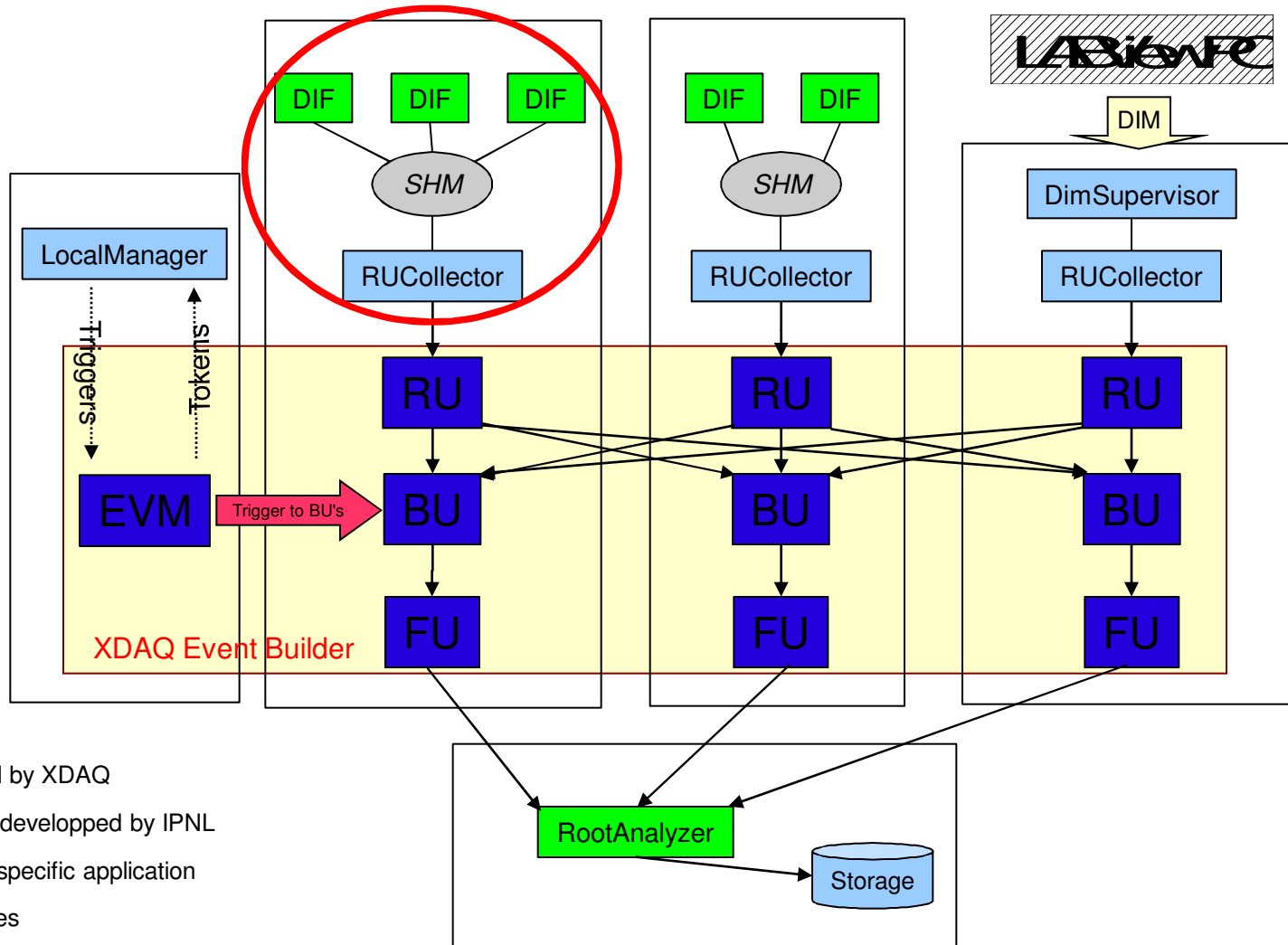
1. Integration of XDAQ event builder (L. Mirabito)
2. Online analysis (L. Mirabito)
3. DAQ can now be started by main FSM instead of Manual control (still possible).
4. Coupling of small RPC DAQ (Labview) with m2 DAQ (Xdaq) using DIM (R. Dellanegra & L. Mirabito)
5. HR2 m2 tests : ASU OK, Xdaq OK. Scurve OK.
6. Power pulsing in (good) progress
7. Environmental monitoring : temperature, pressure and humidity (S. Cuzon)



RU: Readout Unit
 BU: Builder Unit
 FU: Filter Unit

A detailed example

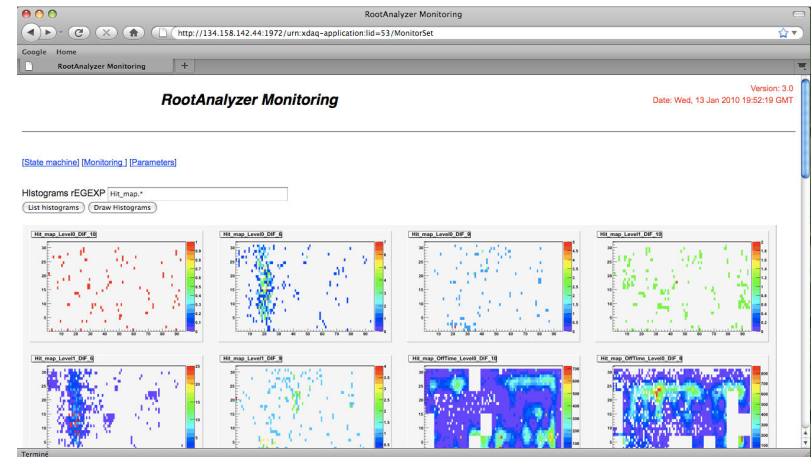
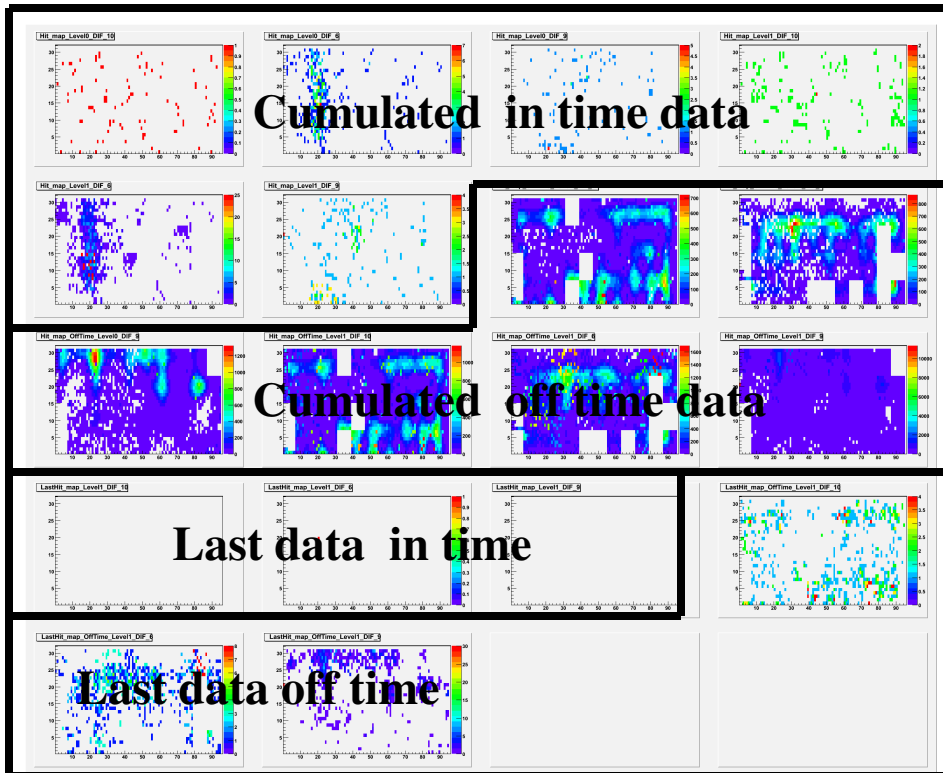
Must run on the same PC



- Each application is a web service and can publish web pages
 - Direct hardware access
 - Monitoring
- Each application can be controlled by an FSM
 - Global configuration using SOAP message from the LocalManager
- The Event Builder (EVM/RU/BU/FU) is provided and maintained by XDAQ
 - Software triggers/tokens exchange between EVM and LocalManager
 - Some generic software developed
 - I2O interfaces from RUCollector and RU and from FU to RootAnalyzer
 - Local manager trigger loop
- Main constraint: Trigger driven
 - Trigger veto board needed (controlled by the LocalManager)
 - Ok for external trigger, further development needed for auto trigger EVB

For each DIF :

NumberOfAsic_InTime	Hit_map_Level0/1
NumberOfFrame_vs_Asic_InTime	Hit_map_OffTime_Level0/1
NumberOfHit_per_Frame_InTime	LastHit_map_Level0/1
NumberOfHit_per_Frame_OffTime	LastHit_map_OffTime_Level0/1
NumberOfHit_vs_Asic_InTim	NumberOfFrame_vs_Asic

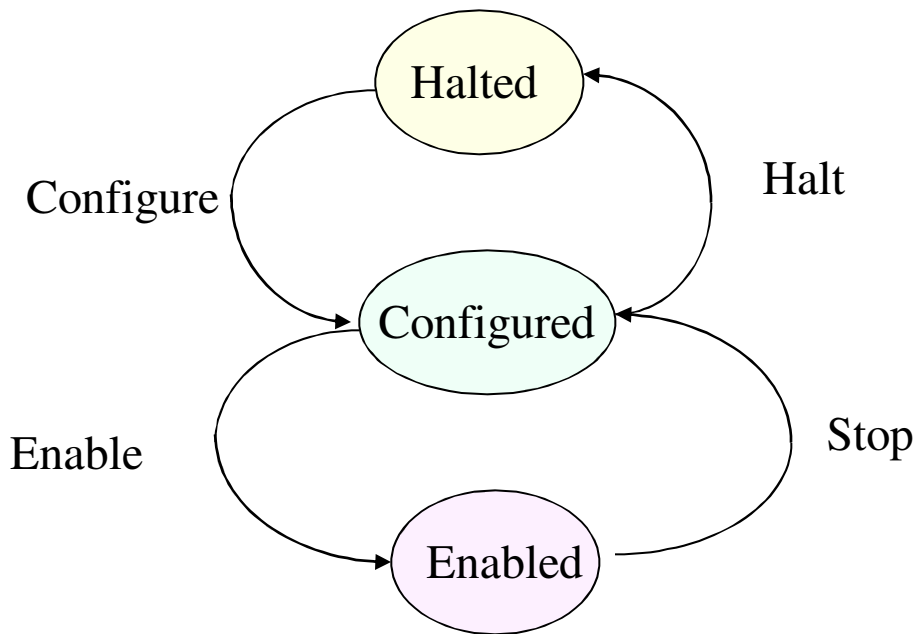
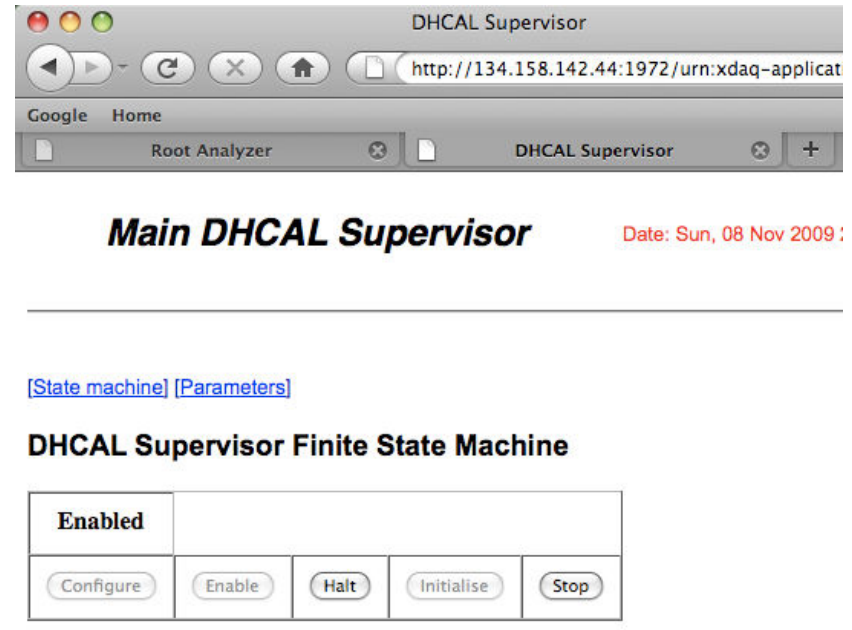


Use of DAQ main FSM

Each Xdaq application can be controlled by the main FSM.

To do this, it must only know the following states : **Halted**, **Configured** and **Enabled**

And implement the following transitions: **Configure**, **Enable**, **Halt** et **Stop**.

Main DHCAL Supervisor Date: Sun, 08 Nov 2009 :

[\[State machine\]](#) [\[Parameters\]](#)

DHCAL Supervisor Finite State Machine

Enabled				
Configure	Enable	Halt	Initialise	Stop



Hardroc2 m2 Slab tests

One buffer for Slow control slow clock is required to access 1 slab of 48 HR2

SLC clock is ok for a single ASU but too depredated for one slab of 48 HR2.

Slab fully functional :

- SLC OK
- Power OK
- SLC OK
- Readout OK
- Calibration OK

We learnt a lot from HR1 m2 : EMI/grounding/shielding problems and (then) solutions found for HR1 successfully implemented in HR2 ASUs

Still some tests ongoing on the way to connect 2 ASU together (see Hervé's talk)



Power pulsing on Hardroc 2 ASU : method

As discussed with HR2 designers :

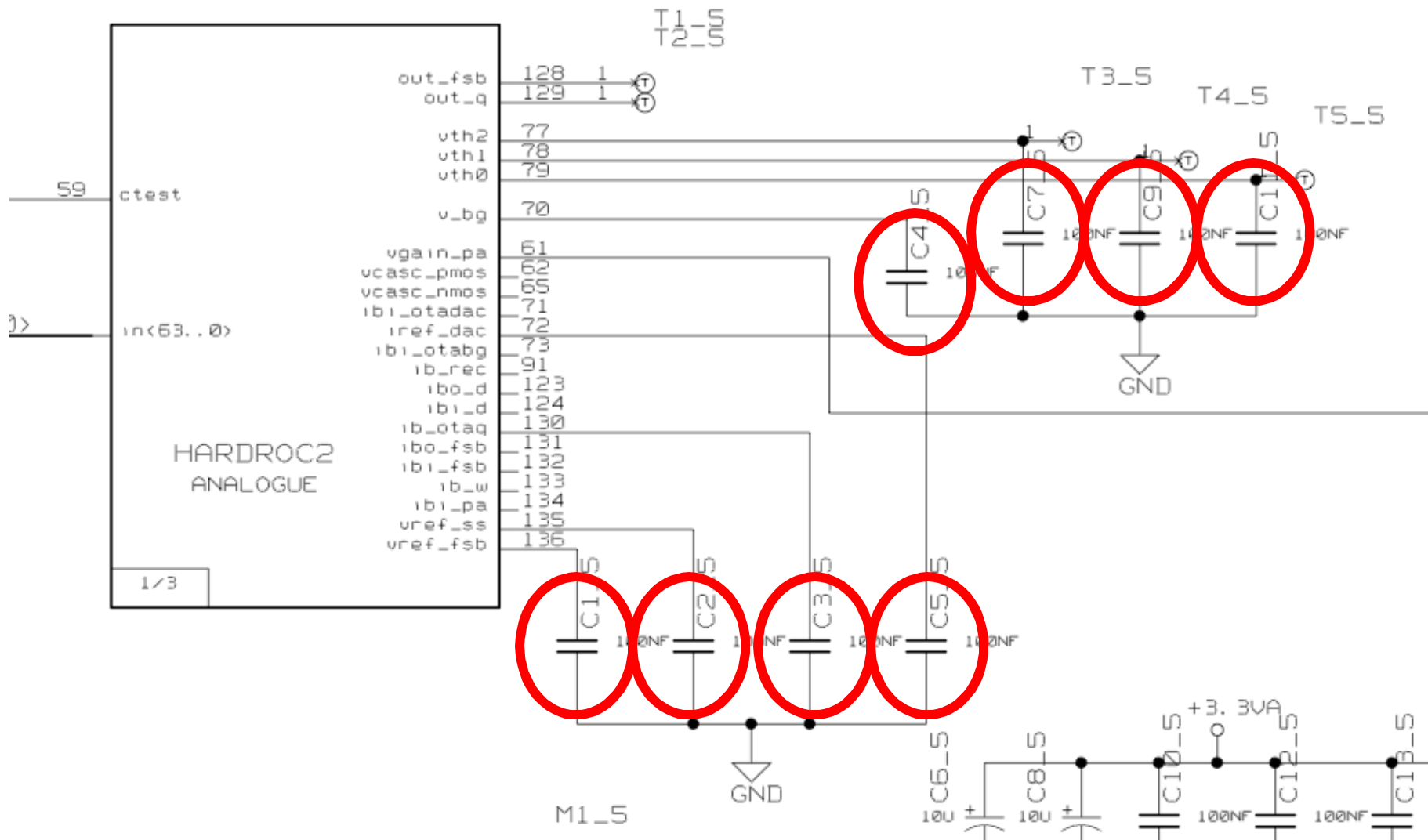
1. Record (reference) Scurves and Bias levels with no capacitor removed
2. Enable PP hardware on DIF (use of Mezzanine pin 1)
3. Enable PP in DIF firmware : PowerOn_x = register OR Mezzanine_1
4. Try PP with no capacitor removed
5. Remove Capacitors on biases of 1 HR2 step by step and check

That's where we are today

6. Record Scurves
7. Remove Capacitors on biases of all asics and check again
8. Record Scurves

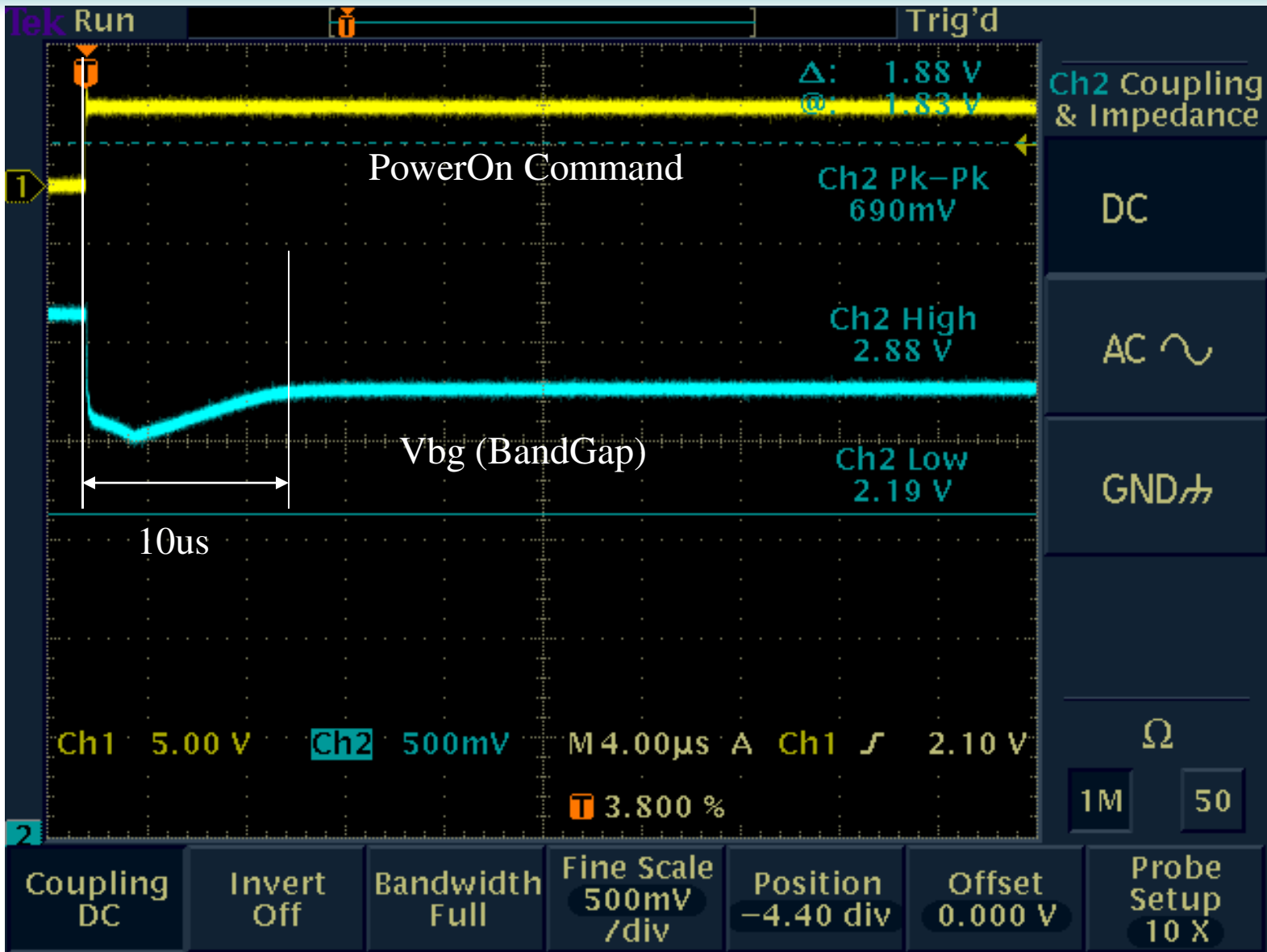


Power pulsing on Hardroc 2 ASU : method





Power pulsing on Hardroc 2 ASU : preliminary results





Power pulsing on Hardroc 2 ASU : preliminary results



One independent measurement station developed (USB, based on Labjack unit) with :

- 1 Pressure channel (atmospheric range)
- 1 Humidity channel
- 6 Temperature channels

One supplementary Labjack unit (8 independent free channels available)

- All included in a independent Xdaq application
- SOAP/I2O communication with Xdaq main DAQ
- Disk data logger
- Online display of parameters



Thank you